S J P N Trust's
Hirasugar Institute of Technology, Nidasoshi.
Inculcating Values, Promoting Prosperity
Approved by AICTE,Recognized by Govt.of Karnataka and Affiliated to VTU, Belagavi.
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ECE Dept.	
Academics	
Models/Charts	
2023-24	

Padagogical teaching Aids

Sem: VII   Sub Name : VLSI Design   Sub. 18EC72

VLSI DESIGN FLOW

System Specification

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Functional (Architecture) Design

⇩

Functional Verification

⇩

Logic Design

⇩

Logic Verification

⇩

Circuit Design

⇩

Circuit Verification

⇩

Physical Design

⇩

Layout Verification

⇩

Fabrication &Testing

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Front End Design:

The steps involved are explained below.

Design entry: It describes the RTL (Register Transfer Level) logics in HDLs. For this, we use any of the hardware description languages (HDLs) such as verilog and VHDL. This design specification contains all the details which all are required for the design architecture, RTL block diagram, clock frequency, frequency domain details, waveforms, port details etc.

Logic Synthesis: The RTL logic written is synthesized to get the gate level netlist. This process can be done with the help of EDA tools. The code written can be implemented on an FPGA board only if, it is synthesizable.

Gate level simulation: The gate level simulation of the logic is very important in the verification. The functional check, timing checks and the Power analysis checks are included in the verification.

Back End Design

The back end design includes following steps.

Schematic entry: Using the cadence schematic editor, you can create and extract the logic design you needed.

Pre layout simulation: The logic design is then verified, before doing its layout. The netlist of the schematic is generated and simulated using any of the tools such as Cadence ultrasim or Synopsys hspice. The working of each circuit can be checked using the simulation results.

Layout Design: After the schematic is simulated and verified, the corresponding mask layers of the circuit should be created which can be done using the Layout Editor by cadence. The layout design includes the floor planning, placement and routing. The locations of each schematic component are decided in the floor planning and are placed accordingly. While routing, the interconnections are done between the components.

Extracted simulation: The layout design should be extracted with the parasitics and simulate the system for performance using hspice or ultrasim. The parasitics can be either resistance or capacitances which are produced because of the interconnecting wires using for the routing. The parasitic components may affect the circuit performance badly. The parasitics cannot be avoided but can be reduced by proper routing. Finally the routed netlist that is called as GDS-II will be sent to the foundry and the chip will be manufactured as per the technology requirement.

Outcome : These charts will help them to rember the VLSI design flow hence help in improving teaching learning process.

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