INSTITUTE VISION

"To be a preferred institution in Engineering Education by achieving excellence in teaching and research and to remain as a source of pride for its commitment to holistic development of individual and society"

INSTITUTE MISSION

"To continuously strive for the overall development of students, educating them in a state of the art infrastructure, by retaining the best practices, people and inspire them to imbibe real time problem solving skills, leadership qualities, human values and societal commitments, so that they emerge as competent professionals"

DEPARTMENTAL VISION

“To be the centre of excellence in providing education in the field of Electronics and Communication Engineering to produce technically competent and socially responsible engineering graduates.”

DEPARTMENTAL MISSION

“Educating students to prepare them for professional competencies in the broader areas of the Electronics and Communication Engineering field by inculcating analytical skills, research abilities and encouraging culture of continuous learning for solving real time problems using modern tool”.

PROGRAM EDUCATIONAL OBJECTIVES (PEOs):

PEO1:

Acquire core competence in Applied Science, Mathematics, and Electronics and Communication Engineering fundamentals to excel in professional carrier and higher study.

PEO2:

Design, Demonstrate and Analyze the Electronic Systems which are useful to society.

PEO3:

Maintain Professional and Ethical values, Employability skills, Multidisciplinary approach and an Ability to realize Engineering issues to broader social contest by engaging in lifelong learning.

PROGRAM SPECIFIC OUTCOMES(PSOS)

The graduates will be able to:

PSO1:

An ability to understand the concepts of Basic Electronics and Communication Engineering and to apply them to various areas like Signal Processing, VLSI, Embedded Systems, Communication Systems and Digital & Analog Devices

PSO2:

An ability to solve complex Electronics and Communication Engineering problems, using latest hardware and software tools, along with analytical skills to arrive at cost effective and appropriate solutions

PROGRAM OUTCOMES (POs):

1. **Engineering knowledge**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
2. **Problem analysis**: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
3. **Design/development of solutions**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
4. **Conduct investigations of complex problems**: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
5. **Modern tool usage**: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
6. **The engineer and society**: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
7. **Environment and sustainability**: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainble development.
8. **Ethics**: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
9. **Individual and team work**: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
10. **Communication**: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
11. **Project management and finance**: Demonstrate knowledge and understanding of the engineering and mangement principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
12. **Life-long learning**: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

STUDENT HELP DESK

Sl. No	Name of the faculty	Activities
1	Dr.M.C.Sarasamba	GATE / Pre placement Coaching
		Students Mentor
		Module Coordinator
		Research Center Coordinator
		Dept. NAAC Criteria Sub Coordinator
		NBA Criteria Coordinator
2	Dr. S. S. Ittannavar	Dean Students Welfare
		GATE / Pre placement Coaching
		BSP /DSP Lab In charge
		Students Mentor
		Module Coordinator
		ISTE Convener & Dept. Coordinator
		NBA /NAAC Criteria Coordinator
		AICTE Coordinator
3	Dr. B. I. Kattimani	GATE / Pre placement Coaching
		NBA Criteria Coordinator
		Module Coordinator
		Students Mentor
		Internship Coordinator
		Communication Lab In charge
4	Prof. S. S. Malaj	GATE / Pre placement Coaching
		Adv. Comm. Lab In charge
		Central Counseling Coordinator
		Students Mentor
		NAAC Criteria Sub Coordinator
		NBA Criteria Coordinator
		Library Committee Member
		NIRF Coordinator
5	Prof. S. S. Kamate	GATE / Pre placement Coaching
		VLSI Lab In charge
		Students Mentor
		Module Coordinator
		IEEE Coordinator/ IA Coordinator
		Dept. NAAC Criteria Sub Coordinator
		Project Coordinator
		Class Teacher VI Sem
		NBA Criteria Coordinator

Sl. No	Name of the faculty	Activities
6	Prof. D. M. Kumbhar	GATE / Pre placement Coaching
		IOT Lab In charge
		Students Mentor
		Dept. Association Coordinator
		Class Teacher III Sem A Div
		IIIC Coordinator
		Dept. NAAC Criteria Sub Coordinator
		NBA Criteria Coordinator
		Institute & Dept. ED Cell Coordinator
7	Prof. S. S. Patil	GATE / Pre placement Coaching
		ARM & ES Lab In charge
		Students Mentor
		NAAC Criteria 7 Convenor
		NBA Criteria Coordinator
		Admission Coordinator
		Module Coordinator
8	Prof. D. B. Madihalli	GATE / Pre placement Coaching
		DSD Lab In charge
		UHV Coordinator
		Students Mentor
		NBA / NAAC Coordinator
		News & Publicity Coordinator
		NBA Criteria Coordinator
		Website Coordinator
		VTU LIC Coordinator
9	Prof. P. V. Patil	GATE / Pre placement Coaching
		E- Yantra Lab In charge
		Students Mentor
		NBA /NAAC Criteria Coordinator
		Dean TP & IIIC Cell
		SPOC PMV & PMKEY
		Alumni Coordinator

Sl. No	Name of the faculty	Activities
10	Prof. B. P. Khot	GATE / Pre placement Coaching
		MC Lab In charge
		Students Mentor
		Dept. Time Table Coordinator
		Dept. Meeting Coordinator
		Class Teacher VIII Sem
		NBA/NAAC Criteria Coordinator
		Dept T&P Cell Coordinator
		Seminar Coordinator
11	Prof. S. R. Mallurmath	EMS Coordinator
		ERP Coordinator
		GATE / Pre placement Coaching
		Students Mentor
		News Letter / Technical Magazine
		Class Teacher III Sem B Div
		NBA/NAAC Criteria Coordinator
12	Prof. K.S.Patil	GATE / Pre placement Coaching
		Students Mentor
		NBA /NAAC Criteria Coordinator
		AICTE Activity Coordinator
13	Prof. S. M. Patil	GATE / Pre placement Coaching
		Students Mentor
		EMS Coordinator
		NBA Criteria Coordinator

CONTENTS

DEPARTMENTAL RESOURCES

Department of Electronics and Communication Engineering was established in the year 1996 and is housed in total area of **1112.83 Sq. Mtrs**.

FACULTY POSITION

S.N.	Category	No. in position	Average experience
1	Teaching faculty.	10	18.64Y
2	Technical supporting staff.	03	24.02Y
3	Helper staff	02	23.03Y

MAJOR LABORATORIES

S. N.	Name of the laboratory	Area in Sq. Mtrs	Amount Invested in Lakhs	S. N.	Name of the laboratory	Area in Sq. Mtrs	Amount Invested in Lakhs
1	Digital Electronics Lab	71	1.54	5	VLSI Lab	71	39.03
2	Analog Electronics Lab	92	8.24	6	Project Lab	95	--
3	Advanced Commn & Commn + LIC Lab	92	20.01	7	Research/E-Yantra/DSP & C.N.Lab	71	12.15
4	HDL/MC / EMD Lab	71	22.61	8	Power Electronics Lab	--	4.86
Total Investment in The Department						**Rs. 109.09 Lacs**	

TEACHING FACULTY DETAILS

Sl. No.	Name	Designation	Qualification	Specialization	Professional Membership	Teaching Exp.	Contact No.
1	Dr. M. C. Sarasamba	Prof. & HOD	Ph.D	Micro strip Antenna	LMISTE	20Y.06M	9480714746
2	Dr. S .S .Ittannavar	Assoc. Prof	Ph.D	DSP	LMISTE	12Y.00M	9964299498
3	Dr. B. I. Kattimani	Assoc. Prof	Ph.D	Micro strip Antenna	LMISTE	16Y.00M	9060467209
4	Prof. S. S. Malaj	Asst. Prof	M.E.	E & TC	LMISTE	27Y.08M	9731795803
5	Prof. S. S .Kamate	Asst. Prof	M.Tech	Digital Electronics	LMISTE	22Y.01M	9008696825
6	Prof. D.M. Kumbhar	Asst. Prof	M.Tech	Electronics	LMISTE	21Y.00M	09373609880
7	Prof. S .S. Patil	Asst. Prof	M.Tech	VLSI & Embedded	LMISTE	20Y.09M	9448102010
8	Prof. D. B. Madihalli	Asst. Prof	M.Tech	Industrial Electronics	LMISTE	17Y.08M	9902854324
9	Prof. P. V. Patil	Asst. Prof	M.Tech	VLSI & Embedded	LMISTE	12Y.06M	9731104059
10	Prof. B. P. Khot	Asst. Prof	M.Tech	Microelectronics & Control Systems	--	9Y.00M	9964019501
11	Prof. S. R. Mallurmath	Asst. Prof	M.Tech	Industrial Electronics	LMISTE	12Y.00M	7259865769
12	Prof. K. S. Patil	Asst. Prof	M.Tech	VLSI	LMISTE	30Y.06M	9902682781
13	Prof. S. M. Patil	Asst. Prof	M.Tech	VLSI & EMD	--	02Y.00M	9986238640

TECHNICAL SUPPORTING STAFF

S.N.	Name	Qualification	Experience
1.	Sri. P. S. Desai	DEC	24Y-.07M
2.	Sri.M.A.Attar	DEC	14Y-09M
	Sri. M.S. Byali	DEC	14Y-09M

SCHEME OF TEACHING AND EXAMINATION
VI Sem ECE

VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI
B.E. in Electronica and Communication Engineering
Scheme of Teaching and Examinations2022
Outcome Based Education (OBE) and Choice Based Credit System (CBCS)
(Effective from the academic year 2023-24)

VI SEMESTER

Sl. No	Course and Course Code		Course Title	Teaching Department (TD) and Question Paper Setting Board (PSB)	Teaching Hours /Week				Examination				Credits
					Theory Lecture	Tutorial	Practical/ Drawing	SDA	Duration in hours	CIE Marks	SEE Marks	Total Marks	
					L	T	P	S					
1	IPCC	BEC601	Embedded System Design	TD- ECE/ETE PSB-ECE/ETE	3	0	2		03	50	50	100	4
2	PCC	BEC602	VLSI Design and Testing	TD- ECE/ETE PSB-ECE/ETE	4	0	0		03	50	50	100	4
3	PEC	BEC613x	Professional Elective Course	TD- ECE/ETE PSB-ECE/ETE	3	0	0		03	50	50	100	3
4	OEC	BEC654x	Open Elective Course	TD- ECE/ETE PSB-ECE/ETE	3	0	0		03	50	50	100	3
5	PROJ	BEC685	Major Project Phase I	TD- ECE/ETE PSB-ECE/ETE	0	0	4		03	100	--	100	2
6	PCCL	BECL606	VLSI Design and Testing Lab	TD- ECE/ETE PSB-ECE/ETE	0	0	2		03	50	50	100	1
7	AEC/SDC	BEC657x	Ability Enhancement Course/Skill Development Course V	TD- ECE/ETE PSB-ECE/ETE	If the course is offered as a Theory 1	0	0		01	50	50	100	1
					If course is offered as a practical 0	0	2						
8	MC	BNSK658	National Service Scheme (NSS)	NSS coordinator	0	0	2			100	---	100	0
		BPEK658	Physical Education (PE) (Sports and Athletics)	Physical Education Director									
		BYOK658	Yoga	Yoga Teacher									
9	IKS	BIKS609	Indian Knowledge System		1	0	0		01	100	---	100	0
									Total	**600**	**300**	**900**	**18**

Professional Elective Course

BEC613A	**Multimedia Communication**	BEC613C	Digital Image Processing

BEC613B	Computer and Data Security	BEC613D	FPGA System Design using Verilog
Open Elective Course			
BEC654A	Digital System Design using Verilog	BEC654C	Electronic Communication Systems
BEC654B	Consumer Electronics	BEC654D	Basic VLSI Design
Ability Enhancement Course / Skill Enhancement Course-V			
BEC657A	FPGA System Design using Verilog LAB	BEC657C	IOT Lab
BEC657B	System Modelling using Simulink	BEC657D	Python Programming for Machine Learning Applications

PCC: Professional Core Course, **PCCL**: Professional Core Course laboratory, **UHV**: Universal Human Value Course, **MC**: Mandatory Course (Non-credit), **AEC**: Ability Enhancement Course, **SEC**: Skill Enhancement Course, **L:** Lecture, **T**: Tutorial, **P**: Practical **S= SDA**: Skill Development Activity, **CIE**: Continuous Internal Evaluation, **SEE**: Semester End Evaluation. **K :** The letter in the course code indicates common to al the stream of engineering. **PROJ**: Project /Mini Project. **PEC**: Professional Elective Course. **PROJ**: Project Phase -I, **OEC**: Open Elective Course

Professional Core Course (IPCC): Refers to Professional Core Course Theory Integrated with practicals of the same course. Credit for IPCC can be 04 and its Teaching–Learning hours (L : T : P) can be considered as (3 : 0 : 2) or (2 : 2 : 2). The theory part of the IPCC shall be evaluated both by CIE and SEE. The practical part shall be evaluated by only CIE (no SEE). However, questions from the practical part of IPCC shall be included in the SEE question paper. For more details, the regulation governing the Degree of Bachelor of Engineering /Technology (B.E./B.Tech.) 2022-23

National Service Scheme /Physical Education/Yoga: All students have to register for any one of the courses namely National Service Scheme (NSS), Physical Education (PE)(Sports and Athletics), and Yoga(YOG) with the concerned coordinator of the course during the first week of III semesters. Activities shall be carried out between III semester to the VI semester (for 4 semesters). Successful completion of the registered course and requisite CIE score is mandatory for the award of the degree. The events shall be appropriately scheduled by the colleges and the same shall be reflected in the calendar prepared for the NSS, PE, and Yoga activities. These courses shall not be considered for vertical progression as well as for the calculation of SGPA and CGPA, but completion of the course ismandatory for the award of degree.

Professional Elective Courses (PEC): A professional elective (PEC) course is intended to enhance the depth and breadth of educational experience in the Engineering and Technology curriculum. Multidisciplinary courses that are added supplement the latest trend and advanced technology in the selected stream of engineering. Each group will provide an option to select one course. The minimum number of students' strengths for offering professional electives is 10. However, this conditional shall not be applicable to cases where the admission to the program is less than 10.

Open Elective Courses:

Students belonging to a particular stream of Engineering and Technology are not entitled to the open electives offered by their parent Department. However, they can opt for an elective offered by other Departments, provided they satisfy the prerequisite condition if any. Registration to open electives shall be documented under the guidance of the Program Coordinator/ Advisor/Mentor. The minimum number of students' strength for offering Open Elective Course is 10. However, this condition shall not be applicable to class where the admission to the program is less than 10.

Project Phase-I : Students have to discuss with the mentor /guide and with their helphe/she has to complete the literature survey and prepare the report and finally define the problem statement for the project work.

S J P N Trust's
Hirasugar Institute of Technology, Nidasoshi.
Approved by AICTE, New Delhi, Permanently Affiliated to VTU, Belagavi Recognized under 2(f) & 12B of UGC Act, 1956
Accredited at 'A+' Grade by NAAC & Programmes Accredited by NBA:CSE & ECE

IQAC
Institute CoE
AY:2024-25 (Even)
Rev: 03

INSTITUTE CALENDAR OF EVENTS (CoE)

AY: 2024-25 (Even Sems.: II , IV, VI & VIII) (w.e.f.: 10th Feb. 2025)

Ref: 1. VTU CoE Notifications No.: VTU/BGM/BoS/Academic Calendar/2024-25/5487 &5601, Dated :24th /29th Jan. 2025
2. IQAC Meeting No.:HSIT/NDS/NAAC/IQAC/Meeting-Actions-Proceedings/2024-25/32, Dated: 29th Jan. 2025
3. VTU CoE Notifications No.: VTU/BGM/BoS/Academic Calendar/2024-25/6056, Dated :21st Feb. 2025

Hirasugar Institute of Technology NIDASOSHI-591236 Dist: Belgaum.

February -2025

Sun	Mon	Tue	Wed	Thu	Fri	Sat
						1
2	3	4	5	6	7	8
9	10	11	12	13	14	15
16	17	18	19	20	21	22
23	24	25	26	27	28	

26th Feb. 2025 GH: Maha Shivaratri
27th Feb. 2025 LH: Mahadasoha of Shri. Math (UHV Program Org. by NSSD, DSCs & UHV Coordinator)

March-2025

Sun	Mon	Tue	Wed	Thu	Fri	Sat
30	31					1
2	3	4	5	6	7	8
9	10	11	12	13	14	15
16	17	18	19	20	21	22
23	24	25	26	27	28	29

30th March 2025 GH: Yugadi Festival
31st March 2025 GH: Kutub-A-Ramjan
19th March 2025 LH: Rang Panchami (Tentative)

April -2025

Sun	Mon	Tue	Wed	Thu	Fri	Sat
		1	2	3	4	5
6	7	8	9	10	11	12
13	14	15	16	17	18	19
20	21	22	23	24	25	26
27	28	29	30			

10th April 2025 GH: Mahaveer Jayanti
14th April 2025 GH: Dr. B.R. Ambedkar Jayanti
18th April 2025 GH: Good Friday
30th April 2025 GH: Basav Jayanti/Aksay-Trutiya

May -2025

Sun	Mon	Tue	Wed	Thu	Fri	Sat
				1	2	3
4	5	6	7	8	9	10
11	12	13	14	15	16	17
18	19	20	21	22	23	24
25	26	27	28	29	30	31

1st May 2025 GH: Labours Day

June -2025

Sun	Mon	Tue	Wed	Thu	Fri	Sat
1	2	3	4	5	6	7
8	9	10	11	12	13	14
15	16	17	18	19	20	21
22	23	24	25	26	27	28
29	30					

Date	Events & Holidays
10th Feb. 2025	Commencement of IV & VI Sem Classes & COP in 1st Week
11th Fab. 2025	International Day of Women & Girls in Science (Org. by WEC)
15th Feb. 2025	Commencement of 15 Weeks Industry/Research Internship (For VIII Sem ME, EE & CV)
21st -22nd Feb. 2025	Major Project Synopsis Presentation Cum Idea Presentation (For VIII Sem. CSE & ECE, Org. by DAs & DSCs)
27th -28th Feb. 2025	Major Project (Phase-I), Synopsis Presentation Cum Idea Presentation (For VI Sem. all branches, Org. by DSCs)
28th Feb. 2025	National Science Day (Org. by FYD)
7th -8th March 2025	International Conference(CRTET-25 (Org. by R&D Cell)
8th March 2025	International Women's Day (Org. by WEC & DSCs,)
12th-14th March 2025	1st IAT for IV & VI Sems. (On 01 CO/Module)
14th March 2025	1st Feedback on T&L Process by IV & VI Sems. Students.
17th March 2025	Commencement of Classes of II Sem & Student Induction Program (SIP) Phase-II (Tentative)
18th March 2025	Display of 1st IAT Marks of IV & VI Sems
20th March 2025	International Day of Happiness (Org. by NSSD & YRCD)
29th March 2025	Technovision-2025 (Host by CSE Dept. Org. by DSCs)
17th April 2025	Annual Sports Day (Host by: Sports Dept. & Org. by DSCs)
24th -26th April 2025	1st IAT for II Sem (On 01 CO/Module)& 2nd IAT for IV & VI Sems. (On 02 COs/ Modules covered after 1st IAT) (On 24th National Panchayathraj Day, Org. by NSSD & DSCs)
26th April 2025	1st Feedback on T&L Process by II Ses. Students. 2nd Feedback on T&L Process by IV & VI Sems. Students. (World Intellectual Property Day, Org. by DSCs, R&D Cell, ED Cell)
29th April 2025	1st Lab IAT for IV & VI Sems. (On 02 COs/5 Expts)
2nd May 2025	Display of 2nd /1st IA Test Marks of IV & VI/II Sems.
8th -9th May 2025	HSIT-QUEST-2025 (Host by ME Dept. Org. by DSCs) (On 8th World Red Cross Day, Org. by YRC, DSCs)
10th May 2025	SEE of NSS/PE/YOGA for VIII Sem (2021 Scheme)
13th -14th May 2025	Technical Seminar Presentation, (For VIII Sem: All branches , Org. by DAs)
12th -16th May 2025	Fun Week (Social & Cultural Activities) (Org. by NSS Cell & Sports Dept, DSCs & Host by EEE Dept.)
16th -17th May 2025	Project Exhibition (VI: All Branches & VIII Sem: CS & EC) (Org. by DAs & DSCs)
15th May 2025	Last Working Day of VIII Sems
20th May 2025	HSIT Shambhrama-25 (Host by EEE Dept. Org. by DSCs)
21st May 2025	Graduation Day (Host by ECE Dept. Org. by DSCs)
26th -28th May 2025	2nd IAT for II Sem, (On 02 COs/ Modules covered after 1st IAT) 3rd IAT for IV & VI Sems, (On 02 COs/Modules covered after 2nd IAT)
28th May 2025	2nd Feedback on T&L Process by II Sem. Students.
30th May 2025	Display of 3rd /2nd IA Test Marks of IV & VI/II Sems
30th May 2025	2nd Lab IAT for IV&VI Sems. (On remaining 03 COs/5Expts)
31st May 2025	Last Working Day of IV & VI Sems (World Tobacco Day, Org. by DSCs, NSSD & YRCD)
2nd June 2025	Display of final CIE (IAT+CCA) marks
16th-26th May 2025	VTU Theory Examinations (SEE) (For VIII Sems.)
27th May -2nd June 2025	VTU Practical/Internship/Project Examinations (For VIII Sem.)
13th-15th June 225	Alumni Meet/Re-Union/Activities (Org. by AA)
2nd -13th June 2025	VTU Practical Examinations (For IV & VI Sems.)
23rd -25th June 2025	3rd IAT II Sem. (On 02 COs/Modules covered after 2nd IAT)
28th June 2025	Last Working Day of II Sem
30th June 2025	Display of 3rd Test Marks of II Sem.
16th June-1st Aug. 2025	VTU Theory Examinations (SEE) (For IV & VI Sems.)
1st July -11th July 2025	VTU Practical Examinations (For II Sem.)
14th July-9th Aug. 2025	VTU Theory Examinations (SEE) (For II Sem.)
4th Aug. 2025	Commencement of AY: 2025-26, III & V Sems.
One week	Evaluation of COs-POs-PSOs Attainments through Direct & Indirect Methods after SEE revaluation results
5th June 2025	World Environment Day/Plastic free Awareness & Pledge, Org. by NSSD
12th June 2025	World Blood Donor Day, Org. by DSCs, YRCD & NSSD
21st June 2025	International YOGA Day, Org. by DSCs, Sports Dept. & NSSD

GH: General Holiday LH: Local Holiday NSS: National Service Scheme WEC: Women Empowerment Cell R&D: Research & Development YRC: Youth Red Cross CO: Course Outcome PO: Program Outcome IAT: Internal Assessment Test SIP: Student Induction Program COP: Course Orientation Program AA: Alumni Association SEE: Semester End Exams DSC: Dept. Student Council DA: Dept. Association ED: Entrepreneurship Development T&L: Teaching & Learning

21/02/2025

Dr. S. N. Topannavar
IQAC Coordinator
Hirasugar Institute of Technology
Nidasoshi-591236

Dr. S.C. Kamate
Professor & Principal
Hirasugar Institute of Technology,
NIDASOSHI-591236

Copy to all key authorities, displayed on N/Bs and circulated to all students through WhatsApp groups

Nidasoshi, Taq: Hukkeri, Dist: Belgaum, Karnataka - 591 236
Phone: 91-8333-278887, Fax:278886, Web: www.hsit.ac.in, Mail: principal@hsit.ac.in

Subject Title	**Embedded System Design**		
Subject Code	BEC601	**CIE Marks**	50
Number of Lecture Hrs / Week	03	**SEE Marks**	50
Total Number of Lecture Hrs	40	**Exam Hours**	03
			CREDITS –

FACULTY DETAILS:		
Name: Prof. S.R. Malluramath	**Designation:** Asst. Professor	**Experience:** 11 Years
No. of times course taught: 01	**Specialization:** Industrial Electronics	

1.0 Prerequisite Subjects:

Sl. No	Branch	Semester	Subject
01	Electronics & Communication Engineering	III	Digital system design using verilog
02	Electronics & Communication Engineering	IV	Microcontroller

2.0 Course Objectives

- Identify various components, their purpose, and their application to the embedded system's applicability.
- Program various embedded components using the embedded C program.
- Understand the embedded system's real-time operating system and its application in IoT.
- Understand the fundamentals of ARM-based systems, including architecture and its units like registers , debug interface, stack, MPU, Interrupts etc.
- Use the various instructions to program the ARM controller.

3.0 Course Outcomes

At the end of the course students will be able to:

	Course Outcome	POs
CO313.1	Describe the architectural features and instructions of 32-bit microcontroller ARM Cortex M3.	PO1-8,12
CO313.2	Apply the knowledge gained for Programming ARM Cortex M3 for different applications.	PO1-8,12
CO313.3	Understand the basic hardware components and their selection method based on the characteristics and attributes of an embedded system.	PO1-8,12
CO313.4	Understand the hardware software co-design and firmware design approaches.	PO1-8,12
CO313.5	Explain the need of real time operating system for embedded system applications.	PO1-8,12
Total Hours of instruction		40

4.0 Course Content

Content	RBT
Module-1 **08 Hours** **Introduction to Embedded System:** What is an Embedded Systems? Embedded systems Vs General computing systems, History of Embedded Systems, Classification of Embedded systems, Major Application Areas of Embedded Systems. Purpose of Embedded Systems, The Typical Embedded System, Microprocessor Vs Microcontroller, Differences between RISC and CISC, Harvard V/s Von-Neumann Processor/Controller Architecture, Big-endian V/s Little-endian processors, Memory (ROM and RAM types), Sensors & Actuators, The I/O Subsystem – I/O Devices, Light Emitting Diode (LED), 7- Segment LED Display, Optocoupler, Relay, Piezo buzzer, Push button switch, Communication Interfaces, On-board Communication Interface, External Communication Interface, Embedded Firmware, Other System Components. Text 1: All the Topics from Ch-1 and Ch-2.)	L1,L2
Module-2 **08 Hours** **Embedded System Design Concepts:** Characteristics and Quality Attributes of Embedded Systems, Operational and non-operational quality attributes, Embedded Systems-Application and Domain specific, Hardware Software Co-Design and Program Modeling (excluding UML), Embedded firmware design and development (excluding C language). Text 1: Ch-3, Ch-4 (4.1, 4.2.1 and 4.2.2 only), Ch-7 (Sections 7.1, 7.2 only), Ch-9 (Sections 9.1, 9.2, 9.3.1, 9.3.2 only)	L1,L2,L3
Module-3 **08 Hours** **RTOS and IDE for Embedded System Design:** Operating System basics, Types of operating systems, Task, process and threads (Only POSIX Threads with an example program), Thread preemption, Preemptive Task scheduling techniques, Task Communication, Task synchronization issues – Racing and Deadlock. How to choose an RTOS, Integration and testing of Embedded hardware and firmware, Embedded system Development Environment – Block diagram (excluding Keil). Text 1: Ch-10 (Sections 10.1, 10.2, 10.3, 10.5.2 , 10.7, 10.8.1.1, 10.8.1.2 only), Ch-12, Ch-13 (a block diagram before 13.1, only).	L1,L2,L3
Module-4 **08 Hours** **ARM Embedded Systems:** Introduction, RISC design philosophy, ARM design philosophy, Embedded system hardware – AMBA bus protocol, ARM bus technology, Memory, Peripherals, Embedded system software – Initialization (BOOT) code, Operating System, Applications. ARM Processor Fundamentals, ARM core dataflow model, registers, current program status register, Pipeline, Exceptions, Interrupts and Vector Table, Core extensions. Text 2: Chapter 1, 2	L1,L2,L3
Module-5 **08 Hours** **Introduction to the ARM Instruction set:** Introduction, Data processing instructions, Load – Store instruction, Software interrupt instructions, Program status register instructions, Loading constants, ARMv5E extensions, Conditional Execution. Text 2: Chapter 3	L1,L2,L3

5.0 Relevance to future subjects

Sl No	Semester	Subject	Topics
01	VIII	Project work	Microcontroller based projects
02	Higher	Embedded system	Design and Programming

6.0 Relevance to Real World

SL.No	Real World Mapping
01	Microcontroller based system design
02	Model creation for analysis
03	Development of a software applications

7.0 Gap Analysis and Mitigation

SL. No	Delivery Type	Details
01	Tutorial	Topic: ARM application development tutor
02	NPTEL	ARM Cortex M3 Microcontroller Application

8.0 Books Used and Recommended to Students

Text Books
1. Shibu K V, "Introduction to Embedded Systems", Tata McGraw Hill Education 2. Andrew N Sloss, Dominic System and Chris Wright, "ARM System Developers Guide", Elsevier, Morgan Kaufman publisher, 1st Edition, 2008.
Reference Books
1. Raj Kamal, "Embedded Systems: Architecture and Programming", Tata McGraw Hill, 2008.
Additional Study material & e-Books
1. ARM Cortex M3 Microcontroller data sheet

9.0 Relevant Websites (Reputed Universities and Others) for Notes /Animation / Videos Recommended

Website and Internet Contents References
1. https://archive.nptel.ac.in/courses/106/105/106105193/ 2. https://developer.arm.com/documentation/dui0068/b/ARM-Instruction-Reference 3. https://www.udemy.com/course/introduction-to-arm-cortex-m3-and-m4-processors/ 4. www.Nuvoton .com/websites on Advanced ARM Cortex Processors 5. https://alison.com/tag/embedded-systems

10.0 Magazines/Journals Used and Recommended to Students

Sl.No	Magazines/Journals	Website
1	IEEE	http://ieeexplore.ieee.org/Xplore/home.jsp
2	PC World	http://www.pcworld.com/article/146957/components/article.html

11.0 Examination Note

Assessment Details (both CIE and SEE):

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum, passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

CIE for the theory component of the IPCC (maximum marks 50):

- IPCC means practical portion integrated with the theory of the course.
- CIE marks for the theory component are 25 marks and that for the practical component is 25 marks.
- 25 marks for the theory component are split into 15 marks for two Internal Assessment Tests (Two Tests, each of 15 Marks with 01-hour duration, are to be conducted) and 10 marks for other assessment methods mentioned in 22OB4.2. The first test at the end of 40-50% coverage of the

syllabus and the second test after covering 85-90% of the syllabus.

- Scaled-down marks of the sum of two tests and other assessment methods will be CIE marks for the theory component of IPCC (that is for 25 marks).
- The student has to secure 40% of 25 marks to qualify in the CIE of the theory component of IPCC.

CIE for the practical component of the IPCC

- 15 marks for the conduction of the experiment and preparation of laboratory record, and 10 marks for the test to be conducted after the completion of all the laboratory sessions.
- On completion of every experiment/program in the laboratory, the students shall be evaluated including viva-voce and marks shall be awarded on the same day.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to 15 marks.
- The laboratory test (duration 02/03 hours) after completion of all the experiments shall be conducted for 50 marks and scaled down to 10 marks.
- Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for 25 marks.
- The student has to secure 40% of 25 marks to qualify in the CIE of the practical component of the IPCC.

SEE for IPCC

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (duration 03 hours)

- The question paper will have ten questions. Each question is set for 20 marks.
- There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), should have a mix of topics under that module.
- The students have to answer 5 full questions, selecting one full question from each module.
- Marks scored by the student shall be proportionally scaled down to 50 Marks.

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper may include questions from the practical component.

12.0 Course Delivery Plan

Module	Lecture No.	Content of Lecturer	% of Portion
Module 1:	1	**Introduction to Embedded System:** What is an Embedded Systems? Embedded Vs General computing system, Classification of Embedded systems	20
	2	History of Embedded Systems, Classification of Embedded systems.	
	3	Major Application Areas of Embedded Systems. Purpose of Embedded Systems	
	4	The Typical Embedded System, Microprocessor Vs Microcontroller,	
	5	Differences between RISC and CISC, Harvard V/s Von-Neumann Processor/Controller Architecture, Big-endian V/s Little-endian processors,	
	6	Memory (ROM and RAM types), Sensors & Actuators, The I/O Subsystem – I/O Devices, Light Emitting Diode (LED), 7- Segment LED Display	
	7	Opto coupler, Relay, Piezo buzzer, Push button switch, Communication Interfaces, On-board Communication Interface	
	8	External Communication Interface, Embedded Firmware, Other System Components	
Module 2:	9	**Embedded System Design Concepts:** Characteristics	40
	10	Quality Attributes of Embedded Systems	
	11	Operational and non-operational quality attributes	
	12	Embedded Systems-Application and Domain specific	
	13	Hardware Software Co-Design	
	14	Program Modeling (excluding UML)	
	15	Embedded firmware design (excluding C language)	
	16	Embedded firmware development (excluding C language)	

Module 3:	17	**RTOS and IDE for Embedded System Design:** Operating System basics	60
	18	Types of operating systems	
	19	Task, process and threads (Only POSIX Threads with an example program)	
	20	Thread preemption, Preemptive Task scheduling techniques,	
	21	Task Communication, Task synchronization issues – Racing and Deadlock	
	22	How to choose an RTOS,	
	23	Integration and testing of Embedded hardware and firmware	
	24	Embedded system Development Environment – Block diagram (excluding Keil)	
Module 4:	25	**ARM Embedded Systems:** Introduction, RISC design philosophy	80
	26	ARM design philosophy, Embedded system hardware	
	27	AMBA bus protocol, ARM bus technology	
	28	Memory, Peripherals, Embedded system software – Initialization (BOOT) code,	
	29	Operating System, Applications	
	30	ARM Processor Fundamentals	
	31	ARM core dataflow model, registers, current program status register,	
	32	Pipeline, Exceptions, Interrupts and Vector Table, Core extensions	

Module 5:	33	**Introduction to the ARM Instruction set:** Introduction	100
	34	Data processing instructions	
	35	Load – Store instruction	
	36	Software interrupt instructions	
	37	Program status register instructions	
	38	Loading constants	
	39	ARMv5E extensions	
	40	Conditional Execution	

13.0 QUESTION BANK

Module I

1. Explain the components of a typical embedded system in detail.
2. What is ASIC? Explain the role of ASIC in Embedded system Design?
3. What is the difference between Microprocessor and Microcontroller? Explain the role of Microprocessors and Microcontrollers in embedded system design?
4. What is the difference between RISC and CISC processors? Give an example for each.
5. What is the difference between: a. PLD and ASIC b. PROM and EPROM c. RAM and ROM.
6. What is sensor? Explain its role in embedded system design? Illustrate with example.
7. What is Actuator? Explain its role in embedded system design? Illustrate with example.
8. What is Embedded Firmware? What are the different approaches available for embedded firmware development?
9. Explain the difference between I2C and SPI communication Interface.
10. Compare the operation of ZigBee and Wi-Fi network.
11. Explain the role of watchdog timer in embedded system.

Module II

12. Explain the different characteristics of embedded systems in detail.
13. What is operational quality attribute? Explain the important operational quality attributes to be considered in any embedded system design.
14. What is non-operational quality attribute? Explain the important non-operational quality attributes to be considered in any embedded system design.

15. Explain the significance of the quality attributes Testability and Debug-ability in the embedded system design context.
16. Explain Time-to-market? What is its significance in product development?
17. Explain the Product Life Cycle Curve of an embedded product development.
18. Explain the role of embedded system in automotive domain.
19. Explain the different communication buses used in automotive application.
20. What is hardware software co-design? Explain the fundamental issues in hardware software co-design
21. What is the difference between Data Flow Graph (DFG) and Control Data Flow Graph (CDFG) model? Explain their significance in embedded system design.
22. Explain the different ' embedded firmware design' approaches in detail.
23. Explain the format of assembly language instruction.
24. What is relocatable code? Explain its significance in assembly programming.
25. Explain the limitations/drawbacks of 'Assembly language' based Embedded firmware development.
26. What is the difference between: a) C Vs Embedded C b) Compiler Vs Cross Compiler.

Module III

27. Describe in brief about types of Operating System.
28. Define process, thread and Task?
29. Compare OS and RTOS.
30. Define Inter process communication.
31. What are the various scheduling criteria for CPU scheduling?
32. What is mailbox, message queue and message pipe?
33. What is IPC? Mention the two different ways available for it.
34. Explain the various process interaction model in detail.
35. What is Inter Process Communication (IPC)? Give an overview of different IPC mechanisms adopted by various operating systems.

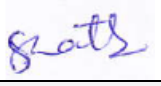
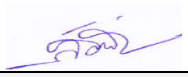
Module IV

36. **What is an ARM microcontroller?**
37. **What are the key features of the ARM architecture?**
38. **Explain the different ARM processor cores.**.
39. **What is the difference between ARM and Thumb instructions?**
40. **Describe the concept of memory-mapped I/O in ARM microcontrollers.**
41. **Explain the different memory types commonly found in ARM microcontrollers.**
42. What are the different types of interrupts available in ARM microcontrollers?
43. Describe the role of the Nested Vector Interrupt Controller (NVIC) in an ARM microcontroller.
44. **What is the concept of a "stack" in ARM programming?**
45. **Explain the difference between a direct memory access (DMA) controller and a general-purpose I/O (GPIO) port.**
46. **What are the different modes of operation for an ARM microcontroller?**
47. **What is a real-time operating system (RTOS) and how does it benefit ARM microcontroller applications?**

48. **What is the significance of the ARM System-on-Chip (SoC) architecture?**
49. **Explain the concept of a "peripheral" in an ARM microcontroller.**
50. **What are the different types of programming languages commonly used with ARM microcontrollers?**

Module V

51. Discuss the instruction set of ARM processor with examples?
52. Explain PSR Instructions with examples.
53. With relevant ARM instructions, explain the various forms of base-plus offset addressing.
54. Explain briefly the data processing instructions for ARM processor.
55. Differentiate ARM and Thumb instruction set features.
56. Explain Multiple – Register of Load-Store Instructions.

Prepared by	Checked by		
			
Prof. S. R. Malluramath	**Prof. S. S. Patil**	**HOD**	**Principal**

Subject Title	**VLSI Design and Testing**		
Subject Code	BEC602	**CIE Marks**	50
Number of Lecture Hrs / Week	04 L	**SEE Marks**	50
Total Number of Lecture Hrs	50	**Exam Hours**	03

FACULTY DETAILS:		
Name: Prof. S. S. Kamate	**Designation:** Asst. Professor	**Experience:21** yrs
No. of times course taught:01	**Specialization:** Digital Electronics	

1.0 Prerequisite Subjects:

Sl. No	Branch	Semester	Subject
01	ECE	III	Analog Electronic Circuits
02	ECE	III	DSDV

2.0 Course Objectives

1. ThiscoursedealswithanalysisanddesignofdigitalCMOSintegratedcircuits.
2. The course emphasizes on basic theory of digital circuits, design principles and techniques for digital design blocks implemented in CMOS technology.
3. Thiscoursewillalsocoverswitchingcharacteristicsofdigitalcircuitsalongwithdelay And power estimation.
4. Understanding the CMOS sequential circuits and memory design concepts.
5. Explore the knowledge of VLSI Design flow and Testing

3.0 Course Outcomes

Having successfully completed this course, the student will be able to draw and analyze.

	Course Outcome	Cognitive Level	POs
C314.1	ApplythefundamentalsofsemiconductorphysicsinMOStransistorsandanalyzethe geometrical effects of MOS transistors	U	PO1, PO2, PO3, PO5, PO8, PO10 PO12
C314.2	Designandrealizecombinational,sequentialdigitalcircuitsandmemorycellsinCMOS logic.	U	PO1, PO2, PO3, PO5, PO8, PO10 PO12
C314.3	Analyze the synchronous timing metrics for sequential designs and structured design basics.	U	PO1, PO2, PO3, PO5, PO8, PO10 PO12
C314.4	Understanddesigningdigitalblockswithdesignconstraintssuchaspropagationdelay and dynamic power dissipation.	U	PO1, PO2, PO3, PO5, PO8, PO10 PO12
C314.5	Understand the concepts of Sequential circuits design and VLSI testing	U	PO1, PO2, PO3, PO5, PO8, PO10 PO12
Total Hours of instruction		**50**	

4.0 Course Content

Course Content:

Module	Teaching Hours	Bloom's Taxonomy (RBT) level
Module 1: **Introduction to CMOS Circuits :**Introduction, MOS Transistors, MOS Transistor switches, CMOS Logic, Alternate Circuit representation, CMOS-nMOS comparison. [Text1:1.1,1.2,1.3,1.4,1.5.1.6.]	**8 Hours**	**L1, L2**
Module 2: **MOS Transistor Theory:** n-MOS enhancement transistor, p-MOS transistor, Threshold Voltage, Threshold voltage adjustment ,Body effect, MOS device design equations, V-I characteristics, CMOS inverter DC characteristics, Influence ofβn / βp ratio on transfer characteristics, Noise margin, Alternate CMOS inverters. Transmission gate DC characteristics. Latch-up in CMOS. [Text1:2.1,2.2,2.3,2.4,2.5.2.6.]	**8 Hours**	**L1,L2,L3**
Module 3: **CMOS Process Technology:** Silicon Semiconductor Technology, CMOS Technologies, Layout Design Rules. [Text1:3.1,3.2,3.3.] **Circuit Characterization and Performance Estimation:** Introduction, Resistance Estimation, Capacitance Estimation, Switching Characteristics, CMOS gate transistor sizing, Determination of conductor size, Power consumption, Charge sharing, Scaling of MOS transistor sizing, Yield. [Text1:4.1,4.2,4.3,4.4,4.5.4.6.4.7,4.8,4.9,4.10]	**8 Hours**	**L1,L2,L3**
Module 4 : **CMOS Circuit and Logic Design:** Introduction, CMOS Logic structures, CMOS Complementary logic, Pseudo n-MOS logic, Dynamic CMOS logic, Clocked CMOS Logic, Cascade Voltage Switch logic, Pass transistor Logic, Electrical and Physical design of Logic gates, The inverter, NAND and NOR gates, Body effect, Physical Layout of Logic gates, Input output Pads. [Text1:5.1,5.2,5.2.1,,5.2.2,5.2.3,5.2.4,5.2.6,5.2.8,5.3,5.3.1,5.3.2,5.3.4,5.3.8,5.5]	**8 Hours**	**L1,L2,L3**
Module 5: **Sequential MOS Logic Circuits:** Introduction, Behavior of Bistable Elements (Excluding Mathematical analysis) SR Latch Circuit, Clocked Latch and Flip-Flop Circuits, Clocked SR Latch, Clocked JK Latch. [Text2:8.1,8.2,8.3,8.4] **Structured Design and Testing:** Introduction**,** Design Styles, Testing. [Text1:6.1,6.2.6.5]	**8 Hours**	**L1,L2,L3**

5.0 Relevance to future subjects

Sl No	Semester	Subject	Topics
01	VII	VLSI Lab	VLSI Design of Circuits
02	VIII	Projects on VLSI	Projects and Research

6.0 Relevance to Real World

SL.No	Real World Mapping
01	Analyze different types of VLSI Designs
02	Design of different types of VLSI circuits

7.0 Gap Analysis and Mitigation

Sl. No	Delivery Type	Details
01	Tutorial	Topic: VLSI Lab
02	NPTEL	Demonstration and Application

8.0 Books Used and Recommended to Students

Text Books
1. Principals of CMOS VLSI Design System approach Neil HE Weste and Kamran Eshraghain . Addition Wisley Publishing company. 2. "CMOSDigitalIntegratedCircuits:AnalysisandDesign",SungMoKang&Yosuf Leblebici,Third Edition, Tata McGraw-Hill.
Reference Books
1."CMOSVLSIDesign-ACircuitsandSystemsPerspective",NeilHEWeste,andDavid Money Harris 4th Edition, Pearson Education. 2. "BasicVLSIDesign",DouglasAPucknell,KamranEshraghian,3rdEdition,PrenticeHallofIndiapublication, 2005.
Additional Study material & e-Books
2. VTU on line notes.

9.0 Relevant Websites (Reputed Universities and Others) for Notes/Animation/Videos Recommended

Website and Internet Contents References
01) https://nptel.co.in 02) http://m.noteboy.in/vtuflies 03) https://www.edx.org/school/iitbombayx?utm_source=bing&utm_medium=cpc&utm_term=iit-bombay&utm_campaign=partner-iit-bombay

10.0 Magazines/Journals Used and Recommended to Students

Sl. No	Magazines/Journals	website
1	IEEE Xplorer	http://ieee.com
2	International Journal of Science and Technology	http://www.sciencedirect.com/science/journal/00207683
3	Journal of Communication Engineering	http://ieee.com

11.0 Examination Note

Internal Assessment: 25 Marks
Three IA will be conducted and average of best of two will be accounted.

Scheme of Evaluation for Internal Assessment (20 Marks)

- Internal Assessment test in the same pattern as the of the main examination. (25marks.)

SCHEME OF EXAMINATION:
Two questions to be set from the syllabus covered.
Student has to answer one part each from each question.
Question 1 or 2 1x12.5 = 12.5Marks
Question 3 or 4 1x12.5 = 12.5Marks
Total = 25Marks

INSTRUCTION FOR SEE EXAMINATION

- Four full questions will be given which consists of a,b,c sub sections.
- Students have to answer either Q :1 or 2 and Q 3 or 4 completely.

SEM END EXAM(SEE): 100 Marks

1. Ten full questions will be given which consists of a,b,c,d sub sections. Each question is for 20marks
2. There are two questions from each module, students can attempt one full question from each module.

12.0 Course Delivery Plan

Course Delivery Plan:

MODULE	LECTURE NO.	CONTENT OF LECTURE	% OF PORTION
1	1	Introduction:	20
	2	MOS Transistors	
	3	MOS Transistors	
	4	MOS Transistor switches	
	5	Alternate Circuit representation	
	6	Alternate Circuit representation cont'd...	
	7	CMOS-nMOS comparison	
	8	CMOS-nMOS comparison cont'd...	
2	9	n-MOS enhancement transistor	
	10	p-MOS transistor	
	11	Threshold Voltage, Threshold voltage adjustment,	
	12	Body effect, MOS device design equations	
	13	V-I characteristics	
	14	CMOS inverter DC characteristics	
	15	Influence ofβn / βp ratio on transfer characteristics	
	16	Noise margin, Alternate CMOS inverters	
	17	Transmission gate DC characteristics, Latch-up in CMOS	
3	18	Silicon Semiconductor Technology	60
	19	CMOS Technologies	
	20	Layout Design Rules	
	21	Introduction, Resistance Estimation	
	22	Capacitance Estimation, Switching Characteristics	
	23	CMOS gate transistor sizing	
	24	Determination of conductor size	
	25	Power consumption	
	26	Charge sharing, Scaling of MOS transistor sizing, Yield.	
4	27	Introduction, CMOS Logic structures	80
	28	CMOS Complementary logic	
	29	Pseudo n-MOS logic, Dynamic CMOS logic	
	30	Clocked CMOS Logic	
	31	Cascade Voltage Switch logic	
	32	Pass transistor Logic,	
	33	Electrical and Physical design of Logic gates	
	34	The inverter, NAND and NOR gates	
	35	Physical Layout of Logic gates	
	36	Input output Pads	

5	37	Behavior of Bitable Elements SR Latch Circuit,	100
	39	SR Latch Circuit	
	40	Clocked Latch and Flip-Flop Circuits	
	41	Clocked SR Latch	
	42	Clocked JK Latch	
	43	Introduction to Structured Design and Testing	
	44	Design Styles,	
	45	Testing	

13.0 Assignments, Pop Quiz, Mini Project, Seminars

14.0 QUESTION BANK

MODULE -1

1.What is Moore's first law? Discuss about evaluation of integrated circuit technology.
2. Explain switching characteristics of nMOS.
3. Explain switching characteristics of pMOS
4. Explain basic CMOS structure.
5. Explain nMOS and pMOS characteristics.
6. Explain Alternative circuit representation.
7. Explain nMOS logic

MODULE -2

1. Draw & explain basic n-MOS enhancement mode transistor action.
2. Draw & explain basic p-MOS enhancement mode transistor action
3. What is threshold voltage? explain.
4. What is body effect?
5. Derive basic equation for Ids.
6. Draw & explain dc transfer characteristics of CMOS inverter.
7. Explain noise margin & CMOS inverter noise margins.
8. Draw & explain transfer characteristics of pseudo n-MOS inverter
9. Explain latch-up in CMOS.
10. Explain in detail, output characteristics of transmission gate.

.MODULE -3

1. Explain CMOS fabrication process.
2. Explain layout design rules.
3. Draw scaled n-MOS transistor for combined voltage & dimension model. Find out scaling factors for all parameters given below - gate area (Ag), gate capacitance per unit area (Co), gate capacitance (Cg), parasitic capacitance (Cx), carrier density in channel (Qon), channel resistance (Ron), gate delay (Td), maximum operating frequency (fo), saturation current (Idss), current density (J), switching energy per gate (Eg), power dissipation per gate (Pg), power dissipation per unit area (Pa), speed power product (PT).
4. Find out scaling effect on each factor in each model that is combined voltage & dimensional model, constant field model & constant voltage model in tabular form.
5. What is the effect of substrate doping on scaling factors?
6. What is the effect of substrate doping on depletion width?
7. What is the effect of miniaturization on minimum size of the transistor? And howit should be?
8. What is the effect on interconnect & contact resistance due to scaling down?What are the solutions for it?

MODULE -4

1. Explain CMOS logic structure.
2. Explain Pseudo n-MOS logic with an example
3. Explain Dynamic CMOS logic logic with an example
4. Explain Clocked CMOS Logic logic with an example
5. Explain Cascade Voltage Switch logic with an example
6. Explain Cascade Pass transistor Logic with an example.
7. Explain Electrical and Physical design of Logic gates
8. What is body effect?
9. Draw the physical layout of logic gates
10. Write notes on - i) pseudo n-MOS logic ii) Dynamic CMOS logic iii) Clocked
11. CMOS logic iv) CMOS domino logic v) n-p CMOS logic

MODULE-5

1. What are bitable elements briefly? explain their behavior.
2. Explain SR latch.
3. Explain Clocked Latch and Flip-Flop Circuits.
4. Explain Clocked SR Latch.
5. Explain Clocked JK Latch.
6. Explain Structured Design
7. Explain structured design styles
8. Explain Testing.

15.0 University Result

Examination	FCD	FC	SC	% Passing
New Subject				

Prepared by	Checked by		
			
Prof. S. S. KAMATE	Prof. S.S.KAMATE	HOD	Principal

Subject Title	**Digital Image Processing**		
Subject Code	**BEC613C**	**CIE Marks**	**50**
Teaching Hrs / Week(L:T:P:S)	**3:0:0:1**	**SEE Marks**	**50**
Total Number of Lecture Hrs	**40**	**Total Marks**	**100**
Credits	**3**	**Exam Hours**	**03**

Faculty Details:		
Name: Prof. B. P. Khot	**Designation: Assistant Professor**	**Experience: 9 Years**
No. of times course taught: 07	**Specialization: Microelectronics and control systems**	

1.0 Prerequisite Subjects:

Sr. No.	Branch	Semester	Subject
01	Electronics & Communication	III	Digital Electronics
02	Electronics & Communication	V	Digital signal Processing

2.0 Course Objectives

1. Understand the fundamentals of digital image processing.
2. Understand the image transform used in digital image processing.
3. Understand the image enhancement techniques in spatial domain used in digital image processing.
4. Understand the Color Image Processing and frequency domain enhancement techniques in digital image processing.
5. Understand the image restoration techniques and methods used in digital image processing.

3.0 Course Outcomes

Having successfully completed this course, the student will be able to

	Course Outcome	RBT Level	POs
C317.1	Understand image formation and the role human visual system plays in perception of gray and color image data.	L1, L2, L3	PO1-PO6, PO10-PO12
C317.2	Compute various transforms on digital images.	L1, L2, L3	PO1-PO6, PO10-PO12
C317.3	Conduct independent study and analysis of Image Enhancement techniques.	L1, L2, L3	PO1-PO6, PO10-PO12
C317.4	Apply image processing techniques in frequency (Fourier) domain.	L1, L2, L3	PO1-PO6, PO10-PO12
C317.5	Design image restoration techniques.	L1, L2, L3	PO1-PO6, PO10-PO12
Total Hours of instruction		40	

4.0 Course Content

Module-1	RBT Level
Digital Image Fundamentals: What is Digital Image Processing? Origins of Digital Image Processing, Examples of fields that use DIP, Fundamental Steps in Digital Image Processing, Components of an Image Processing System, Elements of Visual Perception, Image Sensing and Acquisition, Image Sampling and Quantization, Some Basic Relationships Between Pixels. [Text 1: Chapter 1, Chapter 2: Sections 2.1 to 2.5] 8 Hours	L1, L2, L3
Module-2	
Image Transforms: Introduction, Two-Dimensional Orthogonal and Unitary Transforms, Properties of Unitary Transforms, Two-Dimensional DFT, cosine Transform, Haar Transform. Text 2: Chapter 5: Sections 5.1 to 5.3, 5.5, 5.6, 5.9] 8 Hours	L1, L2, L3
Module-3	
Spatial Domain: Some Basic Intensity Transformation Functions, Histogram Processing, Fundamentals of Spatial Filtering, Smoothing Spatial Filters, Sharpening Spatial Filters [Text: Chapter 3: Sections 3.2 to 3.6] 8 Hours	L1, L2, L3
Module-4	
Frequency Domain: Basics of Filtering in the Frequency Domain, Image Smoothing and Image Sharpening Using Frequency Domain Filters. **Color Image Processing:** Color Fundamentals, Color Models, Pseudo-color Image Processing. [Text: Chapter 5: Sections 5.2, to 5.9] 8 Hours	L1, L2, L3
Module-5	
Restoration: A model of the Image Degradation/Restoration Process, Noise models, Restoration in the Presence of Noise Only using Spatial Filtering and Frequency Domain Filtering, Inverse Filtering, Minimum Mean Square Error (Wiener) Filtering. [Text 1: Chapter 5: Sections 5.1, to 5.4.3, 5.7, 5.8] 8 Hours	L1, L2, L3

5.0 Relevance to future subjects

Sr. No.	Semester	Subject	Topics
01	VIII	Project work	Image Processing Projects

6.0 Relevance to Real World

Sr. No.	Real World Mapping
01	Machine vision (Robotics)
02	Medical image Processing
03	Video processing (TVs, monitors, displays)

7.0 Gap Analysis and Mitigation

Sr. No.	Delivery Type	Details
01	NPTEL	Image Enhancement, Image Restoration

8.0 Books Used and Recommended to Students

Text Books
1. Digital Image Processing- Rafael C Gonzalez and Richard E Woods, PHI, 3rd Edition 2010. 2. Fundamentals of Digital Image Processing- A K Jain, PHI Learning Private Limited 2014.
Reference Books
1. Digital Image Processing- S Jayaraman, S Esakkirajan, T Veerakumar, Tata McGraw Hill, 2014

9.0 Relevant Websites (Reputed Universities and Others) for Notes /Animation / Videos Recommended

Website and Internet Contents References
1. Image databases, https://imageprocessingplace.com/root_files_V3/image_databases.htm 2. Student support materials, https://imageprocessingplace.com/root_files_V3/students/students.htm 3. NPTEL Course, Introduction to Digital Image Processing, https://nptel.ac.in/courses/117105079 4. Computer Vision and Image Processing, https://nptel.ac.in/courses/108103174 5. Image Processing and Computer Vision – Matlab and Simulink, 6. https://in.mathworks.com/solutions/image-video-processing.html

10.0 Magazines/Journals Used and Recommended to Students

Sr. No.	Magazines/Journals	Website
1	Introduction of Digital Image Processing	http://textofvideo.nptel.ac.in/117105135/lec1.pdf
2	Digital image fundamentals	http://www.acfr.usyd.edu.au/courses/amme4710/Lectures/AMME4710-Chap2-DigitalImageFundamentals.pdf
3	Image enhancement	https://link.springer.com/content/pdf/10.1007%2F978-1-4471-2751-2_4.pdf
4	Image Enhancement	http://textofvideo.nptel.ac.in/117105079/lec17.pdf
5	Image Restoration - I	http://textofvideo.nptel.ac.in/117105079/lec22.pdf
6	Color Image Processing	http://textofvideo.nptel.ac.in/117105079/lec26.pdf
7	Fundamental Concepts & an Overview of the Wavelet Theory	http://web.iitd.ac.in/~sumeet/WaveletTutorial.pdf
8	Mathematical Morphology- III	http://textofvideo.nptel.ac.in/117105079/lec35.pdf
9	Image Segmentation	http://textofvideo.nptel.ac.in/117105079/lec29.pdf

11.0 Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

1. Verilog /VHDL coding for Image manipulation.
2. Simulink models for Image processing.

12.0 Examination Note

Details Assessment (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

Three Unit Tests each of 20 Marks (duration 01 hour)

1. First test at the end of 5th week of the semester
2. Second test at the end of the 10th week of the semester
3. Third test at the end of the 15th week of the semester

Two assignments each of 10 Marks

4. First assignment at the end of 4th week of the semester
5. Second assignment at the end of 9th week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for 20 Marks (duration 01 hours)

6. At the end of the 13th week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination: Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (duration 03 hours)

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module.. Marks scored out of 100 shall be reduced proportionally to 50 marks

13.0 Course Delivery Plan

1	1	Digital Image Fundamentals: What is Digital Image Processing?	20
	2	Origins of Digital Image Processing	
	3	Examples of fields that use DIP,	
	4	Fundamental Steps in Digital Image Processing	
	5	Components of an Image Processing System	
	6	Elements of Visual Perception, Image Sensing and Acquisition	
	7	Image Sampling and Quantization	
	8	Some Basic Relationships Between Pixels	
2	9	Image Transforms: Introduction	20
	10	Two-Dimensional Orthogonal Transforms	
	11	**Two-Dimensional** Unitary Transforms	
	12	Properties of Unitary Transforms	
	13	Properties of Unitary Transforms	
	14	Two-Dimensional DFT	
	15	cosine Transform	
	16	Haar Transform	

3	17	Spatial Domain: Introduction	20
	18	Some Basic Intensity Transformation Functions	
	19	Some Basic Intensity Transformation Functions	
	20	Histogram Processing	
	21	Histogram Processing	
	22	Fundamentals of Spatial Filtering	
	23	Smoothing Spatial Filters	
	24	Sharpening Spatial Filters	
4	25	Frequency Domain: Introduction	20
	26	Basics of Filtering in the Frequency Domain	
	27	Basics of Filtering in the Frequency Domain	
	28	Image Smoothing Using Frequency Domain Filters	
	29	Image Sharpening Using Frequency Domain Filters	
	30	Color Image Processing: Color Fundamentals	
	31	Color Models	
	32	Pseudo-color Image Processing	
5	33	Restoration: A model of the Image Degradation/Restoration Process,	20
	34	Noise models,	
	35	Restoration in the Presence of Noise Only using Spatial Filtering	
	36	Restoration in the Presence of Noise Only using Spatial Filtering	
	37	Restoration in the Presence of Noise Only using Frequency Domain Filtering,	
	38	Restoration in the Presence of Noise Only using Frequency Domain Filtering,	
	39	Inverse Filtering,	
	40	Minimum Mean Square Error (Wiener) Filtering.	
		Total	100

14.0 Assignments, Pop Quiz, Mini Project, Seminars

Sr. No.	Title	Outcome expected	Allied study	Week No.	Individual / Group activity	Reference: book/website /Paper
1	Assignment 1:	Students study the Topics and write the Answers. Get practice to solve university questions.	Module 1,4,5 of the syllabus	4	Individual Activity.	Text Book 1, Reference book 1, 2 of the reference list. Website of the Reference list.
2	Assignment 2:	Students study the Topics and write the Answers. Get practice to solve university questions.	Module 2,3 of the syllabus	9	Individual Activity.	Text Book 1, Reference book 1, 2 of the reference list. Website of the Reference list.

15.0 QUESTION BANK

Module 1: Digital image fundamentals

1. What is digital image processing?
2. Write a note on origins of digital image processing.
3. Explain the fundamental steps in digital image processing.
4. Explain the fields that use DIP.
5. Explain about visual perception
6. Briefly explain the components of an image processing system.
7. Explain image sensing and acquisition.

Module 2: Digital image fundamentals

1. What is digital image processing?
2. Write a note on origins of digital image processing.
3. Explain the fundamental steps in digital image processing.
4. Explain the fields that use DIP.
5. Explain about visual perception
6. Briefly explain the components of an image processing system.
7. Explain image sensing and acquisition.

Module 3: Spatial Domain:

1. Explain image sampling and quantization.
2. Explain some basic relationships between pixels.
3. Write a note on linear and nonlinear operations.
4. Write a note on basic intensity transformation functions.
5. Explain histogram processing.
6. Explain the fundamentals of spatial filtering.
7. Write a note on smoothing spatial filters
8. Write a note on sharpening spatial filters.

Module 4: Frequency Domain

1. Explain preliminary concepts of selective filtering.
2. Explain Discrete Fourier Transform (DFT) of two variables.
3. Explain properties of the 2-D DFT.
4. Explain filtering in the frequency domain.
5. Write a note on image sharpening using frequency domain filters.
6. Write a note on image smoothing using frequency domain filters.
7. Write a note on color fundamentals.
8. Write a note on color models.
9. Explain pseudo color image processing.

Module 5: Restoration

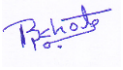
1. Write a note on restoration process.
2. Explain noise models.
3. Explain restoration in the presence of noise only, using spatial filtering.
4. Write a note on restoration in the presence of noise only, using frequency domain filtering.
5. Write a note on linear degradations.
6. Explain position-invariant degradations.
7. Explain Minimum Mean Square Error (Wiener) filtering.

15.0 University Result

Examination	FCD	FC	SC	% Passing
Dec.-2013/Jan-2014	37	04	01	100
Dec.-2014/Jan-2015	13	17	07	100
Dec.-2017/Jan-2018	21	10	04	100
Dec -2018/Jan-2019	31	15	09	100
Dec -2019/Jan-2020	28	09	06	100
Dec -2020/Jan-2021	25	10	00	100

2018 Scheme

Examination	S	A	B	C	D	E	% Passing
Feb 2022	9	12	9	2	3	-	100

Prepared by	Checked by		
			
Prof. B. P. Khot	Dr. S. S. Ittannavar	HOD	Principal

Subject Title	PROJECT MANAGEMENT		
Subject Code	BME654A	**IA Marks**	50
Number of Lecture Hrs / Week	03	**SEE**	50
Total Number of Lecture Hrs	40	**Exam Hours**	03
CREDITS – 03			

FACULTY DETAILS:		
Name: Nagaraj. T. Kambar	**Designation:** Asst. Professor	**Experience:**05
No. of times course taught:01	**Specialization:** Thermal Engineering	

1.0 Course Objectives

1. To understand how to break down a complex project into manageable segments and use of effective project management tools and techniques to arrive at solution and ensure that the project meets its deliverables and is completed within budget and on schedule.
2. To impart knowledge on various components, phases and attributes of a project.
3. To prepare students to plan, develop, lead, manage and successfully implement and deliver projects within their chosen practice area.

2.0 Course Outcomes

On completion of the course, the students will be able to;

1. Understand the selection, prioritization and initiation of individual projects and strategic role of project management.
2. Understand the work breakdown structure by integrating it with organization also the scheduling and uncertainty in projects.
3. Understand risk management planning using project quality tools also the activities like purchasing, acquisitions, contracting, partnering and collaborations related to performing projects.
4. Determine project progress and results through balanced score card approach.
5. Draw the network diagram to calculate the duration of the project and reduce it using crashing.

3.0 Course Content

MODULE – 1

INTRODUCTION

Definition of project, characteristics of projects, understand projects, types of projects, scalability of project tools, project roles Project Selection and Prioritization–Strategic planning process, Strategic analysis, strategic objectives, portfolio alignment–identifying potential projects, methods of selecting projects, financial mode/scoring models to select projects, prioritizing projects, securing and negotiating projects. **08 hours**

MODULE 2

Planning Projects: Defining the project scope, Project scope check list, Project priorities, Work Breakdown Structure (WBS), Integrating WBS with organization, coding the WBS for the information system.

Scheduling Projects: Purpose of a project schedule, historical development, how project schedules are limited and created, develop project schedules, uncertainty in project schedules, Gantt chart.

08 hours

MODULE 3

Resourcing Projects: Abilities needed when resourcing projects, estimate resource needs, creating staffing management plant, project team composition issues.

Budgeting Projects: Cost planning, cost estimating, cost budgeting, establishing cost control.

Project Risk Planning: Risk Management Planning, risk identification, risk analysis, risk response planning,

Project Quality Planning and Project Kickoff: Development of quality concepts, project quality management plan, project quality tools, kickoff project, baseline and communicate project management plan using

Microsoft Project for project baselines. **08 hours**

MODULE 4

Performing Projects: Project supply chain management:-Plan purchasing and acquisitions, plan contracting, contact types, project partnering and collaborations, project supply chain management.

P**roject Progress and Results:** Project Balanced Scorecard Approach, Internal project, customer, financial issues,

Finishing the project: Terminate project early, finish projects on time, secure customer feedback and approval, knowledge management, perform administrative and contract closure.

08 hours

MODULE 5

Network Analysis: Introduction, network construction - rules, Fulkerson's rule for numbering the events, AON and AOA diagrams; Critical path method (CPM) to find the expected completion time of a project, floats; PERT for finding expected duration of an activity and project, determining the probability of completing a project, predicting the completion time of project; crashing of simple projects.

4.0 Relevance to future subjects

Sl.No	Semester	Subject	Topics
01	VIII	Project work	Planning Projects, Scheduling Projects, Resourcing Projects, Budgeting Projects and Performing Projects.

5.0 Relevance to Real World

Sl.No	Real World Mapping
01	While working in an industry on project.

6.0 Gap Analysis and Mitigation

Sl. No	Delivery Type	Details
01	Tutorial	Topic: Agile Project Management
02	Tutorial	Topic: Project Manager
03	Tutorial	Topic: Human Factors and Project Team

7.0 Books Used and Recommended to Students

Text Books
1 Project Management Timothy J Kloppenborg Cengage Learning Edition 2009
2 Project Management-A systems approach to planning scheduling and controlling Harold kerzner CBS publication
3 Project Management S Choudhury McGraw Hill Education(India)Pvt.Ltd.NewDelhi2016

Reference Books
1 Project Management Pennington Lawrence McGrawHill 2 Project Management A Moder Joseph and Phillips New Yark Van Nostrand Reinhold 3 Project Management, Bhavesh M. Patel Vikas publishing House
Additional Study material & e-Books
3. "Contemporary project management" by Thimothy J Kloppenberg

8.0 Relevant Websites (Reputed Universities and Others) for Notes/Animation/Videos Recommended

Website and Internet Contents References
1) https://en.wikipedia.org/wiki/Project_management *2) https://www.manage.gov.in/studymaterial/PPM-E.pdf* 3) https://www.scribd.com/document/475871105/FINAL-Word 4) https://www.planview.com/resources/guide/what-is-project-management/

9.0 Magazines/Journals Used and Recommended to Students

Sl.No	Magazines/Journals	website
1	Project management journal	https://journals.sagepub.com/toc/pmxa/current
2	International journal of project management	https://www.sciencedirect.com/science/article/pii/S0263786315001027
3	Complexity in project management	https://www.sciencedirect.com/science/article/pii/S1877050917323001
4	Project management planning and control	https://www.sciencedirect.com/book/9780081020203/project-management-planning-and-control

10.0 Examination Note

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIEis40% of the maximum marks (20marksoutof 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together

Continuous Internal Evaluation:

- The CIE is the sum of Average of **Two Internal Assessment Tests each of 25 marks** and any two Assessment methods for **25 marks**.
- The first test will be administered after 40-50% of the syllabus has been covered, and the second test will be administered after 85-90% of the syllabus has been covered.
- Any two assessment methods mentioned in the 22OB 42, if an assignment is project based then only one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned.
- For the course, CIE marks will be based on a **scaled down sum of two tests** and other methods of assessment for a total of **50 marks**.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:
Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**).

1. The question paper will have ten questions. Each question is set for **20 marks**.
2. There will be **2 questions** from each module. Each of the two questions under a module (with a maximum of 3 sub questions), should have a mix of topics under that module.
3. The students have to answer 5 full questions, selecting **one full question** from each module.
4. Marks scored shall be proportionally reduced to **50 marks**

11.0 Course Delivery Plan

Module	Lecture No.	Content of Lecturer	% of Portion
Module 1:	1	Introduction to Project Management, Definition of project, characteristics of projects, understand projects	20
	2	types of projects, scalability o project tools	
	3	project roles Project Selection and Prioritization – Strategic planning process	
	4	Strategic analysis, strategic objectives	
	5	portfolio alignment – identifying potential projects	
	6	methods of selecting projects	
	7	financial mode / scoring models to select projects	
	8	Prioritizing projects, Securing and negotiating projects.	
Module 2:	9	**Planning Projects:** Defining the project scope, Project scope checklist	20
	10	Project priorities, Work Breakdown Structure (WBS)	
	11	Integrating WBS with organization, coding the WBS for the information system.	
	12	**Scheduling Projects:** Purpose of a project schedule	
	13	historical development, how project schedules are limited and created	
	14	develop project schedules	
	15	uncertainty in project schedules	
	16	Gantt chart.	
Module 3:	17	**Resourcing Projects:** Abilities needed when resourcing projects, estimate resource needs	20
	18	creating staffing management plant, project team composition issues	
	19	**Budgeting Projects:** Cost planning, cost estimating	
	20	Cost budgeting, establishing cost control.	
	21	**Project Risk Planning**: Risk Management Planning, risk identification, risk analysis, risk response planning	
	22	**Project Quality Planning and Project Kick off:** Development of quality concepts, project quality management plan	
	23	project quality tools, kick off project, baseline and	
	24	Communicate project management plan using Microsoft Project for project baselines.	
Module 4:	25	**Performing Projects and Project supply chain management:** - Plan purchasing and acquisitions, plan contracting	20
	26	Contact types, project partnering and collaborations, project supply chain management.	
	27	**Project Progress and Results:** Project Balanced Scorecard Approach	
	28	Internal project, customer, financial issues	
	29	**Finishing the project:** Terminate project early, finish projects on time	
	30	secure customer feedback and approval	
	31	Knowledge management	
	32	Perform administrative and contract closure.	

Module 5:	33	**Network Analysis:** Introduction	20
	34	network construction - rules	
	35	Fulkerson's rule for numbering the events, AON and AOA diagrams	
	36	Critical path method (CPM) to find the expected completion time of a project floats	
	37	PERT for finding expected duration of an activity and project	
	38	determining the probability of completing a project	
	39	predicting the completion time of project	
	40	Crashing of simple projects.	

12.0 Assignments, Pop Quiz, Mini Project, Seminars

Sl.No.	Title	Outcome expected	Allied study	Week No.	Individual / Group activity	Reference: book /website /Paper
1	Assignment 1:	Students study the Topics and write the Answers. Get practice to solve university questions.	Module 1& 2 of the syllabus	4	Individual Activity.	Books 1, 2 and 3 of the text book list
2	Assignment 2:	Students study the Topics and write the Answers. Get practice to solve university questions.	Module 3,4 & 5 of the syllabus	9	Individual Activity.	Books 1, 2 and 3 of the text book list

13.0 QUESTION BANK

Module 1

1. What is a project?
2. What is project management?
3. What types of constraints are common to most projects?
4. Which deliverable authorizes the project team to move from Selecting & Initiating to Planning?
5. At what stage of a project life cycle are the majority of the "hands-on" tasks completed?
6. What are the five process groups of project management?
7. What are the 10 project management knowledge areas?
8. What two project dimensions are components of project performance?
9. How do you define project success?
10. How do you define project failure?
11. List four common causes of project failure.
12. What are three common ways of classifying projects?
13. List and describe each step in the strategic planning process.
14. Name five things that may be negotiated between a client company and a contractor company
15. What are some common reasons for project failure?

Module 2

1. List three reasons why understanding stakeholder is important to successful project management.
2. What is the difference between an internal and external stakeholder?
3. Which three criteria should you consider when prioritizing stakeholders?
4. Describe an AGILE "stand-up" meeting.
5. What three tasks comprise the "define scope" process?
6. Why is scope definition important?
7. What are two common causes of scope creep?
8. What does the acronym WBS stand for?
9. What are the advantages of using a WBS?
10. List three ways of organizing a WBS.
11. The lowest level of the WBS is known as?
12. What items are typically included in a work package description?
13. What is rolling wave planning?
14. What is uncontrolled change known as?

15. Why do project teams use change control systems?
16. List the major sections that should be included in a change request form, and tell why each is important.
17. When can the first draft of a project schedule be constructed?
18. What is the difference between an activity and a work package?
19. How can a **Gantt chart** be helpful in project planning?

Module 3

1. In addition to technical skills, what other skill must a project manager have in order to successful resource a project?
2. Why is it important to involve workers in the planning phase of a project when possible?
3. What are two techniques used to compress a project schedule?
4. When crashing a project, what two criteria are considered when deciding which activities to speed up?
5. What type of costs does not depend on the size of a project?
6. During which phase of a project do recurring costs typically occur?
7. What are some examples of expedited costs?
8. What is the purpose of an order of magnitude cost estimate?
9. What is the "time value of money," and why is it relevant to project management?
10. For a routine project, what is a typical percentage of total project costs that should be placed into contingency reserves? For an unusual project?
11. Should a project manager alone identify potential risks for the project? Why or why not?
12. During which stage of a project are most risks typically uncovered?
13. Are both qualitative and quantitative risk analyses used on all projects? Why or why not?
14. What is an example of transferring risk?
15. In the risk register, why should only one person be assigned "owner" of a risk?
16. Identify similarities and differences among TQM, ISO, and Six Sigma. What strengths and weaknesses are inherent in each of these approaches?
17. Discuss the areas of ISO. Which do you feel is most important and why?
18. Describe the process of achieving stakeholder satisfaction. Why is it important to consider stakeholder satisfaction?
19. Describe the three outputs of quality control.
20. List the project quality tools you expect to use on your project. Tell where you plan to use each tool and why it is important.

Module 4

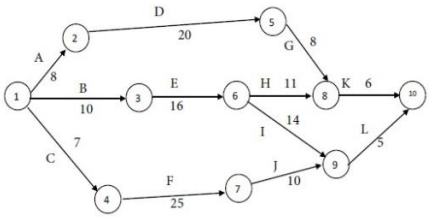
1. Do small businesses often outsource project work? Why or why not?
2. Which is the first of the four processes that make up project procurement management?
3. In supply chain management, what are some other names for the seller? What are some other names for the buyer?
4. List three functional areas that are frequently outsourced by business organizations.
5. What are some potential issues related to outsourcing?
6. What are four potential information sources that organizations can use to identify potential sellers?
7. Describe two methods that can be used to evaluate potential suppliers.
8. What items are generally included in a request for proposal?
9. What is the primary reason for determining project progress and results?
10. Which five aspects of project success are evaluated in the balanced scorecard approach?
11. Give three categories of internal project issues and an example of each.
12. In addition to the WBS, what might trigger project work to be authorized and performed?
13. What is an advantage of letting workers self-control their work?
14. How does one calculate schedule variance?
15. What does cost performance index (CPI) measure?
16. When does a project move into the closing stage?
17. What is validate scope?
18. What is the purpose of a "punch list"?
19. What should a project manager refer back to in order to make sure that all planned work has, in fact, been completed?
20. When might a contract clause be invoked?
21. If an early termination of his project seems likely, what two avenues can a project manager explore to increase the likelihood of being able to continue the project?

Module 5

1. What is network analyses? Write its salient feature.
2. Define following
   i) Pert
   ii) CPM
3. How 20 key project manager actions are organized? Explain.
4. What is material requirement planning (MRP)? define it with suitable example
5. How MRP is a 'push' system while JIT is a 'pull' system? explain it
6. Determine the critical path, the critical activities and the project completion time
   The following details are available regarding a project:

Activity	Predecessor Activity	Duration (Weeks)
A	-	3
B	A	5
C	A	7
D	B	10
E	C	5
F	D,E	4

7. Find out the completion time and the critical activities for the following project:



8. Draw the network diagram and determine the critical path for the following project

Activity	Time estimate (Weeks)
1- 2	5
1- 3	6
1- 4	3
2 -5	5
3 -6	7
3 -7	10
4 -7	4
5 -8	2
6 -8	5
7 -9	6
8 -9	4

9. Develop a network diagram for the project specified below

Activity	Immediate Predecessor Activity
A	-
B	A
C, D	B
E	C
F	D
G	E, F

14.0 University Result

New scheme subject

Prepared by	Checked by		
Prof. Nagaraj .T. Kambar	Prof. M A Hipparagi	HOD	Principal
Course coordinator	Module coordinator		

Subject Title	**VLSI Design and Testing LAB**		
Subject Code	**BECL606**	**IA Marks**	50
Number of Lecture Hrs / Week	2 Hrs. Lab	**Exam Marks**	50
Total Number of Lecture Hrs	40	**Exam Hours**	03

FACULTY DETAILS:		
Name: Prof. S. S. KAMATE	**Designation:** Asst. Professor	**Experience:** T-21.Yrs, I-00Yrs
No. of times course taught: 01	**Specialization:** Digital Electronics	

1.0 Prerequisite Subjects:

Sl. No	Branch	Semester	Subject
01	Electronics & Communication Engineering	III	Digital Electronics
02	Electronics & Communication Engineering	V	Fundamentals of CMOS VLSI
03	Electronics & Communication Engineering	VI	Microelectronics Circuits

2.0 Course Objectives

This course will enable students to:

- This laboratory course enables students to
- Design, model, simulate and verify digital circuits.
- Perform ASIC design flow and understand the process of synthesis, synthesis constraints and evaluating the synthesis reports to obtain optimum gate level netlist.
- Perform RTL-GDSII flow and understand the ASIC Design flow.

3.0 Course Outcomes

At the end of the course students will be able to:

	Course Outcome	Cognitive Level	POs
C323.1	Design and simulate combinational and sequential digital circuits using Verilog HDL	U	PO1, PO2, PO3, PO5, PO8, PO10,
C323.2	Understand the Synthesis process of digital circuits using EDA tool	U	PO1, PO2, PO3, PO5, PO8, PO10,
C323.3	Perform ASIC design flow and understand the process of synthesis, synthesis	U	PO1, PO2, PO3, PO5, PO8, PO10,
C323.4	Design and simulate basic CMOS circuits like inverter, common source amplifier	U	PO1, PO2, PO3, PO5, PO8, PO10,
C323.5	Perform RTL-GDSII flow and understand the stages in ASIC design	U	PO1, PO2, PO3, PO5, PO8, PO10,
Total Hours of instruction		**40**	

4.0 Course Content

Laboratory Experiments

Sl. No.	Experiments
1.	Designa4-BitAdder • Write a Verilog description • Verify the Functionality using Test-bench • Synthesizethedesignbysettingproperconstraintsandgeneratethegatelevelnetlist. FromthereportgeneratedidentifyCriticalpath,Maximumdelay,Totalnumberofcells,Power requirement and Total area required
2.	4-BitShiftandaddMultiplier • Write Verilog Code • Verify the Functionality using Test-bench • Synthesizethedesignbysettingproperconstraintsandobtainthegatelevelnetlist. From the report generated identify Critical path, Maximum delay, Total number of cells, Power requirement and Total area required
3.	32-BitALUSupporting4-Logicaland4-Arithmetic operations, using case and if statement for ALU Behavioral Modeling • Write Verilog description • Verify functionality using Test-bench • Synthesizethedesigntargetingsuitablelibraryandbysettingareaandtimingconstraints • Tabulate the Area ,Power and Delay for the Synthesized netlist • Identify Critical path
4.	Flip-Flops(D,SR and JK) • Write the Verilog description • Verify the Functionality using Test-bench • Synthesizethedesignbysettingproperconstraintsandobtainthegatelevelnetlist. From the report gate level netlist identify Critical path, Maximum delay, Total number of cells, Power requirement and Total area required. • VerifythefunctionalityusingGatelevelnetlistandcompare theresultsatRTLand gate level netlist.
5.	Four bit Synchronous MOD-N counter with Asynchronous reset • Write Verilog Code • Verify functionality using Test-bench • Synthesizethedesigntargetingsuitablelibraryandbysettingareaandtimingconstraints • Tabulate the Area ,Power and Delay for the Synthesized netlist Identify Critical path
6.	a) Construct the schematic of CMOS inverter with load capacitance of 0.1pF and set the widths of inverter with Wn=Wp,Wn =2Wp,Wn= Wp/2andlengthatselected technology. Carry out the following: i. Set the input signal to a pulse with rise time ,fall time of1nsandpulsewidthof10ns andthetimeperiodof20nsandplottheinputvoltageandoutputvoltageofdesigned inverter? ii. From the simulation result compute tpHL, tpLH and td for all three geometrical settings of width? iii. Tabulatetheresultsofdelayandfindthebestgeometryforminimumdelayfor CMOS inverter. Draw layout of inverter with Wp/Wn = 40/20, use optimum layout methods. Verify for DRCandLVS,extractparasiticandperformpostlayoutsimulations,compare theresults with pre layout simulations and compare the results.
7.	Capture the schematic of2-input CMOS NORg ate having similar delay as that of CMOS inverter computed in experiment above. Verify the functionality of NOR gate and also find out the delay td for all four possible combinations of input vectors. Table the results.Increasethedrivestrengthto2Xand4Xandtabulatetheresults.
8.	Construct the schematic of the Boolean Expression $Y=\overline{AB+CD+E}$usingCMOSLogic.Verifythefunctionalityoftheexpressionfind out the delay td for some combination of input vectors. Tabulate the results.

9.	a) Construct the schematic of Common Source Amplifier with PMOS Current Mirror Load and find its transient response and AC response ? Measure the Unit Gain Band width(UGB), amplification factor by varying transits or geometries, study the impact of variation in width to UGB. b) Draw Layout of common source amplifier, use optimumlay out methods. Verify for DRC & LVS, extract parasitic and perform post layout simulations, compare the results with pre-Layout simulations. Record the observations.
10.	a) Construct the schematic of two-stage operational amplifier and measure the following: i. Unity gain Band width ii. dB Band width iii. Gain Margin and phase margin with and without coupling capacitance iv. Use the op-amp in the inverting and non-inverting configuration and verify its functionality. v. StudytheUGB,3d B band width , gain and power requirement in op-amp by varying the stage wise transistor geometries and record the observations. b) Draw layout of two-stage operational amplifier with minimum transistor width setto 300 (in 180/90/45 nm technology),choose appropriate transistor geometries as per the results obtained inparta.Useoptimumlayoutmethods.VerifyforDRCandLVS,extractparasiticandperform post layout simulations, compare the results with pre-layout simulations and perform the comparative analysis.
	Demonstration Experiments (For CIE)
11.	UART • Write Verilog description • Verify the Functionality using Test-bench • Synthesizethedesigntargetingsuitablelibraryandbysettingareaandtimingconstraints TabulatetheArea,PowerandDelayfortheSynthesizednetlist,IdentifyCriticalpath.
12.	Designandcharacterize6TbinarySRAMcellandmeasurethefollowing: • Read Time, Write Time, SNM, Power • Draw Layout of 6 TSRAM, use optimum layout methods. Verify for DRC & LVS, extract Parasitic and perform post layout simulations, compare the results with pre-layout simulations. Record the observations.

5.0 Relevance to future subjects

SL. No	Semester	Subject	Topics
01	VIII	Project work	VLSI based projects
02	Higher	VLSI era	Exposure to the VLSI flow and different types of design.

6.0 Relevance to Real World

SL.No	Real World Mapping
01	VLSI design
02	Miniaturization of different designs to provide more flexibility for the designers

7.0 Gap Analysis and Mitigation

SL. No	Delivery Type	Details
02	NPTEL	VLSI design methods

8.0 Books Used and Recommended to Students

Text Books
1.**"**Basic VLSI Design" by Douglas A. Pucknell and Kamran Eshaghian 2. "CMOS VLSI Design"- A Circuits and Systems Perspective**"**- Neil H.E. Weste,David Harris, Ayan Banerjee, 3rd Edition, Pearson Education. 3."FPGA Based System Design"-Wayne Wolf, Pearson Education, 2004,Technology and Engineering

9.0 Relevant Websites (Reputed Universities and Others) for Notes /Animation / Videos Recommended

Website and Internet Contents References
1) https://vtu.ac.in 2) http://www.bookspar.com/engineering-vtu 3) http://www.slideshare.net/farohalolya/8086-microprocessor-lab-manual 4) https://www.youtube.com/results?search_query=microprocessor

10.0 Magazines/Journals Used and Recommended to Students

Sl.No	Magazines/Journals	website
1	IEEE	http://ieeexplore.ieee.org/Xplore/home.jsp
2	PC World	http://www.pcworld.com/article/146957/components/article.html

11.0 Examination Note

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE)is50%.The minimum passing mark for theCIEis40%ofthemaximummarks(20marks).Astudent shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

Continuous Internal Evaluation(CIE):

CIEmarksforthepracticalcourseis**50Marks**.

The split-up of CIE marks for record/journalandtestareintheratio**60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubricsfortheevaluationofthejournal/write-upforhardware/softwareexperimentsdesignedby the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Totalmarksscoredbythestudentsarescaleddownedto30marks(60%ofmaximummarks).
- Weightagetobegivenforneatnessandsubmissionofrecord/write-upontime.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8thweekofthesemesterandthesecondtestshallbeconductedafterthe14thweek of the semester.
- In each test , test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- Thesuitablerubricscanbedesignedtoevaluateeachstudent'sperformanceandlearning ability. Rubrics suggested in Annexure-II of Regulation book
- Theaverageof02testsisscaleddownto **20marks**(40%ofthemaximummarks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two testsis the total CIE marks scored by the student.

Semester End Evaluation(SEE):

SEEmarksforthepracticalcourseis50Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script tobe strictly adhered to by the examiners. **OR**

Based on the course requirement evaluation rubrics shall be done.

12.0 Course Delivery Plan

Sl. No.	Experiments
1.	Designa4-BitAdder • Write a Verilog description • Verify the Functionality using Test-bench • Synthesize the design by setting proper constraints and generate the gate level netlist. From the report generated identify Critical path, Maximum delay, Total number of cells, Power requirement and Total area required
2.	4-BitShiftandaddMultiplier • Write Verilog Code • Verify the Functionality using Test-bench • Synthesize the design by setting proper constraints and obtain the gate level netlist. From the report generated identify Critical path, Maximum delay, Total number of cells, Power requirement and Total area required
3.	32-BitALUSupporting4-Logicaland4-Arithmetic operations, using case and if statement for ALU Behavioral Modeling • Write Verilog description • Verify functionality using Test-bench • Synthesize the design targeting suitable library and by setting area and timing constraints • Tabulate the Area, Power and Delay for the Synthesized netlist • Identify Critical path
4.	Flip-Flops (D,SR and JK) • Write the Verilog description • Verify the Functionality using Test-bench • Synthesize the design by setting proper constraints and obtain the gate level netlist. From the report gate level netlist identify Critical path, Maximum delay, Total number of cells, Power requirement and Total area required. • Verify the functionality using Gate level netlist and compare the results at RTL and gate level netlist.
5.	Four bit Synchronous MOD-N counter with Asynchronous reset • Write Verilog Code • Verify functionality using Test-bench • Synthesizethedesigntargetingsuitablelibraryandbysettingareaandtimingconstraints • Tabulate the Area ,Power and Delay for the Synthesized netlist Identify Critical path
6.	b) Construct the schematic of CMOS inverter with load capacitance of 0.1pF and set the widths of inverter with Wn=Wp,Wn =2Wp,Wn= Wp/2andlengthatselected technology. Carry out the following: i. Set the input signal to a pulse with rise time, fall time of1nsandpulsewidthof10ns andthetimeperiodof20nsandplottheinputvoltageandoutputvoltageofdesigned inverter? ii. From the simulation result compute tp HL, tpLH and td for all three geometrical settings of width? iii. Tabulate the results of delay and find the best geometry for minimum delay for CMOS inverter. out of inverter with Wp/Wn = 40/20, use optimum layout methods. Verify for DRC andLVS,extractparasiticandperformpostlayoutsimulations,compareitheresults with pre layout simulations and compare the results.
7.	Capture the schematic of2-input CMOS NORgate having similar delay as thatof CMOS inverter computed in experiment above. Verify the functionality of NOR gate and also find out the delay td for all four possible combinations of input vectors. Table the results. Increase thedrivestrengthto2Xand4Xandtabulatetheresults.
8.	Construct the schematic of the Boolean Expression $Y=\overline{AB+CD}+E$usingCMOSLogic.Verifythefunctionalityoftheexpressionfind out the delay td for some combination of input vectors. Tabulate the results.

9.	c) Construct the schematic of Common Source Amplifier with PMOS Current Mirror Load and find its transient response and d) AC response? Measure the Unit Gain Band width(UGB), amplification factorby varying transistor geometries, study the impact of variation in width to UGB. e) Draw Lay out of common source amplifier ,use optimum layout methods. Verify for D RC & LVS , extract parasitic and perform post layout simulations ,compare the results with pre-Layout simulations. Record the observations.
10.	a) Construct theschematicoftwo-stageoperationalamplifierandmeasurethefollowing: i. Unity gain Bandwidth. dB Band width iii. Gain Margin and phase margin with and without coupling capacitance iv. Use the op-amp in the inverting and non-inverting configuration and verify its functionality. v. Study the UGB,3dBbandwidth, gain and power requirement in op-amp by varying the stage wise transistor geometries and record the observations. b) Draw layout of two-stage operational amplifier with minimum transistor width set-to 300 (in 180/90/45 nm technology), choose appropriate transistor geometries as per the results obtained inparta. Use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations and perform the comparative analysis.
	Demonstration Experiments(ForCIE)
11.	UART • Write Verilog description • Verify the Functionality using Test-bench • Synthesize the design targeting suitable library and by setting area and timing constraints Tabulate the Area, Power and Delay for the Synthesized netlist, Identify Critical path.
12.	Design and characterize 6 T binary SRAM cell and measure the following: • Read Time, Write Time, SNM, Power • Draw Layout of 6T SRAM, use optimum lay out methods. Verify for DRC & LVS, extract Parasitic and perform post layout simulations, compare the results with pre-layout simulations. Record the observations.

13.0 VIVA BANK

1. The minimum voltage to keep the MOS transistor in on state is known as. 'Pinch off of the channel takes place in which region.
3. Which of 'the following equation is true for liner region?
a)Vds<Vgs -Vt b) Ids>Vgs - Vt c) Vds = Vgs - Vt d) None
4. The oxide layer used in the MOS fabrication is
5. Which of the following Well process is superior?
a) P-well b)N-well c) Both P-well and N-well d) None
6. What is the advantage of CMOS technology?
7. Transit time is given by----------
8. When the VTC of the CMOS inverter shifts towards left,
9. The demarcation line has to be drawn in----------stick diagram.
10. If the value of lambda is 1micrometer then the minimum feature size o the transistor is ?
11. The scaling factor for the Gate Capacitance Cg is given by
12. The scaling factor for power-speed product is given by
13. If the gate voltage and the input voltage of the NMOS transistor is 5V and threshold voltage of the transistor is O. 7V, then the output voltage
14. The mobility of the electrons is---------- than the holes.
15. As the width of the transistor increases the number of contact cuts----------
16. Transmission gate is----------
17. The CMOS schematic diagram of NAND gate consists of----------
18. If the size of the transistors in an inverter increases, then the input capacitance
19. The minimum value of the scaling factor in a cascaded inverter circuit to drive large capacitive load
20. In a lambda-based rules, the distance between two MI layers is
21. Match the following;

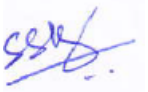
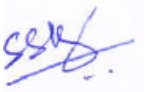
A	B
a) CMOS technology	i) Strong '0'
b) Bipolar technology	ii) Strong' 1’
c) Transmission gate	iii) High input impedance
d) PMOS transistor	iv) Low input impedance
e) NMOS transistor	v) Bi-directional switch

22. What is rise time & fall time of Inverter.
23. Define Symmetrical inverter.
24. What is the value of e in case of load handling by inverter.

25. What is Pass transistor?
26. Give the disadvantage of Pass transistor.
27 What is the advantage of Transmission gate over Pass transistor.
28. What is a Flip-flop?
29. What is a master slave Flip-flop?
30. What is a race-around condition?
31. What is RC extraction?
32. What is Back annotation?
33. What do you mean by DC-analysis?
34. What do you mean by AC-analysis?
35. What is the Gain of common drain amplifier?
36. How the common source amplifier is formed.
37. What is speed Vs area tradeoff?
38. What is DRC & ERC.
39. Differentiate Serial & Parallel adder.
32. Explain booth multiplier

14.0 University Result

Examination	FCD	FC	SC	% Passing
New Course				

Prepared by	Checked by		
			
Prof. S.S.Kamate	**Prof. S. S.Kamate**	**HOD**	**Principal**

Subject Title	**IoT (Internet of Things) Lab**		
Subject Code	BEC657C	**CIE Marks**	50
Number of Lecture Hrs/Week / RBT Level	02 Hours Laboratory L1, L2, L3	**SEE Marks** **Exam Hours**	50 03
CREDITS – 01			

FACULTY DETAILS:		
Name: Prof. D M Kumbhar	**Designation:** Assistant Professor	**Experience :Teach- 17**years (Ind 07years)
No. of times course taught: 02	**Specialization:** Digital Electronics	

1.0 Prerequisite Subjects:

Sl. No	Branch	Semester	Subject
01	ECE	I	C programming
02	ECE	III	Basic electrical & electronics
03	ECE	III	Transducers

2.0 Course Objectives

This laboratory course enables students to

- To impart necessary and practical knowledge of components of Internet of Things.
- To develop skills required to build real-life IoT based projects.

3.0 Course Outcomes

Having successfully completed this course, the student will be able to

	Course Outcome	Cognitive Level	PO's
CO326.1	Explain the Internet of Things and its hardware and software components.	U	1,2,3,4,5,6,7,8,9,10,11,12
CO326.2	Interface I/O devices, sensors & communication modules	U	1,2,3,4,5,6,7,8,9,10,11,12
CO326.3	Remotely monitor data and control devices	U	1,2,3,4,5,6,7,8,9,10,11,12
CO326.4	Develop real life IoT based projects	U	1,2,3,4,5,6,7,8,9,10,11,12
Total Hours of instruction		**40**	

4.0 Course Content

Laboratory Experiments:

1	i) To interface LED/Buzzer with Arduino/Raspberry Pi and write a program to 'turn ON' LED for 1 sec after every 2 seconds. ii) ii) To interface Push button/Digital sensor (IR/LDR) with Arduino/Raspberry Pi and write a program to 'turn ON' LED when push button is pressed or at sensor detection.
2	i) To interface DHT11 sensor with Arduino/Raspberry Pi and write a program to print temperature and humidity readings. ii) ii) To interface OLED with Arduino/Raspberry Pi and write a program to print temperature and humidity readings on it.
3	To interface motor using relay with Arduino/Raspberry Pi and write a program to 'turn ON' motor when push button is pressed
4	i) Write an Arduino/Raspberry Pi program to interface the Soil Moisture Sensor.

	ii) Write an Arduino/Raspberry Pi program to interface the LDR/Photo Sensor.

5	Write a program to interface an Ultrasonic Sensor with Arduino /Raspberry Pi.
6	Write a program on Arduino/Raspberry Pi to upload temperature and humidity data to thing speak cloud.
7	Write a program on Arduino/Raspbeii y Pi to retrieve temperature and humidity data from thing speak cloud.
8	Write a program to interface LED using Telegram App.
9	Write a program on Arduino/Raspbeii y Pi to publish temperature data to the MQTT broker.
10	Write a program to create a UDP server on Arduino/Raspberry Pi and respond with humidity data to the UDP client when requested.
11	Write a program to create a TCP server on Arduino /Raspberry Pi and respond with humidity data to the TCP client when requested.
12	Write a program on Arduino / Raspberry Pi to subscribe to the MQTT broker for temperature data and print it.

5.0 Relevance to future subjects

Sl. No	Semester	Subject	Topics
01	VII/VIII	Project work	All experiments

6.0 Relevance to real world

SL No	Real World Mapping
01	Control of various devices using Iot e.g. Motor, Fan Control

7.0 Gap Analysis and Mitigation

Sl. No	Delivery Type	Details
01	Tutorial	Topic: Simulation software like Arduino IDE.
02	NPTEL	IoT appliance control

8.0 Books Used and Recommended to Students

Text Books

1. Vijay Madisetti, Arshdeep Bahga, Internet of Things. "A Hands on Approach", University Press
2. Dr. SRN Reddy, Rachit Thukral and Manasi Mishra, "Introduction to Internet of Things: A practical Approach", ETI Labs
3. Pethuru Raj and Anupama C Raman, "The Internet of Things: Enabling Technologies, Platforms, and Use Cases", CRC Press
4. Jeeva Jose, "Internet of Things", Khanna Publishing House, Delhi
5. Adrian McEwen, "Designing the Internet of Things", Wiley
6. Raj Kamal, "Internet of Things: Architecture and Design", McGraw Hill

9.0 Relevant Websites (Reputed Universities and Others) for Notes/Animation/Videos Recommended

Website and Internet Contents References

3) https://nptel.co.in
4) https://robocraze.com/blogs/post
5) https://www.geeksforgeeks.org

6) https://lastminuteengineers.com

10.0 Magazines/Journals Used and Recommended to Students

Sl.No	Magazines/Journals	website
1	IEEE Xplorer	http://ieee.com
2	International Journal of Science and Technology	http://www.sciencedirect.com/science/journal/00207683
3	Journal of Communication Engineering	http://ieee.com

11.0 Examination Note

CIE marks for the practical course are **50 Marks.**

The split-up of CIE marks for record/ journal and test are in the ratio **60:40.**

- Each experiment will be evaluated for conduction with an observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments are designed by the faculty who is handling the laboratory session and are made known to students at the beginning of the practical session.
- The record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- The total marks scored by the students are scaled down to **30 marks** (60% of maximum marks).
- Weightage is to be given for neatness and submission of record/write-up on time.
- The department shall conduct a test of 100 marks after the completion of all the experiments listed in the syllabus.
- In a test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.
- The marks scored shall be scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and marks of a test is the total CIE marks scored by the student.

- Semester End Evaluation (SEE): SEE marks for the practical course is 50 Marks.
- SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University
- All laboratory experiments are to be included for practical examination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. OR based on the course requirement evaluation rubrics shall be decided jointly by examiners.
- Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.
- Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.
- General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks.
- SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)
- Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.
- The duration of SEE is 03 hours

12.0 Course Delivery Plan

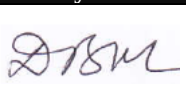
Experiment	Lecture No.	Content	% of Portion
1	1	i) To interface LED/Buzzer with Arduino/Raspberry Pi and write a program to 'turn ON' LED for 1 sec after every 2 seconds. ii) To interface Push button/Digital sensor (IR/LDR) with Arduino/Raspberry Pi and write a program to 'turn ON' LED when push button is pressed or at sensor detection.	7
2	2	i) To interface DHT11 sensor with Arduino/Raspberry Pi and write a program to print temperature and humidity readings. ii) To interface OLED with Arduino/Raspberry Pi and write a program to print temperature and humidity readings on it.	14
3	3	To interface motor using relay with Arduino/Raspberry Pi and write a program to 'turn ON' motor when push button is pressed	21
4	4	i) Write an Arduino/Raspberry Pi program to interface the Soil Moisture Sensor. ii) Write an Arduino/Raspberry Pi program to interface the LDR/Photo Sensor.	29
5	5	Write a program to interface an Ultrasonic Sensor with Arduino /Raspberry Pi.	36
6	6	Write a program on Arduino/Raspberry Pi to upload temperature and humidity data to thingspeak cloud.	43
7	7	Write a program on Arduino/Raspbeii y Pi to retrieve temperature and humidity data from thingspeak cloud.	50
8	8	Write a program to interface LED using Telegram App.	64
9	9	Write a program on Arduino/Raspbeii y Pi to publish temperature data to the MQTT broker.	72
10	10	Write a program to create a UDP server on Arduino/Raspberry Pi and respond with humidity data to the UDP client when requested.	86
11	11	Write a program to create a TCP server on Arduino /Raspberry Pi and respond with humidity data to the TCP client when requested.	93
12	12	Write a program on Arduino / Raspberry Pi to subscribe to the MQTT broker for temperature data and print it.	100

13.0 VIVA BANK

1. What is IoT? / What is the Internet of Things?
2. What are the most important characteristics or features of IoT?
3. How does the IoT (Internet of Things) affect our everyday lives?
4. What industries can be benefitted from IoT?
5. What are the different types of components used in IoT?
6. What is Raspberry Pi?
7. What are the key advantages of IoT?
8. What are the different types of sensors used in IoT?
9. What is PWM or Pulse Width Modulation?
10. What is Arduino used in IoT?
11. What are the different types of communication models used in IoT?
12. What is the basic difference between an IoT device and a normal sensor device?
13. What are the various wireless communications boards available in Raspberry Pi?
14. What functions are used to read analog and digital data from a sensor in Arduino?
15. What are the different available models in Raspberry Pi used in IoT?
16. Define Arduino
17. List mostly used sensors types in IoT
18. Mention applications of PWM in IoT
19. What are the functions used to read analog and digital data from a sensor in Arduino?
20. What is Bluetooth Low Energy?
21. Define MicroPython
22. Differentiate between Arduino and Raspberry pi
23. List available models in Raspberry Pi

13.0 University Result

NEW SCHME

Prepared by	Checked by		
			
Prof. D. M. Kumbhar	**Prof. D. B. Madihalli**	**HOD**	**Principal**

Subject Title	**INDIAN KNOWLE DGE SYSTEMS**		
Subject Code	BIK609	**CIE Marks**	100
Number of Lecture Hrs / Week	01 L	**SEE Marks**	---
Total Number of Lecture Hrs	15	**Sem. End Exam Hours**	---

FACULTY DETAILS:		
Name: Prof. S. S. Kamate	**Designation:** Asst. Professor	**Experience:21** yrs
No. of times course taught:01	**Specialization:** Digital Electronics	

1.0 Prerequisite Subjects:

Sl. No	**Branch**	**Semester**	**Subject**
01	--		--

2.0 Course Objectives

1. To facilitate the students with the concepts of Indian traditional knowledge and to make them understand the Importance of roots of knowledge system.
2. To make the students understand the traditional knowledge and analyze it and apply it to their day-to-day life.

3.0 Course Outcomes

Having successfully completed this course, the student will be able to draw and analyze.

	Course Outcome	**Cognitive Level**	**POs**
C329.1	Provide an overview of the concept of the Indian Knowledge System and its importance.	U	PO1, PO8,
C329.2	Appreciate the need and importance of protecting traditional knowledge.	U	PO6
C329.3	Recognize the relevance of Traditional knowledge in different domains.	U	PO3, PO4,
C329.4	Establish the significance of Indian Knowledge systems in the contemporary world.	U	PO6, PO7
Total Hours of instruction		**50**	

4.0 Course Content

Course Content:

Module	Teaching Hours	Bloom's Taxonomy (RBT) level
Module 1: Overview, Vedic Corpus, Philosophy, Character scope and importance, traditional knowledge vis-a-vis indigenous knowledge, traditional knowledge vs. western knowledge.	**8 Hours**	**L1, L2**
Module 2: **Traditional Knowledge in Humanities and Sciences**: Lingistics, Number and measurements - Mathematics, Chemistry, Physics, Art, Astronomy, Astrology, Crafts and Trade in India and Engineering and Technology..	**8 Hours**	**L1,L2,L3**
Module 3: **Traditional Knowledge in Professional domain:** Town planning and architecture- Construction, Health, wellness and Psychology- Medicine, Agriculture, Governance and public administration, United Nations Sustainable development goals.	**8 Hours**	**L1,L2,L3**

5.0 Relevance to future subjects

Sl No	Semester	Subject	Topics
01	VII	VLSI Lab	VLSI Design of Circuits
02	VIII	Projects on VLSI	Projects and Research

6.0 Relevance to Real World

SL. No	Real World Mapping
01	Concept of the Indian Knowledge System and its importance
02	Establish the significance of Indian Knowledge systems in the contemporary world

7.0 Gap Analysis and Mitigation

Sl. No	Delivery Type	Details
01	---	----

8.0 Books Used and Recommended to Students

Text Books
Introduction to Indian Knowledge System-concepts and applications, B Mahadevan, Vinayak Rajat Bhat, Nagendra Pavana R N, 2022, PHI Learning Private Ltd, ISBN-978-93-91818-21-0
Traditional Knowledge System in India, Amit Jha, 2009, Atlantic Publishers and Distributors (P)Ltd., ISBN-13:978-8126912230,
Knowledge Traditions and Practices of India,Kapil Kapoor,Avadesh Kumar Singh,Vol. 1, 2005, DK Print World(P)Ltd., ISBN 81-246-0334,
Additional Study material & e-Books
4. VTU on line notes.

9.0 Relevant Websites (Reputed Universities and Others) for Notes/Animation/Videos Recommended

Website and Internet Contents References
https://www.youtube.com/watch?v=LZP1StpYEPM
http://nptel.ac.in/courses/121106003/
http://www.iitkgp.ac.in/department/KS;jsessionid=C5042785F727F6EB46CBF432D7683B63(Centre of Excellence for Indian Knowledge System, IIT Kharagpur)
https://www.wipo.int/pressroom/en/briefs/tk_ip.html
https://unctad.org/system/files/official-document/ditcted10_en.pdf
http://nbaindia.org/uploaded/docs/traditionalknowledge_190707.pdf
https://unfoundation.org/what-we-do/issues/sustainable-development-goals/?gclid=EAIaIQobChMInp-Jtb_p8gIVTeN3Ch27LAmPEAAYASAAEgIm1vD_BwE

10.0 Magazines/Journals Used and Recommended to Students

Sl. No	Magazines/Journals	website
1	International Jounal Bharatiya Knowledge System	https://www.vbuss.org/international-journal-bharatiya-knowledge-system
2	Indian Journal of Traditional Journal	https://or.niscpr.res.in/index.php/IJTK
3		

11.0 Examination Note

Internal Assessment: 100 Marks
Two Internal Assessment Tests will be conducted, each for 25 Marks and the sum of two will be reduced to 40 Marks.

SCHEME OF EXAMINATION:
Two questions to be set from the syllabus covered.
Student has to answer one part each from each question.
Question 1 or 2 1x12.5 = 12.5Marks
Question 3 or 4 1x12.5 = 12.5Marks
Total = 25Marks

INSTRUCTION FOR INTERNAL ASSESSMENT TEST

- Four full questions will be given which consists of a,bsub sections.
- Students have to answer either Q :1 or 2 and Q 3 or 4 completely.

ASSESSMENT AND EVALUATION PATTERN	
WEIGHTAGE	**100%(CIE)**
QUIZZES	
Quiz-I	Each quiz is evaluated for 10marks adding up To **20Marks.**
Quiz-II	
THEORY COURSE-(Bloom's Taxonomy Levels: Remembering, Understanding, Applying, Analyzing, Evaluating, and Creating)	
Test–I	Each test will be conducted for 25 Marks adding upto 50 marks. Final test marks will be reduced to **40 Marks**
Test–II	

EXPERIENTIAL LEARNING	**40**
Case Study-based Teaching-Learning	--
Sector wise study & consolidation (viz., Engg. Semiconductor Design, Healthcare & Pharmaceutical, FMCG, Automobile, Aerospace and IT/ ITeS)	--
Video based seminar(4-5minutesper student)	--
Maximum Marks for the Theory	---
Practical	--
Total Marks for the Course	**100**

12.0 Course Delivery Plan

Course Delivery Plan:

MODULE	LECTURE NO.	CONTENT OF LECTURE	% OF PORTION
1	1	Overview	20
	2	Vedic Corpus, Philosophy	
	3	Character scope and importance traditional knowledge vis-a-vis	
	4	indigenous knowledge, traditional knowledge vs. western knowledge	
2	5	Lingistics	
	6	Number and measurements	
	7	Chemistry, Physics	
	8	Art, Astronomy	
	9	Astrology, Crafts	
	10	Trade in India and Engineering and Technology	
3	11	Town planning and architecture-.	60
	12	Construction, Health, wellness and Psychology	
	13	Medicine, Agriculture	
	14	Governance and public	
	15	administration, United Nations Sustainable	
	16	development goals	

13.0 Assignments, Pop Quiz, Mini Project, Seminars

14.0 QUESTION BANK

MODULE -1

MCQs, Definition, True/False, Fill in the blanks (1 Marks Each)

1) Which branch of Vedic knowledge focuses on the grammatical structure of the Vedic language?
A) Siksa
B) Vyakarana
C) Chandas
D) Nirukta

2)What are the six parts of knowledge called, which are like branches of learning and are linked to the Vedas?
A) Vedantas

B) Veda-shastras
C) Vedangas
D) Vedic sciences

3) What are the Vedangas?
A) Six ancient astronomical texts
B) Six branches of learning linked to the Vedas
C) Six types of celestial bodies
D) Six mathematical methods used in astronomy

4) What was the primary purpose of the Vedangajyotisa?
A) Predicting solar eclipses B) Calculating the positions of planets
C) Determining the right times for rituals
D) Exploring the lunar calendar
5) What was the primary purpose of the Gavamayana sacrificial ritual mentioned in the text?
A) Observing the Sun's and Moon's movements
B) Predicting solar eclipses
C) Measuring the Earth's circumference
D) Studying planetary motion
6) In the Yajurveda, how many solar months and seasons did they recognize in a year?
A) 10 solar months and 4 seasons
B) 8 solar months and 5 seasons
C) 6 solar months and 3 seasons
D)12 solar months and 6 seasons
7) Which chapter of a typical Siddhantic text addresses the computation of lunar and solar eclipses?
A) Madhyama Adhikara
B) Triprasna Adhikara
C)Chandra and Surya-Grahan Adhikara
D) Spasta Adhikara

8) Who is credited with proposing a heliocentric model of the solar system that predates Copernicus?
A) Aryabhata I B) Bhaskara II
C) Nilakantha Somayaji
D) Varahamihira
9) Which Indian mathematician and astronomer is known for his book "Aryabhatiyam"?
A) Bhaskara I
B) Brahmagupta
C) Varahamihira
D**) Aryabhata I**

10) In Aryabhatiyam, which part of the book discusses trigonometric tables for 'Sine'?
A) Gitika
B) Ganita
C) Kalakriya
D) Gola

11)Which correction is applicable to the non-circular nature of planetary orbits in Siddhantic astronomy?
A) Sighra correction
B) Manda correction
C) Bija Samskara correction
D) Parallax correction

12) What were the two other types of texts mentioned in the text besides the siddhantas?
A) Tantras and Karanas
B) Vedas and Puranas
C) Upanishads and Sutras
D) Bhagavad Gita and Ramayana

13) What is the term for the type of texts that provide practical methods for astronomy using recent dates and smaller numbers?
A) Tantras

B) Karanas
C) Siddhantas
D) Vedangas

14) Who is known for his book "Khandakhadyaka" and made practical astronomical calculations?
A) Aryabhata I
B) Bhaskara II
C) Brahmagupta
D) Varahamihira

15) Who is the author of "Tantrasangraha," one of the Tantra texts mentioned in the text?
A) Aryabhata I
B) Nilakantha Somayaji
C) Bhaskara II
D) Ganesa Daivajna

16) In the context of Indian astronomy, what does the term "Ahargana" refer to? A) The number of solar months in a year
B) The number of lunar phases in a year C) The number of constellations in the zodiac
D) The number of civil days from a specific epoch

17) What was the primary purpose of the "Triprasna Adhikara" chapter in Siddhantic texts?
A) Studying planetary motion
B) Determining latitude and longitude
C) Addressing three fundamental questions of direction, place and time
D) Calculating lunar phases

18) Which correction is applicable to the non-circular nature of planetary orbits in Siddhantic astronomy?
A) Sighra correction
B) Manda correction
C) Bija Samskara correction
D) Parallax correction

19) Who authored "Mahabhaskariyam" and "Laghubhaskariyam"?
A) Bhaskara I
B) Aryabhata I
C) Bhaskara II
D) Brahmagupta

20) Who authored "Mahabhaskariyam" and "Laghubhaskariyam"?
A) Bhaskara I
B) Aryabhata I
C) Bhaskara II
D) Brahmagupta

21) Which of the following celestial bodies is NOT mentioned as one of the tara grahas in the text?
A) Mercury
B) Venus
C) Mars
D) Neptune

22) In Indian astronomy, what is the significance of the concept of "Madhyama Adhikara"?
A) It deals with lunar eclipses.
B) It focuses on the equinoxes.
C) It calculates mean positions of celestial bodies
D) It discusses the heliocentric model

23) Which astronomical system did Varahamihira consider the best in his book "Panchasiddhantika"?
A) Aryasiddhanta
B) Vasisthasiddhanta
C)Suryasiddhanta
D) Romakasiddhanta

Descriptive questions: (5 Marks Each)

1)Briefly introduce Indian Astronomy and Ancient Indian Astronomy.
2)Discuss the significance of the Vedangajyotisa and its two versions (Rgveda Jyotisa and Yajurveda Jyotisa). What were the key purposes of this ancient text?
3)What is the "yuga" concept in Indian astronomy, and how was it used to measure time and track seasonal changes within the Indian calendar system? Explain the role of nakshatras and provide an example from the Rgveda.
4)Explain the useful classification of Vedangjyotisa.
5)Write a short note on Siddhanta.
6)Who wrote the book "Aryabhatiyam"? Describe it's all part in detail.
7)Analyze the significant contributions of Aryabhata I to mathematics and astronomy. How didhis work impact subsequent developments in Indian astronomy?
8)Name the text other than the siddhanta and explain each of them.
9)Write name of any 10 Indian Astronomers and their composition of work.
10) Explain in brief about the contents of the Siddhanta.11)Write a short note on continuity in Astronomical tradition.

15.0 University Result

Examination	FCD	FC	SC	% Passing
New Subject				

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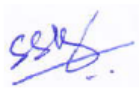	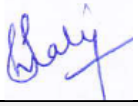		
Prof. S. S. KAMATE	Prof. S.S.Malaj	HOD	Principal