INSTITUTE VISION

"To be a preferred institution in Engineering Education by achieving excellence in teaching and research and to remain as a source of pride for its commitment to holistic development of individual and society"

INSTITUTE MISSION

"To continuously strive for the overall development of students, educating them in a state of the art infrastructure, by retaining the best practices, people and inspire them to imbibe real time problem solving skills, leadership qualities, human values and societal commitments, so that they emerge as competent professionals"

DEPARTMENTAL VISION

"To be the centre of excellence in providing education in the field of Electronics and Communication Engineering to produce technically competent and socially responsible engineering graduates."

DEPARTMENTAL MISSION

"Educating students to prepare them for professional competencies in the broader areas of the Electronics and Communication Engineering field by inculcating analytical skills, research abilities and encouraging culture of continuous learning for solving real time problems using modern tool".

PROGRAM EDUCATIONAL OBJECTIVES (PEOs):

PEO1:

Acquire core competence in Applied Science, Mathematics, and Electronics and Communication Engineering fundamentals to excel in professional carrier and higher study.

PEO2:

Design, Demonstrate and Analyze the Electronic Systems which are useful to society.

PEO3:

Maintain Professional and Ethical values, Employability skills, Multidisciplinary approach and an Ability to realize Engineering issues to broader social contest by engaging in lifelong learning.

PROGRAM SPECIFIC OUTCOMES(PSOS)

The graduates will be able to:

PSO1:

An ability to understand the concepts of Basic Electronics and Communication Engineering and to apply them to various areas like Signal Processing, VLSI, Embedded Systems, Communication Systems and Digital & Analog Devices

PSO2:

An ability to solve complex Electronics and Communication Engineering problems, using latest hardware and software tools, along with analytical skills to arrive at cost effective and appropriate solutions

PROGRAM OUTCOMES(POs):

1. **Engineering knowledge**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

2. **Problem analysis**: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

3. **Design/development of solutions**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

4. **Conduct investigations of complex problems**: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

5. **Modern tool usage**: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

6. **The engineer and society**: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

7. **Environment and sustainability**: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainble development.

8. **Ethics**: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

9. **Individual and team work**: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

10. **Communication**: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

11. **Project management and finance**: Demonstrate knowledge and understanding of the engineering and mangement principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

12. **Life-long learning**: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

STUDENT HELP DESK

Sr.No	Name of the faculty	Activities
1	Dr.M.C.Sarasamba	GATE / Preplacement Coaching
		Students Mentor
		Module Coordinator
		Research Center Coordinator
		Dept. NAAC Criteria Sub Coordinator
		NBA Criteria Coordinator
2	Prof. S. S. Malaj	GATE / Preplacement Coaching
		Adv.Comm. Lab In charge
		Students Mentor
		Dept. NAAC Criteria Sub Coordinator
		NBA Criteria Coordinator
		NIRF Coordinator
3	Prof. S. S. Kamate	GATE / Preplacement Coaching
		VLSI Lab In charge
		Students Mentor
		Module Coordinator
		IEEE Coordinator/ IA Cordinator
		Dept. NAAC Criteria Sub Coordinator
		Project Coordinator
		NBA Criteria Coordinator
4	Prof. D. M. Kumbhar	GATE / Preplacement Coaching
		AC Lab In charge
		Students Mentor
		Dept. Association Coordinator
		Class Teacher
		IIIC Coordinator
		Dept. NAAC Criteria Sub Coordinator
		NBA Criteria Coordinator
		AICTE Activity Coordinator
		Dept. ED Cell Coordinator

Sr.No	Name of the faculty	Activities
5	Prof. S. S. Patil	GATE / Preplacement Coaching
		ARM & ES Lab In charge
		Students Mentor
		Class Teacher
		NBA Criteria Coordinator
		AICTE Activity Coordinator
		Admission Coordinator
		Module Coordinator
6	Prof. D. B. Madihalli	GATE / Preplacement Coaching
		DSD Lab In charge
		Students Mentor
		NBA Coordinator
		News & Publicity Coordinator
		NBA Criteria Coordinator
		Website Coordinator
		VTU LIC Coordinator
7	Prof. P. V. Patil	GATE / Preplacement Coaching
		HDL Lab In charge
		Students Mentor
		NBA Criteria Coordinator
		T&P Cell Coordinator
		Alumni Coordinator
8	Dr. S. S. Ittannavar	GATE / Preplacement Coaching
		BSP /DSP Lab In charge
		Students Mentor
		Module Coordinator
		News Letter / Technical Magazine
		AICTE Coordinator
9	Prof. B. P. Khot	GATE / Preplacement Coaching
		CN/MC Lab In charge
		Students Mentor
		Dept. Time Table Coordinator & Meeting Coordinator
		Class Teacher
		NBA Criteria Coordinator
		Dept T&P Cell Coordinator
		AICTE Activity Coordinator
10	Prof. S.R.Mallurmath	EMS Coordinator
		GATE / Preplacement Coaching
		Students Mentor
		AICTE Activity Coordinator
		NBA Criteria Coordinator
11	Prof. K.S.Patil	GATE / Preplacement Coaching
		Students Mentor
		AICTE Activity Coordinator
		NBA Criteria Coordinator

CONTENTS

Sl. No	TOPIC	PAGE NO.
1	Institute Vision & Mission	1
2	Department Mission, PEO's & PO's	2,3
3	Student Help Desk	4,5
4	Contents	6
5	Departmental Resources	7
6	Faculty Details Technical Supporting Staff	
7	Scheme of Teaching And Examination	8
8	Academic Calendar	9
9	**Theory – Course Plans** **18EC71**-Computer Networks **18EC72**-VLSI Design **Professional Elective – 2** **18EC731**-Real Time systems **Professional Elective – 3** **18EC743**-Multi Media Communication **Open Elective –B** **18ME751**-Energy and Environment **18ECL76**-Computer Networks Lab **18ECL77**-VLSI Laboratory	10-14 15-20 21-26 27-33\ 34-39 40-43 44-49

FACULTY POSITION

S.N.	Category	No. in position	Average experience
1	Teaching faculty.	09	17.00Y
2	Technical supporting staff.	04	22.08Y
3	Helper staff	02	22.00Y

MAJOR LABORATORIES

S.N.	Name of the laboratory	Area in Sq. Mtrs	Amount Invested in Lakhs	S.N.	Name of the laboratory	Area in Sq. Mtrs	Amount Invested in Lakhs
1	Digital Electronics Lab	71	1.54	5	VLSI Lab	71	35.51
2	Analog Electronics (ED &I) Lab	92	8.24	6	Project Lab	95	--
3	Advanced Commn & Commn + LIC Lab	92	20.50	7	Research/E-Yantra/DSP & C.N.Lab	71	16.49
4	HDL/MC / EMD Lab	71	19.57	8	Power Electronics Lab	--	4.86
Total Investment In The Department					**Rs. 95.31 Lacs**		

FACULTY DETAILS

TEACHING FACULTY

S.N.	Name and Designation	Qualification	Specialization	Professional Membership	Teaching Exp.	Contact No.
1	Prof. M.C.Sarasamba	Ph.D	E&C	LMISTE	18Y.05M	9480714746
2	Assoc.Prof.S .S .Ittannavar	Ph.D	DSP	LMISTE	10Y.05M	9964299498
3	Asst.Prof. S. S. Malaj	M.E.	E & TC	LMISTE	26Y.01M	9731795803
4	Asst.Prof.S.S.Kamate	M.Tech	Digital Electronics	LMISTE	20Y.06M	9008696825
5	Asst.Prof. D.M. Kumbhar	M.Tech	Electronics	LMISTE	19Y.04M	09373609880
6	Asst.Prof. Sachin .S. Patil	M.Tech	VLSI & Embedded	LMISTE	19Y.02M	9448102010
7	Asst.Prof .D.B. Madihalli	M.Tech	Industrial Electronics	LMISTE	16Y.01M	9902854324
8	Asst.Prof.P.V.Patil	M.Tech	VLSI & Embedded	LMISTE	10Y.10M	9731104059
9	Asst.Prof. B. P. Khot	M.Tech	Microelectronics & Control Systems	LMISTE	7Y.05M	9964019501
10	Asst.Prof. S.R.Mallurmath	M.Tech		LMISTE		7259865769
11	Asst.Prof.K.S.Patil	M.Tech	VLSI	LMISTE	29Y.00M	9902682781

TECHNICAL SUPPORTING STAFF

S.N.	Name	Qualification	Experience (in years)
1.	Sri. P. S. Desai	DEC	23Y-.01M
2.	Sri. V. V. Guruwodeyar	DEC	31Y-08 M
3.	Sri.M.A.Attar	DEC	13Y-03M

VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI
Scheme of Teaching and Examination 2018 – 19
Outcome Based Education(OBE) and Choice Based Credit System (CBCS)(Effective from the academic year 2018 – 19)

VII SEMESTER

Sl.No	Course and Course code		Course Title	Teaching Department	Teaching Hours /Week			Examination				
					Theory Lecture	Tutorial	Practical/ Drawing	Duration in hours	CIE Marks	SEE Marks	Total Marks	Credits
					L	T	P					
1	PCC	18EC71	Computer Networks		3	--	--	03	40	60	100	3
2	PCC	18EC72	VLSI Design		3	--	--	03	40	60	100	3
3	PEC	18XX73X	Professional Elective - 2		3	--	--	03	40	60	100	3
4	PEC	18XX74X	Professional Elective - 3		3	--	--	03	40	60	100	3
5	OEC	18XX75X	Open Elective -B		3	--	--	03	40	60	100	3
6	PCC	18ECL76	Computer Networks Lab		--	2	2	03	40	60	100	2
7	PCC	18ECL77	VLSI Laboratory		--	2	2	03	40	60	100	2
8	Project	18ECP78	Project Work Phase - 1		--	--	2	--	100	--	100	1
9	Internship	--	Internship	(If not completed during the vacation of VI and VII semesters, it shall be carried out during the vacation of VII and VIII semesters)								
				TOTAL	15	4	6	21	380	420	800	20

Note: PCC: Professional core, PEC: Professional Elective.

Professional Elective - 2

Course code under 18XX73X	Course Title
18EC731	Real Time System
18EC732	Satellite Communication
18EC733	Digital Image Processing
18EC734	Data Structures using C++
18EC735	DSP Algorithms &Architecture

Professional Electives - 3

Course code under 18XX74X	Course Title
18EC741	IOT & Wireless Sensor Networks
18EC742	Automotive Electronics
18EC743	Multimedia Communication
18EC744	Cryptography
18EC745	Machine Learning

Open Elective –B

(i) 18EC751 Communication Theory   (ii) 18EC752 Neural Networks

Students can select any one of the open electives offered by other Departments except those that are offered by the parent Department (Please refer to the list of open electives under 18XX75X).

Selection of an open elective shall not be allowed if,
- The candidate has studied the same course during the previous semesters of the programme.
- The syllabus content of open elective is similar to that of the Departmental core courses or professional electives.
- A similar course, under any category, is prescribed in the higher semesters of the programme.

Registration to electives shall be documented under the guidance of Programme Coordinator/ Advisor/Mentor.

Project work:
Based on the ability/abilities of the student/s and recommendations of the mentor, a single discipline or a multidisciplinary project can be assigned to an individual student or to a group having not more than 4 students. In extraordinary cases, like the funded projects requiring students from different disciplines, the project student strength can be 5 or 6.

CIE procedure for Project Work Phase - 1:
(i) Single discipline: The CIE marks shall be awarded by a committee consisting of the Head of the concerned Department and two senior faculty members of the Department, one of whom shall be the Guide.
The CIE marks awarded for the project work phase -1, shall be based on the evaluation of the project work phase -1 Report (covering Literature Survey, Problem identification, Objectives and Methodology), project presentation skill and question and answer session in the ratio 50:25:25.The marks awarded for the Project report shall be the same for all the batch mates.
(ii) Interdisciplinary: Continuous Internal Evaluation shall be group wise at the college level with the participation of all guides of the college. Participation of external guide/s, if any, is desirable.
The CIE marks awarded for the project work phase -1, shall be based on the evaluation of project work phase -1 Report, project presentation skill and question and answer session in the ratio 50:25:25.The marks awarded for the project report shall be the same for all the batch mates.

Internship: All the students admitted to III year of BE/B.Tech shall have to undergo mandatory internship of 4 weeks during the vacation of VI and VII semesters and /or VII and VIII semesters. A University examination shall be conducted during VIII semester and the prescribed credit shall be included in VIII semester. Internship shall be considered as a head of passing and shall be considered for the award of degree. Those, who do not take- up/complete the internship shall be declared fail and shall have to complete during subsequent University examination after satisfying the internship requirements.

		IQAC
S J P N Trust's		File I-11
Hirasugar Institute of Technology, Nidasoshi.		AY:2023-24 (Odd)
Approved by AICTE, New Delhi, Permanently Affiliated to VTU, Belagavi Recognized under 2(f) & 12B of UGC Act, 1956 Accredited at 'A' Grade by NAAC & Programmes Accredited by NBA:CSE & ECE		Rev: 01

ACADEMIC CALENDAR OF EVENTS-01 (CoE-01) OF I & VII SEM FOR THE AY: 2023-24

Ref: 1. VTU CoE Notification No.: VTU/BGM/ACA/2023-24/2668, Dated 25th Aug. 2023
        2. HSIT/NDS/HOD-Meeting-23/2022-23, Dated: 20th Sept. 2023

Calendar	Date	Events & Holidays
September -2023	14th Aug.-9th Sept.2023	One Month Internship for VI Semester completed students
	4th -14th Sept. 2023	Commencement of I Semester & 11 days Students Induction Program (SIP)
	11th Sept.2023	Commencement of VII Semester Classes
	15th Sept.2023	Commencement of I Semester Classes
	19th Sept.2023	GH: Varasiddhi Vinayaka Vrata
	21st Sept. 2023	LH: Mahadasoha of Shri Math Nidasoshi
October -2023	28th Sept.2023	GH: Eid-Milad
	2nd Oct. 2023	GH: Gandhi Jayanthi
	19th -21st Oct.2023	1st IA Test
	21st Oct. 2023	1st Feedback on Teaching-Learning (I & VII Sems.)
	23rd -24th Oct. 2023	GH: Mahanavami, Ayudhapooja, Vijayadasami
November -2023	26th Oct. 2023	Display of 1st IA Test Marks
	1st Nov. 2023	GH: Kannada Rajyothsava
	10th -11th Nov. 2023	Lab IA Test-I (2021 & 2022 Scheme)
	14th Nov. 2023	GH: Balipadyami, Deepavali
	23rd -25th Nov. 2023	2nd IA Test
December -2023	25th Nov. 2023	2nd Feedback on Teaching-Learning (I & VII Sems.)
	29th Nov. 2023	Display of 2nd IA Test Marks
	30th Nov. 2023	GH: Kanakadasa Jayanti
	8th-9th Dec. 2023	International Conference
	25th Dec. 2023	GH: Christmas
	1st -3rd Jan. 2024	3rd IA Test
January -2024	5th Jan. 2024	Display of 3rd IA Test Marks
	4th -6th Jan. 2024	Lab IA Test-II (2018, 2021 & 2022 Scheme)
	6th Jan. 2024	Last Working Day of the I & VII Semesters
	8th – 19th Jan. 2024	VTU Practical Exams
	12th Jan. 2024	National Youth Day
February -2024	26th Jan. 2024	Republic Day
	22nd Jan. 2024	Commencement of VTU SEE
	13th Feb.2024	Commencement of II Semester
	19th Feb. 2024	Commencement of VIII Semester

September -2023

Sun	Mon	Tue	Wed	Thu	Fri	Sat
					1	2
3	4	5	6	7	8	9
10	11	12	13	14	15	16
17	18	19	20	21	22	23
24	25	26	27	28	29	30

October -2023

Sun	Mon	Tue	Wed	Thu	Fri	Sat
1	2	3	4	5	6	7
8	9	10	11	12	13	14
15	16	17	18	19	20	21
22	23	24	25	26	27	28
29	30	31				

November -2023

Sun	Mon	Tue	Wed	Thu	Fri	Sat
			1	2	3	4
5	6	7	8	9	10	11
12	13	14	15	16	17	18
19	20	21	22	23	24	25
26	27	28	29	30		

December -2023

Sun	Mon	Tue	Wed	Thu	Fri	Sat
					1	2
3	4	5	6	7	8	9
10	11	12	13	14	15	16
17	18	19	20	21	22	23
24	25	26	27	28	29	30
31						

January -2024

Sun	Mon	Tue	Wed	Thu	Fri	Sat
	1	2	3	4	5	6
7	8	9	10	11	12	13
14	15	16	17	18	19	20
21	22	23	24	25	26	27
28	29	30	31			

February -2024

Sun	Mon	Tue	Wed	Thu	Fri	Sat
				1	2	3
4	5	6	7	8	9	10
11	12	13	14	15	16	17
18	19	20	21	22	23	24
25	26	27	28	29		

GH: General Holiday, LH: Local Holiday

Dr.S.N.Topannavar
IQAC Coordinator & Dean (Academics)

Dr.S.C.Kamate
Principal

22/9/23

Subject Title	COMPUTER NETWORKS		
Subject Code	18EC71	CIE Marks	40
Number of Lecture Hrs/ Week	03	Exam Marks	60
Total Number of Lecture Hrs	40	Exam Hours	03
			CREDITS – 03

FACULTY DETAILS:

Name: Prof. B. P. Khot	Designation: Associate Professor	Experience:7.9Yrs
No. of times course taught: 01		Specialization: Microelectronics and control systems

1.0   Prerequisite Subjects:

Sl. No	Branch	Semester	Subject
01	Electronics & Communication Engineering	V/VI	Digital communication/ Principles of communication systems
02	Electronics & Communication Engineering	III	Digital Electronics

2.0   Course Objectives

1. Understand the layering architecture of OSI reference model and TCP/IP protocol suite.
2. Understand the protocols associated with each layer.
3. Learn the different networking architectures and their representations.
4. Learn the functions and services associated with each layer.

3.0   Course Outcomes

At the end of the course students will be able to:

	Course Outcome	RBT Level	POs
C401.1	Understand the concepts of networking thoroughly	L2	PO1 to PO12
C401.2	Describe various networking architectures	L3	PO1 to PO12
C401.3	Identify the protocols and services of different layers.	L3	PO1 to PO12
C401.4	Distinguish the basic network configurations and standards associated with each network	L3	PO1 to PO12
C401.5	Analyze a simple network and measurement of its parameters.	L2	PO1 to PO12
	Total Hours of instruction		**40**

4.0 Course Content

Module-1	RBT Level
Introduction: Data communication: Components, Data representation, Data flow, Networks:Network criteria, Physical Structures, Network types: LAN, WAN, Switching, The Internet.(1.1,1.2, 1.3(1.3.1to 1.3.4 of Text). **Network Models:** Protocol Layering: Scenarios, Principles, Logical Connections, TCP/IPProtocol Suite: Layered Architecture, Layers in TCP/IP suite, Description of layers, Encapsulationand Decapsulation, Addressing, Multiplexing and Demultiplexing, The OSI Model: OSI VersusTCP/IP. (2.1, 2.2, 2.3 of Text)	L1, L2
Module-2	
Data-Link Layer: Introduction: Nodes and Links, Services, Two Categories of link, Sublayers,Link Layer addressing: Types of addresses, ARP. Data Link Control (DLC) services: Framing,Flow and Error Control, Data Link Layer Protocols: Simple Protocol, Stop and Wait protocol,Piggybacking. (9.1, 9.2(9.2.1, 9.2.2), 11.1, 11.2of Text) **Media Access Control**: Random Access: ALOHA, CSMA, CSMA/CD, CSMA/CA. (12.1 ofText). **Wired and Wireless LANs:** Ethernet Protocol, Standard Ethernet. Introduction to wireless LAN:Architectural Comparison, Characteristics, Access Control. (13.1, 13.2(13.2.1 to 13.2.5), 15.1 ofText)	L1, L2,L3
Module-3	
Network Layer: Introduction, Network Layer services: Packetizing, Routing and Forwarding,Other services, Packet Switching: Datagram Approach, Virtual Circuit Approach, IPV4Addresses: Address Space, Classful Addressing, Classless Addressing, DHCP, Network AddressResolution, Forwarding of IP Packets: Based on destination Address and Label. (18.1, 18.2, 18.4,18.5.1, 18.5.2 of Text) **Network Layer Protocols:** Internet Protocol (IP): Datagram Format, Fragmentation, Options,Security of IPv4 Datagrams. (19.1of Text). **Unicast Routing:** Introduction, Routing Algorithms: Distance Vector Routing, Link StateRouting, Path vector routing. (20.1, 20.2of Text)	L1, L2,L3
Module -4	
Transport Layer: Introduction: Transport Layer Services, Connectionless and Connectionoriented Protocols, Transport Layer Protocols: Simple protocol, Stop and wait protocol, Go-BackN Protocol, Selective repeat protocol. (23.1, 23.2.1, 23.2.2, 23.2.3, 23.2.4 of Text) **Transport-Layer Protocols in the Internet:** User Datagram Protocol: User Datagram, UDP Services, UDP Applications, Transmission ControlProtocol: TCP Services, TCP Features, Segment, Connection, State Transition diagram, Windowsin TCP, Flow control, Error control, TCP congestion control.(24.2, 24.3.1, 24.3.2, 24.3.3, 24.3.4, 24.3.5, 24.3.6, 24.3.7, 24.3.8, 24.3.9 of Text)	L1, L2, L3
Module -5	
Application Layer: Introduction: providing services, Application- layer paradigms, StandardClient –Server Protocols: World wide web, Hyper Text Transfer Protocol, FTP: Two connections,Control Connection, Data Connection, Electronic Mail: Architecture, Wed Based Mail, Telnet:Local versus remote logging.Domain Name system: Name space, DNS in internet, Resolution,DNS Messages, Registrars, DDNS, security of DNS. (25.1, 26.1, 26.2, 26.3, 26.4, 26.6 of Text)	L1, L2

5.0 Relevance to future subjects

Sl No	Semester	Subject	Topics
01	VIII	Project work	Computer communication network based projects.
02	Higher	Computer communication networks 1&2	OSI model architecture, algorithms of data link layer programs. Routing algorithms.

6.0	Relevance to Real World

SL.No	Real World Mapping
01	Computer communication network-based components.
02	OSI Model creation for analysis.
03	Development of a software application.

7.0	Gap Analysis and Mitigation

SL. No	Delivery Type	Details
01	Tutorial	Topic: Lettering, Line, Methods of dimensioning
02	NPTEL	Programming and Applications

8.0	Books Used and Recommended to Students

Text Books

1.**Forouzan, "Data Communications and Networking" , 5th Edition, McGraw Hill, 2013, ISBN: 1-25-906475-3.**

Reference Books

1. James J Kurose, Keith W Ross, Computer Networks, , Pearson Education.
2. Wayarles Tomasi, Introduction to Data Communication and Networking, Pearson Education.
3. Andrew Tanenbaum, "Computer networks", Prentice Hall.
4. William Stallings, "Data and computer communications", Prentice Hall

Additional Study material & e-Books

1. https://lecturenotes.in/subject/609/computer-communication-network-ccn
2. http://freecomputerbooks.com/networkComputerBooks.html

9.0	Relevant Websites (Reputed Universities and Others) for Notes /Animation / Videos Recommended

Website and Internet Contents References

1) https://vtu.ac.in
2) http://www.bookspar.com/engineering-vtu
3) http://www.rejinpaul.com/2014/10/vtu-ece-notes-vtu-ece-1st-2nd-3rd-4th-5th-6th-7th-8th-semester-lecture-notes-download-link.htmlhttp://www.vlab.co.in/
4) https://www.youtube.com/results?search_query=microprocessor

10.0	Magazines/Journals Used and Recommended to Students

Sl.No	Magazines/Journals	website
1	IEEE	http://ieeexplore.ieee.org/Xplore/home.jsp
2	PC World	http://www.pcworld.com/article/146957/components/article.html

11.0	Examination Note

Scheme of Evaluation for Internal Assessment (40 Marks)
- Class work, Assignment, Technical quiz: 10 Marks.
- Internal Assessment test Average of all three Tests 30marks.

SCHEME OF EXAMINATION:
- The question paper will have ten questions.
- Each full question consists of 20marks**.**
- There will be 2 full questions (with a maximum of four sub questions) from each module.

- Each full question will have sub questions covering all the topics under a module
- The students will have to answer 5 full questions, selecting one full question from each module.
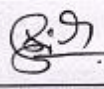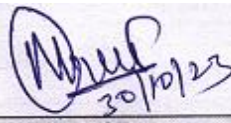
12.0 Course Delivery Plan

Module	Lecture No.	Content of Lecturer	% of Portion
Module- 1 Introduction& Network Models	1	Data communication: Components, Data representation, Data flow	20
	2	Networks:Network criteria, Physical Structures	
	3	Network types: LAN, WAN, Switching, The Internet.	
	4	Protocol Layering: Scenarios, Principles, Logical Connections	
	5	TCP/IPProtocol Suite: Layered Architecture	
	6	Layers in TCP/IP suite, Description of layers	
	7	Encapsulationand Decapsulation, Addressing, Multiplexing and Demultiplexing	
	8	The OSI Model: OSI VersusTCP/IP.	
Module- 2 Data-Link Layer, Media Access Control&Wired and Wireless LANs	9	Introduction: Nodes and Links, Services, Two Categories of link, Sublayers	20
	10	Link Layer addressing: Types of addresses, ARP. Data Link Control (DLC) services	
	11	Framing,Flow and Error Control, Data Link Layer Protocols	
	12	Simple Protocol, Stop and Wait protocol,Piggybacking	
	13	Random Access: ALOHA, CSMA	
	14	CSMA/CD, CSMA/CA	
	15	Ethernet Protocol, Standard Ethernet. Introduction to wireless LAN	
	16	Architectural Comparison, Characteristics, Access Control.	
Module -3 Network Layer, Network Layer Protocols& Unicast Routing	17	Introduction, Network Layer services: Packetizing, Routing and Forwarding,Other services	20
	18	Packet Switching: Datagram Approach, Virtual Circuit Approach, IPV4Addresses	
	19	Address Space, Classful Addressing, Classless Addressing, DHCP	
	20	Forwarding of IP Packets: Based on destination Address and Label.	
	21	Internet Protocol (IP): Datagram Format	
	22	Fragmentation, Options, Security of IPv4 Datagrams	
	23	Introduction, Routing Algorithms: Distance Vector Routing	
	24	Link StateRouting, Path vector routing	
Module -4 Transport Layer, Transport-Layer Protocols in the Internet	25	Introduction: Transport Layer Services	20
	26	Connectionless and Connectionoriented Protocols	
	27	Transport Layer Protocols: Simple protocol, Stop and wait protocol	
	28	Go-BackN Protocol, Selective repeat protocol.	
	29	User Datagram Protocol: User Datagram, UDP Services, UDP Applications	
	30	Transmission ControlProtocol: TCP Services	
	31	TCP Features, Segment, Connection, State Transition diagram	
	32	Windowsin TCP, Flow control, Error control, TCP congestion control.	
Module 5: Application Layer	33	Introduction: providing services, Application- layer paradigms	20
	34	StandardClient –Server Protocols	
	35	World wide web, Hyper Text Transfer Protocol	
	36	FTP: Two connections,Control Connection	
	37	Data Connection, Electronic Mail: Architecture	
	38	Wed Based Mail, Telnet:Local versus remote logging.Domain Name system	
	39	Name space, DNS in internet, Resolution,DNS Messages, Registrars	
	40	DDNS, security of DNS	

13.0   University Result

Examination	FCD	FC	SC	% Passing
2021-22	0	33	1	100

Prepared by	Checked by		
Prof. B. P. Khot	**Dr. S. S. Ittannavar**	**HOD**	**Principal**

Subject Title	VLSI Design		
Subject Code	18EC72	**IA Marks**	40
Number of Lecture Hrs / Week	03 L	**Exam Marks**	60
Total Number of Lecture Hrs	40	**Exam Hours**	03
FACULTY DETAILS:			
Name: Prof. S S. Kamate	**Designation:** Asst. Professor		**Experience: 20.5** yrs.
No. of times course taught: 03		**Specialization:** Digital Electronics	

1.0   Prerequisite Subjects:

Sl. No	Branch	Semester	Subject
01	ECE	III	Analog Electronic Circuits
02	ECE	III	Digital Electronics

2.0   Course Objectives

1. Impart knowledge of MOS transistor theory and CMOS technologies.
2. Learn the operation principles and analysis of inverter circuits.
3. Design Combinational, sequential and dynamic logic circuits as per the requirements.
4. Infer the operation of Semiconductors Memory circuits.
5. Demonstrate the concepts of CMOS testing.

3.0   Course Outcomes

Having successfully completed this course, the student will be able to draw and analyze.

	Course Outcome	Cognitive Level	Pos
C402.1	Demonstrate understanding of MOS transistor theory, CMOS fabrication flow and technology scaling.	U	PO1, PO2 PO3, PO5, PO8,PO9, PO10 PO12
C402.2	Draw the basic gates using the stick and layout diagrams with the knowledge of physical design aspects.	U	PO1, PO2 PO3, PO5, PO8,PO9, PO10 PO12
C402.3	Demonstrate ability to design Combinational, sequential and dynamic logic circuits as per the requirements.	U	PO1, PO2 PO3, PO5, PO8,PO9, PO10 PO12
C402.4	Interpret Memory elements along with timing considerations.	U	PO1, PO2 PO3, PO5, PO8,PO9, PO10 PO12
C402.5	Interpret testing and testability issues in VLSI Design	U	PO1, PO2 PO3, PO5, PO8,PO9, PO10 PO12
Total Hours of instruction		**40**	

4.0 Course Content

Course Content:

Module	Teaching Hours	Bloom's Taxonomy (RBT) level
Module 1: **Introduction:** A Brief History, MOS Transistors, CMOS Logic to 1.4 of TEXT2) **MOS Transistor Theory:** Introduction, Long-channel I-V Characteristics, Non-ideal I-V Effects, DC Transfer Characteristics **(2.1, 2.2, 2.4 and 2.5 of TEXT2).**	**08 Hours**	**L1, L2**
Module 2: **Fabrication:** CMOS Fabrication and Layout, VLSI Design Flow, Introduction, CMOS Technologies, Layout Design Rules, **(1.5 and 3.1 to 3.3 of TEXT2).** MOSFET Scaling and Small-Geometry Effects, MOSFET Capacitances **(3.5 to 3.6 of TEXT1)**	**08 Hours**	**L1, L2**
Module 3: **Delay:** Introduction, Transient Response, RC Delay Model, Linear Delay Model, Logical Efforts of Paths **(4.1 to 4.5 of TEXT2, except sub-sections 4.3.7, 4.4.5, 4.4.6, 4.5.5 and 4.5.6).** **Combinational Circuit Design:** Introduction, Circuit families **(9.1 to 9.2 of TEXT2, except subsection 9.2.4).**	**08 Hours**	**L1, L2, L3**
Module 4: **Sequential Circuit Design:** Introduction, Circuit Design for Latches and Flip-Flops **(10.1 and 10.3.1 to 10.3.4 of TEXT2)** **Dynamic Logic Circuits:** Introduction, Basic Principles of Pass Transistor Circuits, Synchronous Dynamic Circuit Techniques, Dynamic CMOS Circuit Techniques **(9.1, 9.2, 9.4 to 9.5 of TEXT1)**	**08 Hours**	**L1, L2, L3**
Module 5: **Semiconductor Memories:** Introduction, Dynamic Random Access Memory (DRAM) and Static Random Access Memory (SRAM), **(10.1 to 10.3 of TEXT1)** **Testing and Verification:** Introduction, Logic Verification Principles, Manufacturing Test Principles, Design for testability **(15.1, 15.3, 15.5 15.6.1 to 15.6.3 of TEXT 2).**	**08 Hours**	**L1, L2**

5.0 Relevance to future subjects

Sl No	Semester	Subject	Topics
01	VII	VLSI Lab	VLSI Design of Circuits
02	VIII	Projects on VLSI	Projects and Research

6.0 Relevance to Real World

SL. No	Real World Mapping
01	Analyze different types of VLSI Designs
02	Design of different types of VLSI chips

7.0 Gap Analysis and Mitigation

Sl. No	Delivery Type	Details
01	Tutorial	Topic: VLSI Lab
02	NPTEL	Demonstration and Application

8.0	Books Used and Recommended to Students

Text Books

1. "CMOS Digital Integrated Circuits: Analysis and Design" – **Sung Mo Kang & Yosuf Leblebici,** Third Edition, Tata McGraw-Hill.

2. "CMOS VLSI Design- A Circuits and Systems Perspective"- Neil H. E. Weste, and David Money Harris4th Edition, Pearson Education.

Reference Books

1.Adel Sedra and K. C. Smith, "Microelectronics Circuits Theory and Applications", 6th or 7th Edition, Oxford University Press, International Version, 2009.

2. Douglas A Pucknell & Kamran Eshragian, "Basic VLSI Design", PHI 3rd Edition, (original Edition – 1994).

3. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", TMH, 2007.

Additional Study material & e-Books

3. VTU online notes.

9.0	Relevant Websites (Reputed Universities and Others) for Notes/Animation/Videos Recommended

Website and Internet Contents References

01) https://nptel.co.in

02) http://m.noteboy.in/vtuflies

03) https://www.edx.org/school/iitbombayx?utm_source=bing&utm_medium=cpc&utm_term=iit-bombay&utm_campaign=partner-iit-bombay

10.0	Magazines/Journals Used and Recommended to Students

Sl. No	Magazines/Journals	website
1	IEEE Xplorer	http://ieee.com
2	International Journal of Science and Technology	http://www.sciencedirect.com/science/journal/00207683
3	Journal of Communication Engineering	http://ieee.com

11.0	Examination Note

Internal Assessment: 40 Marks
Three IA will be conducted and average of best of two will be accounted.

Scheme of Evaluation for Internal Assessment (40 Marks)
(a) Internal Assessment test in the same pattern as of the main examination. (50 marks.)

SCHEME OF EXAMINATION:
Two questions to be set from the syllabus covered.
Student has to answer one part from each question.
Question 1 or 2   1x25   =   25Marks
Question 3 or 4   1x25   =   25Marks
Total   =   50Marks reduced to 30 Marks
Total CIE marks = 30 from IA and 10 from Assignment or quiz.

INSTRUCTION FOR VLSI Design (18EC72) EXAMINATION
1. Four full questions will be given which consists of a,b,c,d sub sections.
2. Students have to answer either Q :1 or 2 and Q: 3 or 4 completely.

12.0 Course Delivery Plan

Course Delivery Plan:

MODULE	LECTURE NO.	CONTENT OF LECTURE	% OF PORTION
1	1	Introduction: A Brief History of MOS transistors	20
	2	MOS Transistors	
	3	CMOS Logic	
	4	Introduction MOS Transistor Theory	
	5	Long-channel I-V Characteristics	
	6	Non-ideal I –V Effects	
	7	DC Transfer Characteristics	
	8	Cont'd…	
2	9	Introduction to CMOS Fabrication	
	10	Introduction to CMOS Fabrication and Layout	
	11	Cont'd…	
	12	Cont'd…	
	13	VLSI Design Flow	
	14	Introduction CMOS Technologies	
	15	Layout Design Rules	
	16	MOSFET Scaling	
	17	Small-Geometry Effects	
	18	MOSFET Capacitances	
3	19	Introduction to Transient Response	60
	20	RC Delay Model	
	23	Linear Delay Model	
	24	Logical Efforts of Paths	
	25	Introduction to Combinational Circuit Design Circuit families	
	26	Cont'd…	
	27	Circuit families	
4	28	Introduction to Sequential Circuit Design	80
	29	Circuit Design for Latches	
	30	Circuit Design and Flip-Flops	
	31	Cont'd…	
	32	Introduction to Dynamic Logic Circuits	
	33	Cont'd…	
	34	Basic Principles of Pass Transistor Circuits	
	35	Cont'd…	
5	36	Introduction to Semiconductor Memories	100
	37	Introduction to Dynamic Random Access Memory (DRAM) and	
	38	Cont'd…	
	39	Static Random Access Memory (SRAM)	
	40	Introduction to Testing and Verification	
	41	Logic Verification Principles	
	42	Manufacturing Test Principles	
	43	Design for testability	
	44	Cont'd…	

13.0 QUESTION BANK

MODULE -1

1. What is Moore's first law? Discuss about evaluation of integrated circuit technology.
2. Compare between different families with respect to speed and power.
3. Draw & explain basic n-MOS enhancement mode transistor action.
4. Draw & explain basic n-MOS depletion mode transistor action.
5. Draw & explain basic p-MOS enhancement mode transistor action.
6. Explain CMOS logic.
7. Explain Long-channel I-V Characteristics.
8. Explain Non-ideal I-V Effects.
9. Explain DC Transfer characteristics

MODULE -2

1. Explain in detail n-MOS fabrication process.
2. Explain in detail p well-CMOS fabrication process.
3. Explain in detail n well-CMOS fabrication process.
4. Explain VLSI design flow.
5. Draw scaled n-MOS transistor for combined voltage & dimension model.
6. Find out scaling factors for all parameters given below –
   gate area (Ag), gate capacitance per unit area (Co), gate capacitance (Cg), parasitic capacitance (Cx),
   carrier density in channel (Qon), channel resistance (Ron), gate delay (Td), maximum operating frequency
   (fo), saturation current (Idss), current density (J), switching energy per gate (Eg), power dissipation per gate
   (Pg), power dissipation per unit area (Pa), speed power product (PT).
8. Find out scaling effect on each factor in each model that is combined voltage & dimensional model, constant
   field model & constant voltage model in tabular form

MODULE -3

1. What is transient response?
2. Explain transient response of an inverter.
3. Explain RC delay model
4. Explain Linear delay model.
5. Write a note on logical efforts and paths.
6. Explain combinational logic design.
7. Write a note on combinational logic families.

MODULE -4

1. What sequential circuit design.
2. Write a note on sequential circuit design.
3. Explain circuit design for latches.
4. Explain circuit design for flip-flops.
5. What is a pass transistor?
6. Explain basic principles of pass transistor logic.
7. Explain synchronous dynamic circuit techniques.
8. Explain dynamic circuit techniques.

MODULE-5
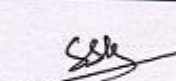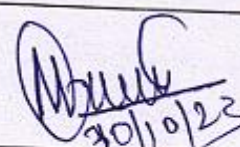
1. What are the different timing considerations?
2. Depending upon area requirement, power dissipation & volatility, discuss following memory elements –
   i) Dynamic shift register cell ii) a 3- Transistor dynamic RAM cell iii) a I-transistor dynamic memory cell.

3. Draw & explain a pseudo static RAM cell.
5. Draw circuit diagram of 4-transistor dynamic shift register cell & explain read and write
    operation with sense amplifier.
6. Draw sense amplifier used in memory array, what it's required?
7. Draw circuit & stick diagram for 6-transistor static CMOS memory cell & explain read *I* write operation
    with sense amplifier.
8. Give a logical arrangement to implement JK-FF.
9. Explain how D-FF is formed?
10. Explain how *you* will design 4X4 bit register array by using pseudo static memory cell?
11. How you will develop selection & control logic *for* 4X4 bit register array?
12. What is testing?
13. Explain logic Verification Principles
14. Explain Manufacturing Test Principles.
15. Write a note on Design for testability.
.

15.0　　　University Result

Examination	FCD	FC	SC	% Passing
Feb 2022	3	09	23	100
Feb 2023	09	09	11	100

Prepared by	Checked by		
Prof. S. S. Kamate	Prof. S. S. Kamate	30/10/23 HOD	Principal

Subject Title	Real Time Systems		
Subject Code	18EC731	CIE Marks	40
Number of Lecture Hrs / Week	03 L	SEE Marks	60
Total Number of Lecture Hrs	40	Exam Hours	03
			CREDITS – 03

FACULTY DETAILS:

Name: Prof. Sunita.S.Malaj	Designation: Asst. Professor	Experience: 25 Years
No. of times course taught: 06	Specialization: E & TC	

1.0   Prerequisite Subjects:

Sl. No	Branch	Semester	Subject
01	Electronics & Communication Engineering	I/II	Basic Electronics
02	Electronics & Communication Engineering	VI	Operating System

2.0   Course Objectives

This Course will enable students to:

- Understand the fundamentals of Real time systems and its classification.
- Describe the concepts of computer control and hardware components.
- Discuss the languages to develop software for Real –Time Applications.
- Explain the concepts of operating system & RTS development methodologies.

3.0   Course Outcomes

At the end of the course students will be able to:

	Course Outcome	RBT Level	Pos
CO303.1	Explain the fundamentals of Real Time systems and its classifications.	L2	PO1 to PO12
CO303.2	Understand the concepts of computer control & the suitable computer hardware requirements for real time applications.	L2	PO1 to PO12
CO303.3	Describe the operating system concepts and techniques required for real time systems.	L2	PO1 to PO12
CO303.4	Develop the software algorithms using suitable languages to meet real time applications.	L2	PO1 to PO12
CO303.5	Apply suitable methodologies to design & develop Real Time systems.	L2	PO1 to PO12
	Total Hours of instruction	40	

4.0   Course Content

Module-1   8 Hours

Introduction to Real-Time Systems: Historical background, Elements of a Computer Control System, RTS- Definition, Classification of Real-time Systems, Time Constraints, Classification of Programs. Concepts of Computer Control: Introduction, Sequence Control, Loop Control, Supervisory Control, Centralized Computer Control, Hierarchical Systems. (Text Book: 1.1 to 1.6 and 2.1 to 2.6)

Module-2   8 Hours

Computer Hardware Requirements for Real-Time Applications: Introduction, General Purpose Computer, Single Chip Microcomputers and Microcontrollers, Specialized Processors, Process-Related Interfaces, Data Transfer Techniques, Communications, Standard Interface.(Text Book: 3.1 to 3.8)

Module-3   8 Hours

Languages for Real-Time Applications: Introduction, Syntax Layout and Readability, Declaration and Initialization of Variables and Constants, Modularity and Variables, Compilation of Modular Programs, Data types, Control Structures, Exception Handling, Low-level facilities, Co-routines, Interrupts and Device Handling, Concurrency, Real-Time Support, Overview of Real-Time Languages. (Text Book: 5.1 to 5.14)

Module-4   8 Hours

Operating Systems: Introduction, Real-Time Multi-Tasking OS, Scheduling Strategies, Priority Structures, Task Management, Scheduler and Real-Time Clock Interrupt Handler, Memory Management, Code Sharing, Resource Control, Task Co-Operation and Communication, Mutual Exclusion.(Text Book: 6.1 to 6.11)

Module-5   8 Hours

Design of RTS – General Introduction: Introduction, Specification Document, Preliminary Design, Single-Program Approach, Foreground/Background System.
RTS Development Methodologies: Introduction, Yourdon Methodology, Ward and Mellor Method, Hately and Pirbhai Method. (Text Book: 7.1 to 7.5 and 8.1, 8.2, 8.4,8.5)

5.0	Relevance to future subjects

Sl. No	Semester	Subject	Topics
01	VII	Real Time Embedded systems	Operating Systems, Real time systems
02	VIII	Real Time Operating systems, Project Work	Design a system using PIC microcontroller in real time.

6.0	Relevance to Real World

Sl. No	Real World Mapping
01	Operate a system in Real Time.
02	Identify the elements needed to design a real time system.
03	Design a real time system.

7.0	Gap Analysis and Mitigation

Sl. No	Delivery Type	Details
01	Tutorial	Topic: Lettering, Line, Methods of dimensioning
02	NPTEL	Assembly Application

8.0	Books Used and Recommended to Students

Text Books
1. Real – Time Computer Control- An Introduction, Stuart Bennet,   2nd Edn. Pearson Education. 2005
Reference Books
1. Real –Time Systems Design & analysis, Philip A Laplante, 2nd edn PHI,2005. 2. Real –time Systems Development , Rob Williams, Elsevier.2006 3. Embedded Systems, Raj Kamal, Tata Mc Graw Hill India 2005.
Additional Study material & e-Books

1. Embedded systems ,Raj Kamal
2. Real Time Systems Design & Analysis, Phillip.A.Laplante, second edition
3. Real Time systems Development ,Rob Williams
4. Real Time Systems –Theory & Practice-Rajib Mall(ebook)

.0	Relevant Websites (Reputed Universities and Others) for Notes /Animation / Videos Recommended

Website and Internet Contents References

3) https://vtu.ac.in
4) http://www.bookspar.com/engineering-vtu
3) http://www.rejinpaul.com/2014/10/vtu-ece-notes-vtu-ece-1st-2nd-3rd-4th-5th-6th-7th-8th-semester-lecture-notes-download-link.htmlhttp://www.vlab.co.in/
4) https://www.youtube.com

10.0	Magazines/Journals Used and Recommended to Students

Sl.No	Magazines/Journals	Website
1	IEEE	http://ieeexplore.ieee.org/Xplore/home.jsp
2	PC World	http://www.pcworld.com/article/146957/components/article.html

11.0	Examination Note

Scheme of Evaluation for CIE (40 Marks)

Internal Assessment test will be done in the same pattern as that of the main examination.
 Internal Assessment: 30 Marks
 Assignment: 10 Marks

SCHEME OF EXAMINATION: 100 Marks, scaled down to 60 in VTU result sheet.
 The question paper will have ten questions.
- Each full question is for 20 marks.
- There will be 2 full questions (with a maximum of three sub questions in one full question) from each module.
- Each full question with sub questions will cover the contents under a module.
- Students will have to answer 5 full questions, selecting one full question from each module.

12.0	Course Delivery Plan

Module	Lecture No.	Content of Lecturer	% of Portion
Module 1:	1	Introduction to Real-Time Systems: Historical background, Elements of a Computer Control System	20
	2	RTS- Definition	
	3	Classification of Real-time Systems	
	4	Time Constraints	
	5	Classification of Programs	
	6	Concepts of Computer Control: Introduction, Sequence Control	
	7	Loop Control	
	8	Supervisory Control	
	9	Centralized Computer Control	
	10	Hierarchical Systems	
Module 2:	11	Computer Hardware Requirements for Real-Time Applications: Introduction	40
	12	General Purpose Computer	
	13	General Purpose Computer	

	14	Single Chip Microcomputers and Microcontrollers	
	15	Single Chip Microcomputers and Microcontrollers	
	16	Specialized Processors	
	17	Process-Related Interfaces	
	18	Data Transfer Techniques	
	19	Communications	
	20	Standard Interface	
Module 3:	21	Languages for Real-Time Applications: Introduction	60
	22	Syntax Layout and Readability	
	23	Declaration and Initialization of Variables and Constants	
	24	Modularity and Variables	
	25	Compilation of Modular Programs, Data types	
	26	Control Structures, Exception Handling	
	27	Low-level facilities, Co-routines	
	28	Interrupts and Device Handling	
	29	Concurrency, Real-Time Support	
	30	Overview of Real-Time Languages	
Module 4:	31	Operating Systems: Introduction	80
	32	Real-Time Multi-Tasking OS	
	33	Scheduling Strategies	
	34	Priority Structures	
	35	Task Management	
	36	Scheduler and Real-Time Clock Interrupt Handler	
	37	Memory Management	
	38	Code Sharing, Resource Control	
	39	Task Co-Operation and Communication	
	40	Mutual Exclusion	
Module 5:	41	Design of RTS – General Introduction: Introduction	100
	42	Specification Document	
	43	Preliminary Design	
	44	Single-Program Approach	
	45	Foreground/Background System	
	46	RTS Development Methodologies: Introduction	
	47	Yourdon Methodology	
	48	Ward and Mellor Method	
	49	Hatley and Pirbhai Method	
	50	Hatley and Pirbhai Method	

13.0 Assignments, Pop Quiz, Mini Project, Seminars

Sl.No.	Title	Outcome expected	Allied study	Week No.	Individual / Group activity	Reference: book/website /Paper
1	Assignment 1: University Questions on Introduction to real time systems	Students study the Topics and write the Answers. Get practice to solve university questions.	Module 1,2 of the syllabus	4	Individual Activity.	Text book
2	Assignment 2: University Questions on computer Hardware requirements for Real Time applications	Students study the Topics and write the Answers. Get practice to solve university questions.	Module 1,2 of the syllabus	8	Individual Activity.	Text book
3	Assignment 3: University Questions Languages for Real	Students study the Topics and write the Answers. Get practice	Module 1,2 of the syllabus	12	Individual Activity.	Text book

	Time applications	to solve university questions.				
4	Assignment 4: University Questions on Operating Systems	Students study the Topics and write the Answers. Get practice to solve university questions.	Module 1,2 of the syllabus	16	Individual Activity.	Text book
5	Assignment 5: University Questions on Design of RTS.	Students study the Topics and write the Answers. Get practice to solve university questions.	Module 1,2 of the syllabus	16	Individual Activity.	Text book

14.0 QUESTION BANK

Module I

1. Define real time system.
2. Differentiate real time system & Non real time system.
3. Explain the historical background of real time systems.
4. Give the classification of RTS based on time constraints.
5. Draw the elements of a computer control system & explain.
6. Explain the following: 1) Cyclic tasks 2) Event based tasks 3) Interactive systems.
7. Explain the following programs. 1) Sequential 2) Multitasking 3) Real time .
8. Give the classification of field applications in real time systems.
9. Explain Sequence control for single chemical reactor vessel.
10. Explain DDC & PID control Algorithm Format. Give the advantages of DDC over analog control.
11. Explain DDC Applications for boiler control scheme.
12. Explain Supervisory Control & illustrate the concept of supervisory control for Evaporation Plant.
13. Explain Hierarchical System with diagram & Batch control using a Hierarchical system.
14. Explain Distributed Systems & Human Computer Interface.
15. List the responsibility of control engineer.
16. Explain the three different forms of adaptive control.
17. What are the objectives & benefits of computer control system.

Module II

1. Explain general purpose computer with block diagram.
2. Explain single chip microcomputers & microcontrollers. Differentiate between single chip microcontroller & Microcomputer.
3. Explain specialized processors.
4. Explain the different forms of parallel computer architectures.
5. Explain process related interfaces.
6. With diagram explain pulse input interface.
7. With diagram explain pulse output interface.
8. With neat diagram explain analog input interface.
9. With neat diagram explain analog output interface.
10. Explain the diff data transfer techniques.
11. Explain Specialized Processors.
12. Explain communications with diagram .Give the different ways of characterizing serial communication techniques.
13. Explain the concept of standard interfaces.
14. Explain the following network topologies. 1) Ring 2) Star 3) Mesh 4) Bus
15. Explain with diagram digital input interface.
16. Explain with diagram digital output interface.
17. What is interrupt? Explain the applications of interrupts.

Module III

1. Explain in brief introduction to languages for real time applications
2. Explain the following
    1) Security 2) Readability 3) Flexibility 4) simplicity 5) portability 6) Efficiency
3. Explain how to declare & initialize the variables & constants
4. Explain different data types.
5. Explain low level facilities.
6. Explain run time support.
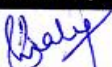
7. Explain Coroutines.

Module IV

1. Explain general purpose operating system & OS with minimum Kernel with diagram.
2. With diagram explain the relationship between various sections of an O.S ,Computer H/W & user.
3. Explain the multitasking RTOS with diagram.
4. What are the different scheduling strategies.
5. What are the functions of task management. Explain task states with task activation diagram.
6. Explain priority structures with diagram.
7. What is memory management. Explain partitioned & Non partitioned memory.
8. With example explain task chaining & Swapping.
9. Explain Code sharing & its problem.
10. with diagram explain the following: 1. Serially Reusable code. 2. Reentrant code.
11. What is semaphore.Explain the concept.
12. What is Monitors. Explain the concept with an example.
13. Explain the concept of channel & Pool.
14. What is mutual exclusion.Explain the concept.
15. Explain task co-operation & communication.
16. Explain liveness.Explain the concept with a example.

Module V

1. With diagram explain Planning Phase & give the table for the % of Rectifying & Correcting errors.
2. With diagram explain Secondary phase.
3. With diagram explain the concept of software design in case of preliminary design of RTSS.
4. With flow chart explain single program approach & write the requirements for the same.
5. With flow chart explain foreground/background program approach & write the requirements for the same.
6. what is multitasking approach.Explain
7. What is monitors.Explain
8. What is Rendezous.Explain
9. Explain the concept of condition flag for design of RTSS.
10. What are the three different phases involved in design of an Real time system.
11. What are the key ideas of Yourdon methodology.
12. Explain ward & mellor method with basic diagram.
13. Draw the the Level1 transformation diagram for drying oven &explain.
14. Draw the Architectural diagram for drying oven & explain with hatley & pirabhai method.
15. Differentiate between Ward & Mellor & Hatley & Pirabhai method.

16.0   University Result

Examination	FCD	FC	SC	% Passing
2020-21	11	18	05	100
2019-20	11	5	2	100

Prepared by	Checked by		
Prof. S.S.Malaj	Prof.S.S.Patil	HOD	Principal

Subject Title	Multimedia Communication		
Subject Code	18EC743	CIE Marks	40
Number of Lecture Hrs / Week	03 L	SEE Marks	60
Total Number of Lecture Hrs	40 (08 Hours/Module)	Exam Hours	03

FACULTY DETAILS:

Name: Dr. S S Ittannavar	Designation: Associate Professor	Experience:10.8 yrs
No. of times course taught: 03		Specialization: Digital Signal Processing

1.0 Prerequisite Subjects:

Sl. No	Branch	Semester	Subject
01	ECE	IV	Signals and Systems
02	ECE	V	Digital Signal Processing
03	ECE	VI	Digital Communication

2.0 Course Objectives

This course will enable students to:
- Understand the importance of multimedia in today's online and offline information sources and repositories.
- Understand the how Text, Audio, Image and Video information can be represented digitally in a computer so that it can be processed, transmitted and stored efficiently.
- Understand the Multimedia Transport in Wireless Networks.
- Understand the Real-time multimedia network applications.
- Understand the Different network layer based application.

3.0 Course Outcomes

Having successfully completed this course, the student will be able to

	Course Outcome	Cognitive Level	POs
C312C.1	Understand basics of different multimedia networks and applications.	L2	PO1, PO2, PO3, PO6, PO8, PO11, PO12
C312C.2	Understand different compression techniques to compress audio and video.	L2	PO1, PO2, PO3, PO6, PO8, PO11, PO12
C312C.3	Describe multimedia Communication across Networks.	L2	PO1, PO2, PO3, PO4, PO6, PO8,
C312C.4	Analyse different media types to represent them in digital form.	L2	PO1, PO2, PO3, PO4, PO6, PO8, PO11, PO12
C312C.5	Compress different types of text and images using different compression techniques and analyse DMS.	L2	PO1, PO2, PO3, PO6, PO8, PO11, PO12
Total Hours of instruction			**40**

4.0   **Course Content**

Course Content:

MODULE -1	RBT Level
Multimedia Communications: Introduction, Multimedia information representation, multimedia networks, multimedia applications, Application and networking terminology. (Chap 1 of Text 1) **08 Hours**	L1, L2
MODULE -2	
Information Representation: Introduction, Digitization principles, Text, Images, Audio and Video (Chap 2 of Text 1) **08 Hours**	L1, L2
MODULE -3	
Text and image compression: Introduction, Compression principles, text compression, image Compression. (Chap 3 of Text 1) **Distributed multimedia systems:** Introduction, main Features of a DMS, Resource management of DMS, Networking and Multimedia operating systems (Chap. 4 - Sections 4.1 to 4.5 of Text 2). **08 Hours**	L1, L2
MODULE -4	
Audio and video compression: Introduction, Audio compression, video compression, video compression principles, video compression. (Chap. 4 of Text 1). **08 Hours**	L1, L2
MODULE -5	
Multimedia Information Networks: Introduction, LANs, Ethernet, Token ring, Bridges, FDDI High-speed LANs, LAN protocol (Chap. 8 of Text 1). **The Internet:** Introduction, IP Datagrams, Fragmentation, IP Address, ARP and RARP, QoS Support, IPv8.(Chap. 9 of Text 1) **08 Hours**	L1, L2

5.0   **Relevance to future subjects**

Sl . No	Semester	Subject	Topics
01	VIII	Project work	Design Communication system

6.0   **Relevance to Real World**

Sl. No	Real World Mapping
01	Multimedia Communication Technologies are digital tools that allow two or more people to communicate with one another.
02	These can be written, verbal, visual or audible communication

7.0   **Gap Analysis and Mitigation**

Sl. No	Delivery Type	Details
01	Tutorial	Topic: Multimedia Modulation Techniques, Networks, Transport Protocol.
02	NPTEL	ISI, Equalizers.

8.0 Books Used and Recommended to Students

Text Books

1. Fred Halsall, "Multimedia Communications", Pearson education, 2001 ISBN - 9788131709948.

2. K. R. Rao, Zoran S. Bojkovic, Dragorad A. Milovanovic, "Multimedia Communication Systems", Pearson education, 2004. ISBN -9788120321458

Reference Books

1. Raifsteinmetz, Klara Nahrstedt, "Multimedia: Computing, Communications and Applications", Pearson education, 2002. ISBN -978817758

Additional Study material & e-Books

4. NPTEL notes and Videos
5. VTU online notes.

9.0 Relevant Websites (Reputed Universities and Others) for Notes/Animation/Videos Recommended

Website and Internet Contents References

5) www.citystudentsgroup.com
6) http://everythingvtu.wordpress.com
7) www.nptelvideos.in/

10.0 Magazines/Journals Used and Recommended to Students

Sl. No	Magazines/Journals	website
1	IEEE Transactions on Communication systems	ieeexplore.ieee.org/xpl/RecentIssue.jsp?punumber=4547466
2	Digital Communications and Networks - Journal - Elsevier	www.journals.elsevier.com/digital-communications-and-networks/
3	International Journal of Digital Communication and Networks	ijdcn.co.in
	Journal of Communication - Wiley Online Library	onlinelibrary.wiley.com

11.0 Examination Note

Internal Assessment: 40 Marks
Three IA will be conducted and average of three will be accounted for 30 Marks.
Assignment is10 Marks.
Total is 40 Marks

Scheme of Evaluation for Internal Assessment (50 Marks)
Four full questions will be given which consists of a, b as sub sections.
Students have to answer either Q: 1 or 2 and Q 3 or 4 completely.
Question 1 or 2   for 25 or 25Marks
Question 3 or 4   for 25 or 25Marks
Each IA will be conducted for 50 Marks.
Three IA will be conducted and average of three will be accounted for 30 Marks.
Assignment is 10 Marks
Total = 40Marks

Scheme of External Exam (60 Marks)
Ten questions to be set from the syllabus covered.
Each Module consists of two questions. Each question consists of a, b, c and d sub questions.

Student has to answer one full question from Each Module.
Each Module Consists of 20 Marks. Total 5 Modules=5*20=100 Marks
This 100 Marks results will be converted for 60 Marks.

| 12.0 | Course Delivery Plan |

Course Delivery Plan:

MODULE	LECTURE NO.	CONTENT OF LECTURE	% OF PORTION
1	1	**Multimedia Communications**: Introduction, Multimedia information representation.	20
	2	Multimedia information representation.	
	3	Multimedia networks	
	4	Multimedia networks	
	5	Multimedia applications	
	6	Multimedia applications	
	7	Application and networking terminology.	
	8	Application and networking terminology	
2	9	Introduction	20
	10	Digitization principles	
	11	Text representation	
	12	Text representation	
	13	Image representation	
	14	Image representation	
	15	Audio representation	
	16	Video representation	
3	17	**Text and image compression:** Introduction, Compression principles.	20
	18	Text compression	
	19	Image Compression.	
	20	**Distributed multimedia systems:** Introduction	
	21	Main Features of a DMS	
	22	Resource management of DMS	
	23	Networking and Multimedia operating systems	
	24	Networking and Multimedia operating systems	
4	25	**Audio and video compression:** Introduction	20
	26	Audio compression	
	27	Audio compression	
	28	Video compression	
	29	Video compression	
	30	Video compression principles.	
	31	Video compression	
	32	Video compression	
5	33	**Multimedia Information Networks:** Introduction	20
	34	LANs, Ethernet, Token ring	
	35	Bridges, FDDI High-speed LANs	

36	LAN protocol
37	**The Internet:** Introduction, IP Datagrams
38	Fragmentation, IP Address
39	ARP and RARP
40	QoS Support, IPv8.

13.0   Assignments, Pop Quiz, Mini Project, Seminars

Sl. No.	Title	Outcome expected	Allied study	Week No.	Individual / Group activity	Reference: book/website /Paper
1	Assignment 1: University Questions on Networks, media types and information representation.	Students study the Topics and write the Answers. Get practice to solve university questions.	Module 1 of the syllabus	2	Individual Activity. Printed solution expected.	Text Book 1, of the reference list. Website of the Reference list
2	Assignment 2: University Questions on Text, Image, Audio, Video representation.	Students study the Topics and write the Answers. Get practice to solve university questions.	Module 2 of the syllabus	4	Individual Activity. Printed solution expected.	Text Book 1, of the reference list. Website of the Reference list
3	Assignment 3: University Questions on Text, Image, Compression.	Students study the Topics and write the Answers. Get practice to solve university questions.	Module 3 of the syllabus	5	Individual Activity. Printed solution expected.	Text Book 2, of the reference list. Website of the Reference list
4	Assignment 4: University Questions on Audio, Video Compression.	Students study the Topics and write the Answers. Get practice to solve university questions.	Module 4 of the syllabus	6	Individual Activity. Printed solution expected.	Text Book 1, of the reference list. Website of the Reference list
5	Assignment 5: University Questions on Multimedia Communication across networks.	Students study the Topics and write the Answers. Get practice to solve university questions.	Module 5 of the syllabus	6	Individual Activity. Printed solution expected.	Text Book 2, of the reference list. Website of the Reference list

14.0   Assignment Questions

Assignment No	Questions	Marks
I	1) The term "multimedia" composed of many media types. Explain them [06]. [Dec-08] 2) Explain briefly the entertainment applications of multimedia [06]. [Dec-08] 3) Mention different modes of multipoint conferencing. [Dec-09] [4] 4) With the help of a diagram, describe the components of PSTN. [10][Jun10] 5) Explain the working of CO packet switched network including routing table. [10] [Dec2010]	5marks for each
II	1. Explain operational modes of communication channel. 2. Explain interactive television application for both cable and satellite network. 3. Mention different modes of multipoint conferencing.	5marks for each

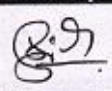|		
	4. Explain 4:2:2 and QCIF digitization formats.	
	5. Explain the principle of operation of a PCM speech codec with block diagram.	
III	1. Explain basic mode and dynamic mode of compression if image using GIF. 2. Compare arithmetic coding and Huffman coding. 3. Explain DPCM with encoder and decoder schematic. 4. Explain ADPCM with block diagram 5. Explain error tracking procedures of H.263, with neat diagrams.	5marks for each
IV	1. Explain Root Bridge, designated cost, root path cost and root port, designated bridge and designated cost. 2. Explain in detail LAN protocols and protocol framework. 3. Explain how RARP is used to enable a diskless host to determine its own IP address from its local server. 4. Explain IP datagram /packet format. 5. Explain the operation of Internet with a neat diagram.	5marks for each
V	1. Explain different types of token ring formats.. 2. Explain the general structure of FDDI High speed LAN.. 3. Explain with neat block diagram of LAN Protocol. 4. Explain ARP and RARP usage and package format. 5. Explain the architecture of Ipv8.	5marks for each

15.0   QUESTION BANK

1. The term "multimedia" composed of many media types. Explain them [06]. [Dec-08]

2. Explain briefly the entertainment applications of multimedia [06]. [Dec-08]

3. Mention different modes of multipoint conferencing. [Dec-09] [4]

4. With the help of a diagram, describe the components of PSTN. [10][Jun10]

5. Explain the working of CO packet switched network including routing table. [10] [Dec2010]

6. Explain operational modes of communication channel. [Dec 2010]

7. Explain speech only interpersonal application. [10][Dec - 2011]

8. Explain interactive television application for both cable and satellite network. [10][June-2012]

9. Explain briefly three types of text that are used to produce pages of documents. [06] [June 12 & Dec 09]

10. Derive the time to transmit a 640X480X8 image at 64 Kbps and 1.5 Mbps separately. [04][Dec 09]

11. Explain briefly MIDI standard and its associated messages. [08][June -2010]

12. Explain the principle of operation of a PCM speech codec with block diagram. [10] [Dec 2011]

13. Explain 4:2:2 and QCIF digitization formats.[10][June 2011]

14. Explain how an image produced by a scanner or digital camera is captured and stored within a computer memory? [08][Dec 2011]

15. Explain run length encoding compression. .[06] [June 12 & Dec 09]

16. Explain basic mode and dynamic mode of compression if image using GIF. [08] [June 2010]

17. Explain Huffman coding. [10][Dec 2010]

18. Explain JPEG encoder. [10][Dec - 2011]

19. Compare arithmetic coding and Huffman coding. [Dec-08] [06]

20. Explain features of TIFF. [08][June 2012]

21. Explain DPCM with encoder and decoder schematic. [08][June -2010]

22. Explain P x 64 standard used for video compression. . [10][Dec - 2011]

23. Explain ADPCM with block diagram.[08][June 2010/ Dec 11]

24. Explain H.261 video encoder. [10][June 2010 & June 12]

25. Explain video compression principles, with a neat diagram, explain B frame encoding.[08] [Dec 2011]

26. Explain error tracking procedures of H.263, with neat diagrams. .[10][June 2011]

27. Explain Root Bridge, designated cost, root path cost and root port, designated bridge and designated cost. [10][May / June 2010 & Dec 11].

28. Explain different types of token ring formats.

29. Explain the general structure of FDDI High speed LAN.

30. Explain with neat block diagram of LAN Protocol.

31. Explain ARP and RARP usage and package format.

32. Explain the architecture of Ipv8.

16.0   University Result

Examination	FCD	FC	SC	% Passing
July- 2018	11	08	12	100
July- 2017	--	--	--	--
July- 2016	--	--	--	--

Prepared by	Checked by		
		30/10/23	
Prof. B. P. Khot	Dr. S. S. Ittannavar	HOD	Principal

3Subject Title		**ENERGY AND ENVIRONMENT**	
Subject Code		18ME751	**IA Marks**	40
No of Lecture Hrs + Tutorial Hrs / Week		03	**Exam Marks**	60
Total No of Lecture + Tutorial Hrs		40	**Exam Hours**	03
			CREDITS – 03	

FACULTY DETAILS:

Name: Dr. M. M. Shivashimpi	**Designation:** Associate Professor	**Experience:** 16 Years
No. of times course taught: 02		**Specialization:** Thermal Power Engineering

1.0   Prerequisite Subjects:

Sl. No	Branch	Semester	Subject
1	Common to all	I/II	Chemistry
2	Common to all	I/II	Physics
3	Common to all	V	Environmental Studies

2.0   Course Objectives

1. To understand the fundamentals of energy sources, energy use, energy efficiency, and resulting environmental implications of various energy supplies.
2. To learn about methods of energy storage, energy management and economic analysis
3. To understand the causes and remedies related to social issues like global warming, ozone layer depletion, climate change etc.
4. To understand environment and its ecosystems.
5. To introduce various aspects of environmental pollution and its control. To introduce various acts related to prevention and control of pollution of water and air, forest protection act, wild life protection act etc.

3.0   Course Outcomes

The student, after successful completion of the course, will be able to

CO	Course Outcome	RBT level	Pos
C413.1	Summarize the basic concepts of energy, its distribution and general Scenario.	L1,l2	PO1, PO2, PO3, PO4, PO6, PO7, PO8, PO9, PO12
C413.2	Explain different energy storage systems, energy management, audit and economic analysis.	L1,l2, l3	PO1, PO2, PO3, PO4, PO6, PO7, PO8, PO9, PO12
C413.3	Summarize the environment eco system and its need for awareness.	L1,l2	PO1, PO2, PO3, PO4, PO6, PO7, PO8, PO9, PO12
C413.4	Identify the various types of environment pollution and their effects.	L1,l2	PO1, PO2, PO3, PO4, PO6, PO7, PO8, PO9, PO12
C413.5	Discuss the social issues of the environment with associated acts.	L1,l2	PO1, PO2, PO3, PO4, PO6, PO7, PO8, PO9, PO12
Total Hours of instruction			**40**

4.0   Course Content

Module-1: Basic Introduction to Energy: Energy and power, forms of energy, primary energy sources, energy flows, world energy production and consumption, Key energy trends in India: Demand, Electricity, Access to modern energy, Energy production and trade, Factors affecting India's energy development: Economy and demographics Policy and institutional framework, Energy prices and affordability, Social and environmental aspects, Investment. (8 Hours)

Module-2: Energy storage systems: Thermal energy storage methods, Energy saving, Thermal energy storage systems Energy Management: Principles of Energy Management, Energy demand estimation, Energy pricing Energy Audit: Purpose, Methodology with respect to process Industries, Characteristic method employed in Certain Energy Intensive Industries. (8 Hours)

Module-3: Environment: Introduction, Multidisciplinary nature of environmental studies- Definition, scope and importance, Need for public awareness. Ecosystem: Concept, Energy flow, Structure and function of an ecosystem. Food chains, food webs and ecological pyramids, Forest ecosystem, Grassland ecosystem, Desert ecosystem and Aquatic ecosystems, Ecological succession.

Module-4: Environmental Pollution: Definition, Cause, effects and control measures of – Air pollution, Water pollution, Soil pollution, Marine pollution, Noise pollution, Thermal pollution and Nuclear hazards, Solid waste Management, Disaster management Role of an individual in prevention of pollution, Pollution case studies. (8 Hours)

Module-5: Social Issues and the Environment: Climate change, global warming, acid rain, ozone layer depletion, nuclear accidents and holocaust. Case Studies. Wasteland reclamation, Consumerism and waste products, Environment Protection Act, Air (Prevention and Control of Pollution) Act, Water (Prevention and control of Pollution) Act, Wildlife Protection Act, Forest Conservation Act, Issues involved in enforcement of environmental legislation. Group assignments: Assignments related to e-waste management; Municipal solid waste management; Air pollution control systems; Water treatment systems; Wastewater treatment plants; Solar heating systems; Solar power plants; Thermal power plants; Hydroelectric power plants; Bio-fuels; Environmental status assessments; Energy status assessments etc. (8 Hours)

5.0   Relevance to future subjects/Career

SL. No	Semester	Subject	Topics / Relevance
01	VII & VIII	Project Phase-1 & Pahse-2	All modules
02	After graduation	Energy and Pollution Analysis and resolving related problems	All modules

6.0   Relevance to Real World

SL. No	Real World Mapping
01	Electrical Engineering and Automobile Engineering
02	Power plant engineering, thermal power plant
03	Environmental Science

7.0   Gap Analysis and Mitigation

Sl. No	Delivery Type	Details
01	nptel.ac.in	E- Learning
02	VTU, E- learning	E- Learning
03	Open courseware	E- Learning

8.0   Books Used and Recommended to Students

Text Books
Textbook for Environmental Studies For Undergraduate Courses of all Branches of Higher Education by University grant commission and Bharathi Vidyapeeth Institute of environment education and Research ,Pune 2. De, B. K., Energy Management audit & Conservation, 2nd Edition, Vrinda Publication, 2010.

Reference Books

1. Turner, W. C., Doty, S. and Truner, W. C., Energy Management Hand book, 7th edition, Fairmont Press, 2009.
2. Murphy, W. R., Energy Management, Elsevier, 2007.
3. Smith, C. B., Energy Management Principles, Pergamum, 2007
4. Environment pollution control Engineering by C S rao, New Age International, 2006, reprint 2015, 2nd edition
5. Environmental studies, by Benny Joseph, Tata McGraw Hill, 2008, 2nd edition.

Additional Study material & e-Books

- Nptel.ac.in
- VTU, E- learning
- India Energy Outlook 2015(www.iea.org/.../IndiaEnergyOutlook_WEO2015.pdf)
- Open courseware

9.0	**Relevant Websites (Reputed Universities and Others) for Notes/Animation/Videos Recommended**

Website and Internet Contents References

1. http://www.nptel.ac.in
2. www.iea.org

10.0	**Magazines/Journals Used and Recommended to Students**

Sl.No	Magazines/Journals	website
1	Elsevier	https://www.journals.elsevier.com/renewable-energy
2	Environmental Sciences Journals	https://www.omicsonline.org/environmental-sciences-journals

11.0	**Examination Note**

Internal Assessment: 40 Marks

Theoretical aspects as well as relevant sketches should be drawn neatly for questions asked in Internal Assessments

Scheme of Evaluation for Internal Assessment

Internal Assessment test in the same pattern as that of the main examination (Better of the two Tests):40marks.

SCHEME OF EXAMINATION:

- There are five modules two questions from each module
- Student has to answer any five question choosing at least one questions from each module.
- Max. Marks: 60Marks

12.0	**Course Delivery Plan**

Module No.	Lecture No.	Content of Lecture	% of Portion
1		**Basic Introduction to Energy:**	**20**
	1	Energy and power, forms of energy, primary energy sources	
	2	Energy flows, world energy production and consumption	
	4	Key energy trends in India: Demand	
	5	Electricity, Access to modern energy,	
	6	Energy production and trade, Factors affecting India's energy development	
	7	Economy and demographics Policy and institutional framework	
	8	Energy prices and affordability, Social and environmental aspects, Investment	

2		**Energy storage systems, Energy Management, Energy Audit, Economic Analysis**	20
	1	Thermal energy storage methods,	
	2	Energy saving, Thermal energy, storage systems	
	3	Principles of Energy Management, Energy demand.	
	4	Energy estimation, Energy pricing, Energy Audit: Purpose	
	5	Methodology with respect to process Industries,	
	6	Characteristic method employed in Certain Energy Intensive Industries	
	7	Economic Analysis: Scope	
	8	Characterization of an Investment Project	
3		**Environment, Ecosystem:**	20
	1	Environment: Introduction, Multidisciplinary nature of environmental studies- Definition, scope and importance.	
	2	Need for public awareness.	
	3	Ecosystem: Concept, Energy flow Structure and function of an ecosystem.	
	4	Food chains, food webs and ecological pyramids	
	5	Forest ecosystem, Grassland ecosystem,	
	6	Desert ecosystem and Aquatic ecosystems,	
	7	Desert ecosystem and Aquatic ecosystems	
	8	Ecological succession	
4		**Environmental Pollution:**	20
	1	Environmental Pollution definition, Cause and effects	
	2	Control measures of – Air pollution,	
	3	Water pollution, Soil pollution,	
	4	Marine pollution, Noise pollution.	
	5	Thermal pollution and Nuclear hazards ,	
	6	Solid waste Management, Disaster management	
	7	Role of an individual in prevention of pollution	
	8	Pollution case studies	
5		**Social Issues and the Environment:**	20
	1	Climate change, global warming, acid rain, ozone layer depletion	
	2	Nuclear accidents and holocaust. Case Studies.	
	3	Wasteland reclamation, Consumerism and waste products	
	4	Environment Protection Act	
	5	Air (Prevention and Control of Pollution) Act	
	6	Water (Prevention and control of Pollution) Act, Wildlife Protection Act,	
	7	Forest Conservation Act,	
	8	Issues involved in enforcement of environmental legislation	

13.0   Assignments, Pop Quiz, Mini Project, Seminars

Sl. No.	Title	Outcome expected	Allied study	Week No.	Individual / Group activity	Reference: book/website /Paper
1	Assignment 1: University Questions	Students study the Topics and write the Answers. Get practice to solve university questions.	Module 1 syllabus	3	Individual Activity and submission of hard copy.	Book 1 and all the reference book
2	Assignment 2: University Questions	Students study the Topics and write the Answers. Get practice to solve university	Module 2 syllabus	6	Individual Activity and submission of hard copy.	Book 1 and all the reference book

		questions.				
3	Assignment 3: University Questions	Students study the Topics and write the Answers. Get practice to solve university questions.	Module 3 syllabus	9	Individual Activity and submission of hard copy.	Book 1 and all the reference book
4	Assignment 3: University Questions	Students study the Topics and write the Answers. Get practice to solve university questions.	Module 4 syllabus	12	Individual Activity and submission of hard copy.	Book 1 and all the reference book
5	Assignment 3: University Questions	Students study the Topics and write the Answers. Get practice to solve university questions.	Module 5 syllabus	15	Individual Activity and submission of hard copy.	Book 1 and all the reference book

14.0   QUESTION BANK

Sl. No	Questions
Module-I	1. Interpret World Energy Scenario with respect to production and consumption using relevant statistics 2. Define Energy and Power. Differentiate the same. 3. Outline the factors that affect India's energy development. 4. Explain the various key energy trends in India. 5. With relevant statistics, enumerate the primary energy production trend for India.
Module-II	1. Explain in the detail the various phases of energy audit methodology. 2. List the various thermal energy storage methods. Explain sensible heat and latent heat storage methods. 3. Define Energy audit. Explain the need for energy audit. 4. Write a short note on energy demand estimation. 5. Calculate the cost of generation per kWh for a power station having the following data: Installed capacity of the plant = 200 MW , Capital cost = Rs 400 crores ,Rate of interest and depreciation = 12% , Annual cost of fuel, salaries and taxation = Rs 5 crores Load factor = 50% Also estimate the saving in cost per kWh if the annual load factor is raisedto 60%. 6. Explain in the detail the various phases of energy audit methodology 7. Elaborate the benefits of thermal energy storage.
Module-III	1. What is an ecosystem? Discuss forest ecosystem. Explain how conservation of forest can be done. 2. Discuss how oxygen cycle is utilized in the ecosystem. 3. Write a short note on (i) ecological succession (ii) food chain, food web and ecological pyramid. 4. Elaborate how the nitrogen cycle ecosystem operates. 5. Enumerate the utilization of carbon in ecosystem. 6. Describe grassland ecosystem. What are its types? How conservation of grassland can be made 7. Discuss how oxygen cycle is utilized in the ecosystem 8. Define Environment. Mention its scope. Discuss the need for public awareness
Module-IV	1. Discuss briefly the causes, effects and control measures of air pollution. 2. Discuss Solid Waste Management techniques. 3. Elaborate the causes, effects and control measures of (i) Soil Pollution (ii) Noise Pollution (iii) Thermal Pollution 4. Enumerate the role of an individual in prevention of pollution. 5. Enumerate the water pollution causes and its effects. Mention the control measures that can be initiated for mitigating the same. 6. Discuss any two case studies related to pollution of environment in detail. 7. Elaborate the causes, effects and control measures of (i) Soil Pollution (ii) Noise Pollution (iii) Thermal Pollution 8. Discuss Solid Waste Management techniques.
Module-V	1. What is acid rain? What are its effects? 2. Explain the salient features of Air Pollution act. 3. Explain about Environment Impact Assessment (EIA). 4. Discuss (i) Wildlife Protection act (ii) Forest Conservation act 5. Write a note on ozone layer depletion. 6. Express the need for reclaiming the wasteland and its development

7. What are the regulations governing water pollution prevention act?
8. Enumerate the impact of global warming on our mother nature.

15.0   University Result

Year	S, A, B (FCD)	C (FC)	C,D,E (SC)	%age of passing
January / February 2023 (CSE)	41	05	05	100
January / February 2023 (ECE)	25	03	01	100
January / February 2023 (EEE)	01	00	00	100

Prepared by	Checked by		
Dr. M. M. Shivashimpi	Dr.K.M. Akkoli	HOD	Principal

Subject Title	**COMPUTER NETWORKS LABORATORY**		
Subject Code	18ECL76	**IA Marks**	40
Number of Lecture Hrs/ Week	2Hr Tutorial + 2 Hrs Lab	**Exam Marks**	60
		Exam Hours	03
CREDITS – 02			

FACULTY DETAILS:

Name: Prof. B. P. Khot	Designation: Assistant Professor	Experience: 6.8 Years
No. of times course taught: 01	Specialization: Microelectronics and control systems	

1.0   Prerequisite Subjects:

Sl. No	Branch	Semester	Subject
01	Electronics & Communication Engineering	I/II	C-Programming
02	Electronics & Communication Engineering	III	Digital Electronics

2.0   Course Objectives

This course will enable students to:
- Choose suitable tools to model a network and understand the protocols at various OSI reference levels.
- Design a suitable network and simulate using a Network simulator tool.
- Simulate the networking concepts and protocols using C/C++ programming.

- Model the networks for different configurations and analyze the results.

3.0   Course Outcomes

	Course Outcome	**RBT Level**	**Pos**
C406.1	Choose suitable tools to model network and understand the protocols at various OSI reference levels.	L1,L2, L3	PO1- PO6, PO8, PO10- PO12
C406.2	Design a suitable network and simulate using a network simulator tool.	L1,L2, L3	PO1- PO6, PO8, PO10- PO12
C406.3	Analyze the networking concepts and protocols using C/C++ Programming.	L1,L2,L3	PO1- PO6, PO8, PO10- PO12
C406.4	Model the networks for different configurations and analyze the results.	L1,L2,L3	PO1- PO6, PO8, PO10- PO12
Total Hours of instruction		**36**	

4.0   Course Content

PART-A: Simulation experiments using NS2/ NS3/ OPNET/ NCTUns/ NetSim/ QualNet/ Packet Tracer or any other equivalent tool.

1. Implement a point to pint network with four nodes and duplex links between them. Analyze the network performance by setting the queue size and varying the bandwidth.
2. Implement a four node point to point network with links n0-n2, n1-n2 and n2-n3. Apply TCP agent between n0-n3 and UDP between n1-n3. Apply relevant applications over TCP and UDP agents changing the parameter and determine the number of packets sent by TCP/UDP.
3. Implement Ethernet LAN using n (6-10) nodes. Compare the throughput by changing the error rate and data rate.
4. Implement Ethernet LAN using n nodes and assign multiple-traffic to the nodes and obtain congestion window for different sources/ destinations.

5. Implement ESS with transmission nodes in Wireless LAN and obtain the performance parameters.
6. Implementation of Link state routing algorithm.

   PART-B: Implement the following in C/C++

   1. Write a program for a HLDC frame to perform the following.
      i) Bit stuffing
      ii)Character stuffing.
   2. Write a program for distance vector algorithm to find suitable path for transmission.
   3. Implement Dijkstra's algorithm to compute the shortest routing path.
   4. For the given data, use CRC-CCITT polynomial to obtain CRC code. Verify the program for the cases
      a. Without-error
      b. With error
   5. Implementation of Stop and Wait Protocol and Sliding Window Protocol
   6. Write a program for congestion control using leaky bucket algorithm.

5.0 Relevance to future subjects

Sl No	Semester	Subject	Topics
01	VIII	Project work	Projects Based on Computer Networks.
02	VIII	HPCN	Advance Computer Networks.

6.0 Relevance to Real World

SL. No	Real World Mapping
01	Design of networking components like modems, firewalls, routers etc.
02	Model creation for analysis
03	Development of a software application.

7.0 Gap Analysis and Mitigation

Sl. No	Delivery Type	Details
01	Tutorial	Topic: Routing algorithms, understanding simulation software's.
02	NPTEL	C/C++ Programming

8.0 Books Used and Recommended to Students

Text Books

1. Data Communications and Networking, Forouzan, 5th Edition, McGraw Hill,2016 ISBN: 1-25-906475-3.
2. Computer Networks, James J Kurose, Keith W Ross, Pearson Education, 2013, ISBN: 0-273-76896-4
3. Introduction to Data Communication and Networking, Wayarles Tomasi, Pearson Education, 2007, ISBN:0130138282

9.0 Relevant Websites (Reputed Universities and Others) for Notes /Animation / Videos Recommended

Website and Internet Contents References

http://nptel.ac.in/courses/106105081/1   2)   http://searchnetworking.techtarget.com/
3)   https://in.udacity.com/auth?next=/course/computer-networking--ud436

10.0 Magazines/Journals Used and Recommended to Students

Sl.No	Magazines/Journals	website

| 1 | Elsevier | https://www.journals.elsevier.com/computer-networks/ |
| 2 | Sciencedirect | https://www.sciencedirect.com/science/journal/13891286 |

11.0   Examination Note

Scheme of Evaluation for Internal Assessment (40 Marks)
(a) Lab work, Assignment, Technical quiz: 10 Marks.
(b) Internal Assessment test at the end of semester: 30 Marks.

SCHEME OF EXAMINATION:
Execute Two questions
Two questions to be set, one from Part-A and one from Part-B
Student has to answer both full questions.
100marks Marks divided in three parts, Write up 15 marks, Conduction 70 marks & Viva 15marks.

12.0   Course Delivery Plan

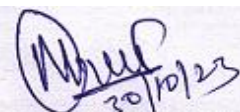| Expt.	Lecture No.	Content	% of Portion
1	1	Implement a point to pint network with four nodes and duplex links between them. Analyze the network performance by setting the queue size and varying the bandwidth.	8.33
2	2		16.66
3	3		25
4	4	Implement Ethernet LAN using n nodes and assign multiple traffic to the nodes and obtain congestion window for different sources/ destinations.	33.33
5	5	Implement a four node point to point network with links n0-n2, n1-n2 and n2-n3. Apply TCP agent between n0-n3 and UDP between n1-n3. Apply relevant applications over TCP and UDP agents changing the parameter and determine the number of packets sent by TCP/UDP.	41.6
6	6	Implement Ethernet LAN using n (6-10) nodes. Compare the throughput by changing the error rate and data rate.	50
7	7	Write a program for a HLDC frame to perform the following. i) Bit stuffingii) Character stuffing.	58.33
8	8	Write a program for distance vector algorithm to find suitable path for transmission.	66.66
9	9	Implement Dijkstra's algorithm to compute the shortest routing path.	75
10	10	For the given data, use CRC-CCITT polynomial to obtain CRC code. Verify the Program for the cases a. Without error b. With error	83.33
11	11	Implementation of Stop and Wait Protocol and Sliding Window Protocol.	91.66
12	12	Write a program for congestion control using leaky bucket algorithm.	100

13.0   VIVA QUESTION BANK

1. What are functions of different layers?
2. Differentiate between TCP/IP Layers and OSI Layers
3. Why header is required?
4. What is the use of adding header and trailer to frames?
5. What is encapsulation?
6. Why fragmentation requires?
7. What is MTU?
8. Which layer imposes MTU?
9. Differentiate between flow control and congestion control.
10. Differentiate between Point-to-Point Connection and End-to-End connections.
11. What are protocols running in different layers?
12. What is Protocol Stack?
13. Differentiate between TCP and UDP.
14. Differentiate between Connectionless and connection oriented connection.

15. Why frame sorting is required?
16. What is meant by subnet?
17. What is meant by Gateway?
18. What is an IP address?
19. What is MAC address?
20. Why IP address is required when we have MAC address?
21. What is meant by port?
22. What are ephemerical port number and well known port numbers?
23. What is a socket?
24. What are the parameters of socket()?
25. Describe bind(), listen(), accept(), connect(), send() and recv().
26. What are system calls? Mention few of them.
27. What is IPC? Name three techniques.
28. Explain mkfifo(), open(), close() with parameters.
29. What is meant by file descriptor?
30. What is meant by traffic shaping?
31. How do you classify congestion control algorithms?
32. Differentiate between Leaky bucket and Token bucket.
33. How do you implement Leaky bucket?
34. How do you generate busty traffic?
35. What is the polynomial used in CRC-CCITT?
36. What are the other error detection algorithms?
37. What is difference between CRC and Hamming code?
38. Why Hamming code is called 7,4 code?
39. What is odd parity and even parity?
40. What is meant by syndrome?
41. What is generator matrix?
42. What are Routing algorithms?
43. How do you classify routing algorithms? Give examples for each.
44. What are drawbacks in distance vector algorithm?
45. How routers update distances to each of its neighbor?
46. How do you overcome count to infinity problem?
47. What is cryptography?
48. How do you classify cryptographic algorithms?
49. What is public key?
50. What is private key?
51. What are key cipher text and plaintext?
52. What is simulation?
53. What are advantages of simulation?

14.0   University Result

Examination	S	A	B	C	D	E	% Passing
Feb 2022	17	12	2	1	2	-	100

Prepared by	Checked by		
Prof. B. P. Khot	Dr. S. S. Ittannavar	HOD	Principal

Subject Title	**VLSI LABORATORY**		
Subject Code	18ECL77	**IA Marks**	40
Number of Lecture Hrs / Week	1 Hr Tutorial + 2 Hrs Lab	**Exam Marks**	100
Total Number of Lecture Hrs	40	**Exam Hours**	03

FACULTY DETAILS:

Name: Prof. S. S. KAMATE	**Designation:** Asst. Professor	**Experience:** T-20.00Yrs, I-00Yrs
No. of times course taught: 02		**Specialization:** Digital Electronics

1.0   Prerequisite Subjects:

Sl. No	Branch	Semester	Subject
01	Electronics & Communication Engineering	III	Digital Electronics
02	Electronics & Communication Engineering	V	Fundamentals of CMOS VLSI
03	Electronics & Communication Engineering	VI	Microelectronics Circuits

2.0   Course Objectives

This course will enable students to:
• Design, model, simulate and verify CMOS digital circuits
• Design layouts and perform physical verification of CMOS digital circuits
• Perform ASIC design flow and understand the process of synthesis, synthesis constraints and evaluating the synthesis reports to obtain optimum gate level netlist
• Perform RTL-GDSII flow and understand the stages in ASIC design.

3.0   Course Outcomes

At the end of the course students will be able to:

	Course Outcome	Cognitive Level	Pos
C407.1	Design and simulate combinational and sequential digital circuits using Verilog HDL	U	PO1 to PO12
C407.2	Understand the Synthesis process of digital circuits using EDA tool	U	PO1 to PO12
C407.3	Perform ASIC design flow and understand the process of synthesis, synthesis constraints and evaluating the synthesis reports to obtain optimum gate level net list	U	PO1 to PO12
C407.4	Design and simulate basic CMOS circuits like inverter, common source amplifier and differential amplifiers.	U	PO1 to PO12
C407.5	Perform RTL-GDSII flow and understand the stages in ASIC design	U	PO1 to PO12
Total Hours of instruction		**40**	

4.0   Course Content

Laboratory Experiments

<div align="center">

Part – A

</div>

Analog Design
Use any VLSI design tools to carry out the experiments, use library files and technology files below 180 nm.

    a) Capture the schematic of CMOS inverter with load capacitance of 0.1pF and set the widths of inverter with Wn = Wp,
    Wn = 2Wp, Wn = Wp/2 and length at selected technology. Carry out the following:

a. Set the input signal to a pulse with rise time, fall time of 1ns and pulse width of 10ns and time periodof 20ns and plot the input voltage and output voltage of designed inverter?

b. From the simulation results compute tpHL, tpLH and td for all three geometrical settings of width?

c. Tabulate the results of delay and find the best geometry for minimum delay for CMOS inverter?

b) Draw layout of inverter with Wp/Wn = 40/20, use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations. Record the observations.

a) Capture the schematic of 2-input CMOS NAND gate having similar delay as that of CMOS inverter computed in experiment 1. Verify the functionality of NAND gate and also find out the delay td for all four possible combinations of input vectors. Table the results. Increase the drive strength to 2X and 4X and tabulate the results.

b)Draw layout of NAND withWp/Wn = 40/20, use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations. Record the observations.

3.a) Capture schematic of Common Source Amplifier with PMOS Current Mirror Load and find its transient response and AC response? Measures the Unity Gain Bandwidth (UGB), amplification factor by varying transistor geometries, study the impact of variation in width to UGB.

1. b) Draw layout of common source amplifier, use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations. Record the observations.

4. a)Capture schematic of two-stage operational amplifier and measure the following:
   a. UGB
   b. dB bandwidth
   c. Gain margin and phase margin with and without coupling capacitance
   d. Use the op-amp in the inverting and non-inverting configuration and verify its functionality
   e. Study the UGB, 3dB bandwidth, gain and power requirement in op-amp by varying the stage wise transistor geometries and record the observations.

4. b) Draw layout of two-stage operational amplifier with minimum transistor width set to 300 (in 180/90/45 nm technology), choose appropriate transistor geometries as per the results obtained in 4.a. Use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations. Record the observations.

Part – B
Digital Design
Carry out the experiments using semicustom design flow or ASIC design flow, use technology library 180/90/45nm and below
Note: The experiments can also be carried out using FPGA design flow, it is required to set appropriate constraints in FPGA advanced synthesis options

1.Write 45erilog code for 4-bit up/down asynchronous reset counter and carry out the following:
a. Verify the functionality using test bench
b.Synthesize the design by setting area and timing constraint. Obtain the gate level netlist, find the critical path and maximum frequency of operation. Record the area requirement in terms of number of cells required and properties of each cell in terms of driving strength, power and area requirement.
c. Perform the above for 32-bit up/down counter and identify the critical path, delay of critical path, and maximum frequency of operation, total number of cells required and total area.

2.Write 45erilog code for 4-bit adder and verify its functionality using test bench. Synthesize the design by setting proper constraints and obtain the net list. From the report generated identify critical path, maximum delay, total number of cells, power requirement and total area required. Change the constraints and obtain optimum synthesis results.

3.Write 45erilog code for UART and carry out the following:
a. Perform functional verification using test bench
b. Synthesize the design targeting suitable library and by setting area and timing constraints
c. For various constrains set, tabulate the area, power and delay for the synthesized netlist
d. Identify the critical path and set the constraints to obtain optimum gate level netlist with suitable constraints

4. Write 45erilog code for 32-bit ALU supporting four logical and four arithmetic operations, use case statement and if statement for ALU behavioral modeling.
a. Perform functional verification using test bench
b. Synthesize the design targeting suitable library by setting area and timing constraints
c. For various constrains set, tabulate the area, power and delay for the synthesized netlist

d. Identify the critical path and set the constraints to obtain optimum gate level netlist with suitable constraints
Compare the synthesis results of ALU modeled using IF and CASE statements.

5. Write 46erilog code for Latch and Flip-flop, Synthesize the design and compare the synthesis report (D, SR, JK).

6. For the synthesized netlist carry out the following for any two above experiments:

a. Floor planning (automatic), identify the placement of pads

b. Placement and Routing, record the parameters such as no. of layers used for routing, flip method for placement of standard cells, placement of standard cells, routes of power and ground, and routing of standard cells c. Physical verification and record the LVS and DRC reports.

d. Perform Back annotation and verify the functionality of the design.

e. Generate GDSII and record the number of masks and its color composition.

5.0 Relevance to future subjects

SL. No	Semester	Subject	Topics
01	VIII	Project work	VLSI based projects
02	Higher	VLSI era	Exposure to the VLSI flow and different types of design.

6.0 Relevance to Real World

SL. No	Real World Mapping
01	VLSI design
02	Miniaturization of different designs to provide more flexibility for the designers

7.0 Gap Analysis and Mitigation

SL. No	Delivery Type	Details
02	NPTEL	VLSI design methods

8.0 Books Used and Recommended to Students

Text Books

1. **"**Basic VLSI Design" by Douglas A. Pucknell and Kamran Eshaghian
2. "CMOS VLSI Design"- A Circuits and Systems Perspective**"-** Neil H.E. Weste, David Harris, Ayan Banerjee, 3rd Edition, Pearson Education.
3. "FPGA Based System Design"-Wayne Wolf, Pearson Education, 2004, Technology and Engineering

9.0 Relevant Websites (Reputed Universities and Others) for Notes /Animation / Videos Recommended

Website and Internet Contents References

2) https://vtu.ac.in
3) http://www.bookspar.com/engineering-vtu
3) http://www.slideshare.net/farohalolya/8086-microprocessor-lab-manual
4) https://www.youtube.com/results?search_query=microprocessor

10.0 Magazines/Journals Used and Recommended to Students

Sl.No	Magazines/Journals	website
1	IEEE	http://ieeexplore.ieee.org/Xplore/home.jsp
2	PC World	http://www.pcworld.com/article/146957/components/article.html

11.0 Examination Note

Scheme of Evaluation for Internal Assessment (20 Marks)

(c) Lab work, Assignment, Technical quiz : 5Marks.

(d) Internal Assessment test Average of two Tests out of Three tests): 15marks.

SCHEME OF EXAMINATION:

Two questions to be set each from Module.

Student has to answer both full questions. 80marks Marks divided in three parts Write up 12marks, Conduction 56marks & Viva 12marks.

12.0   Course Delivery Plan

Experiment	Lecture No.	Content	% of Portion
1.		a) Capture the schematic of CMOS inverter with load capacitance of 0.1pF and set the widths of inverter with Wn = Wp Wn = 2Wp, Wn = Wp/2 and length at selected technology. Carry out the following: a) Set the input signal to a pulse with rise time, fall time of 1ns and pulse width of 10ns and time periodof 20ns and plot the input voltage and output voltage of designed inverter? b) From the simulation results compute tpHL, tpLH and td for all three geometrical settings of width? c). Tabulate the results of delay and find the best geometry for minimum delay for CMOS inverter?	
2.		a) Capture the schematic of 2-input CMOS NAND gate having similar delay as that of CMOS inverter computed in experiment 1. Verify the functionality of NAND gate and also find out the delay td for all four possible combinations of input vectors. Table the results. Increase the drive strength to 2X and 4X and tabulate the results. b)Draw layout of NAND with Wp/Wn = 40/20, use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations. Record the 47erilog47ions.	
3.		a) Capture schematic of Common Source Amplifier with PMOS Current Mirror Load and find its transient response and AC response? Measures the Unity Gain Bandwidth (UGB), amplification factor by varying transistor geometries, study the impact of variation in width to UGB. b) Draw layout of common source amplifier, use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations. Record the observations	
4.		a)Capture schematic of two-stage operational amplifier and measure the following: a. UGB b. dB bandwidth c. Gain margin and phase margin with and without coupling capacitance d. Use the op-amp in the inverting and non-inverting configuration and verify its functionality e. Study the UGB, 3dB bandwidth, gain and power requirement in op-amp by varying the stage wise transistor geometries and record the observations. b) Draw layout of two-stage operational amplifier with minimum transistor width set to 300 (in 180/90/45 nm technology), choose appropriate transistor geometries as per the results obtained in 4.a. Use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations. Record the observations	

		Part – B Digital Design	
1.	5	1.Write 48erilog code for 4-bit up/down asynchronous reset counter and carry out the following: a. Verify the functionality using test bench b. Synthesize the design by setting area and timing constraint. Obtain the gate level netlist, find the critical path and maximum frequency of operation. Record the area requirement in terms of number of cells required and properties of each cell in terms of driving strength, power and area requirement. c. Perform the above for 32-bit up/down counter and identify the critical path, delay of critical path, and maximum frequency of operation, total number of cells required and total area.	
2.	6	2.Write 48erilog code for 4-bit adder and verify its functionality using test bench. Synthesize the design by setting proper constraints and obtain the net list. From the report generated identify critical path, maximum delay, total number of cells, power requirement and total area required. Change the constraints and obtain optimum synthesis results.	
3.	7	Write 48erilog code for UART and carry out the following: a. Perform functional verification using test bench b. Synthesize the design targeting suitable library and by setting area and timing constraints. c. For various constrains set, tabulate the area, power and delay for the synthesized netlist d. Identify the critical path and set the constraints to obtain optimum gate level netlist with suitable constraints	
4.	8	Write 48erilog code for 32-bit ALU supporting four logical and four arithmetic operations, use case statement and if statement for ALU behavioral modeling. a. Perform functional verification using test bench b. Synthesize the design targeting suitable library by setting area and timing constraints c. For various constrains set, tabulate the area, power and delay for the synthesized netlist d. Identify the critical path and set the constraints to obtain optimum gate level netlist with suitable constraints Compare the synthesis results of ALU modeled using IF and CASE statements.	
5.	9	Write 48erilog code for Latch and Flip-flop, Synthesize the design and compare the synthesis report (D, SR, JK).	
6.	10	For the synthesized netlist carry out the following for any two above experiments: a. Floor planning (automatic), identify the placement of pads b. Placement and Routing, record the parameters such as no. of layers used for routing, flip method for placement of standard cells, placement of standard cells, routes of power and ground, and routing of standard cells c. Physical verification and record the LVS and DRC reports d. Perform Back annotation and verify the functionality of the design e. Generate GDSII and record the number of masks and its color composition	

13.0   VIVA BANK

1. The minimum voltage to keep the MOS transistor in on state is known as
2. 'Pinch off of the channel takes place in which region.
3. Which of 'the following equation is true for liner region?
   a)Vds < Vgs –Vt b) Ids> Vgs – Vt c) Vds = Vgs – Vt d) None
4. The oxide layer used in the MOS fabrication is
5. Which of the following Well process is superior?
   a) P-well b)N-well c) Both P-well and N-well d) None
6. What is the advantage of CMOS technology?
7. Transit time is given by-----------------------
8. When the VTC of the CMOS inverter shifts towards left,
9. The demarcation line has to be drawn in--------------------stick diagram.
10. If the value of lambda is 1micrometer then the minimum feature size o the transistor is ?
11. The scaling factor for the Gate capacitance Cg is given by
12. The scaling factor for power-speed product is given by

13. If the gate voltage and the input voltage of the NMOS transistor is 5V and threshold voltage of the transistor is O. 7V, then the output voltage
14. The mobility of the electrons is-------------------- than the holes.
15. As the width of the transistor increases the number of contact cuts----------------
16. Transmission gate is----------------
17. The CMOS schematic diagram of NAND gate consists of-------------------
18. If the size of the transistors in an inverter increases, then the input capacitance
19. The minimum value of the scaling factor in a cascaded inverter circuit to drive large capacitive load
20. In a lambda based rules, the distance between two MI layers is
21. Match the following;

	A		B
a)	CM OS technology	i)	Strong '0'
b)	Bipolar technology	ii)	Strong' 1'
c)	Transmission gate	iii)	High input impedance
d)	PMOS transistor	iv)	Low input impedance
e)	NMOS transistor	v)	Bi-directional switch

22. What is rise time & fall time of Inverter.
23. Define Symmetrical inverter.
24. What is the value of e in case of load handling by invereter.
25. What is Pass transistor?
26. Give the disadvantage of Pass transistor.
27 What is the advantage of Transmission gate over Pass transistor.
28. What is a Flip-flop?
29. What is a master slave Flip-flop?
30. What is a race-around condition?
31. Differentiate Serial & Parallel adder.
32. What is a DAC?
33. Name different types of DAC's.
34. What is a ADC
35. Name different types of ADC's.
36. What is SAR?
37. Explain the working of SAR.
38. What is a Buffer?
39. What is a counter?
40. What is synchronous counter?
41. What is synchronous counter?
42. What is RC extraction?
43. What is Back annotation?
44. What do you mean by DC-analysis?
45. What do you mean by AC-analysis?
46. What is the Gain of common drain amplifier?
47. How the common source amplifier is formed.
48. What is speed Vs area tradeoff?
49. What is the resolution of 4-bit ADC with V reference= 5V
50. What is DRC & ERC.
51. Explain design abstraction for FPGAs.
52. Explain FPGA architecture.
53.Explain in detail the Generic Structure of an FPGA fabric.

14.0 University Result

Examination	FCD	FC	SC	% Passing
Feb 2022	31	03	1	100
Jan 2023	28	-	-	96.5

Prepared by	Checked by		
Prof. S. S. Kamate	Prof. S. S. Kamate	HOD	Principal