INSTITUTE VISION

"To be a preferred institution in Engineering Education by achieving excellence in teaching and research and to remain as a source of pride for its commitment to holistic development of individual and society"

INSTITUTE MISSION

"To continuously strive for the overall development of students, educating them in a state of the art infrastructure, by retaining the best practices, people and inspire them to imbibe real time problem solving skills, leadership qualities, human values and societal commitments, so that they emerge as competent professionals"

DEPARTMENTAL VISION

“To be the centre of excellence in providing education in the field of Electronics and Communication Engineering to produce technically competent and socially responsible engineering graduates.”

DEPARTMENTAL MISSION

“Educating students to prepare them for professional competencies in the broader areas of the Electronics and Communication Engineering field by inculcating analytical skills, research abilities and encouraging culture of continuous learning for solving real time problems using modern tool”.

PROGRAM EDUCATIONAL OBJECTIVES (PEOs):

PEO1:

Acquire core competence in Applied Science, Mathematics, and Electronics and Communication Engineering fundamentals to excel in professional carrier and higher study.

PEO2:

Design, Demonstrate and Analyze the Electronic Systems which are useful to society.

PEO3:

Maintain Professional and Ethical values, Employability skills, Multidisciplinary approach and an Ability to realize Engineering issues to broader social contest by engaging in lifelong learning.

PROGRAM SPECIFIC OUTCOMES(PSOS)

The graduates will be able to:

PSO1:

An ability to understand the concepts of Basic Electronics and Communication Engineering and to apply them to various areas like Signal Processing, VLSI, Embedded Systems, Communication Systems and Digital & Analog Devices

PSO2:

An ability to solve complex Electronics and Communication Engineering problems, using latest hardware and software tools, along with analytical skills to arrive at cost effective and appropriate solutions

PROGRAM OUTCOMES(POs):

1. **Engineering knowledge**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
2. **Problem analysis**: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
3. **Design/development of solutions**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

4. **Conduct investigations of complex problems**: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
5. **Modern tool usage**: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
6. **The engineer and society**: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
7. **Environment and sustainability**: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
8. **Ethics**: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
9. **Individual and team work**: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
10. **Communication**: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
11. **Project management and finance**: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

12. **Life-long learning**: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

STUDENT HELP DESK

Sr.No	Name of the faculty	Activities
1	Dr.M.C.Sarasamba	GATE / Preplacement Coaching
		Students Mentor
		Module Coordinator
		Research Center Coordinator
		Dept. NAAC Criteria Sub Coordinator
		NBA Criteria Coordinator
2	Prof. S. S. Malaj	GATE / Preplacement Coaching
		Adv.Comm. Lab In charge
		Students Mentor
		Dept. NAAC Criteria Sub Coordinator
		NBA Criteria Coordinator
		NIRF Coordinator
3	Prof. S. S. Kamate	GATE / Preplacement Coaching
		VLSI Lab In charge
		Students Mentor
		Module Coordinator
		IEEE Coordinator/ IA Cordinator
		Dept. NAAC Criteria Sub Coordinator
		Project Coordinator
		NBA Criteria Coordinator
4	Prof. D. M. Kumbhar	GATE / Preplacement Coaching
		AC Lab In charge
		Students Mentor
		Dept. Association Coordinator
		Class Teacher
		IIIC Coordinator
		Dept. NAAC Criteria Sub Coordinator
		NBA Criteria Coordinator
		AICTE Activity Coordinator
		Dept. ED Cell Coordinator
5	Prof. S. S. Patil	GATE / Preplacement Coaching
		ARM & ES Lab In charge
		Students Mentor
		Class Teacher
		NBA Criteria Coordinator
		AICTE Activity Coordinator
		Admission Coordinator
		Module Coordinator

Sr.No	Name of the faculty	Activities
6	Prof. D. B. Madihalli	GATE / Preplacement Coaching
		DSD Lab In charge
		Students Mentor
		NBA Coordinator
		News & Publicity Coordinator
		NBA Criteria Coordinator
		Website Coordinator
		VTU LIC Coordinator
7	Prof. P. V. Patil	GATE / Preplacement Coaching
		HDL Lab In charge
		Students Mentor
		NBA Criteria Coordinator
		T&P Cell Coordinator
		Alumni Coordinator
8	Dr. S. S. Ittannavar	GATE / Preplacement Coaching
		BSP /DSP Lab In charge
		Students Mentor
		Module Coordinator
		News Letter / Technical Magazine
		AICTE Coordinator
9	Prof. B. P. Khot	GATE / Preplacement Coaching
		CN/MC Lab In charge
		Students Mentor
		Dept. Time Table Coordinator & Meeting Coordinator
		Class Teacher
		NBA Criteria Coordinator
		Dept T&P Cell Coordinator
		AICTE Activity Coordinator
10	Prof. S.R.Mallurmath	EMS Coordinator
		GATE / Preplacement Coaching
		Students Mentor
		AICTE Activity Coordinator
		NBA Criteria Coordinator
11	Prof. K.S.Patil	GATE / Preplacement Coaching
		Students Mentor
		AICTE Activity Coordinator
		NBA Criteria Coordinator

CONTENTS

FACULTY POSITION

S.N.	Category	No. in position	Average experience
1	Teaching faculty.	09	17.00Y
2	Technical supporting staff.	04	22.08Y
3	Helper staff	02	22.00Y

MAJOR LABORATORIES

S. N.	Name of the laboratory	Area in Sq. Mtrs	Amount Invested in Lakhs	S. N.	Name of the laboratory	Area in Sq. Mtrs	Amount Invested in Lakhs
1	Digital Electronics Lab	71	1.54	5	VLSI Lab	71	35.51
2	Analog Electronics (ED &I) Lab	92	8.24	6	Project Lab	95	--
3	Advanced Commn & Commn + LIC Lab	92	20.50	7	Research/E-Yantra/DSP & C.N.Lab	71	16.49
4	HDL/MC / EMD Lab	71	19.57	8	Power Electronics Lab	--	4.86
Total Investment In The Department					**Rs. 95.31 Lacs**		

FACULTY DETAILS

TEACHING FACULTY

S.N.	Name and Designation	Qualification	Specialization	Professional Membership	Teaching Exp.	Contact No.
1	Prof. M.C.Sarasamba	Ph.D	E&C	LMISTE	18Y.05M	9480714746
2	Assoc.Prof.S .S .Ittannavar	Ph.D	DSP	LMISTE	10Y.05M	9964299498
3	Asst.Prof. S. S. Malaj	M.E.	E & TC	LMISTE	26Y.01M	9731795803
4	Asst.Prof.S.S.Kamate	M.Tech	Digital Electronics	LMISTE	20Y.06M	9008696825
5	Asst.Prof. D.M. Kumbhar	M.Tech	Electronics	LMISTE	19Y.04M	09373609880
6	Asst.Prof. Sachin .S. Patil	M.Tech	VLSI & Embedded	LMISTE	19Y.02M	9448102010
7	Asst.Prof .D.B. Madihalli	M.Tech	Industrial Electronics	LMISTE	16Y.01M	9902854324
8	Asst.Prof.P.V.Patil	M.Tech	VLSI & Embedded	LMISTE	10Y.10M	9731104059
9	Asst.Prof. B. P. Khot	M.Tech	Microelectronics & Control Systems	LMISTE	7Y.05M	9964019501
10	Asst.Prof. S.R.Mallurmath	M.Tech	Industrial Electronics	LMISTE	10Y.04M	7259865769
11	Asst.Prof.K.S.Patil	M.Tech	VLSI	LMISTE	29Y.00M	9902682781

TECHNICAL SUPPORTING STAFF

S.N.	Name	Qualification	Experience (in years)
1.	Sri. P. S. Desai	DEC	23Y-.01M
2.	Sri. V. V. Guruwodeyar	DEC	31Y-08 M
3.	Sri.M.A.Attar	DEC	13Y-03M

VISVESVARAYATECHNOLOGICALUNIVERSITY,BELAGAVI

B.E. in Electronics and Communication Engineering Scheme of Teaching and Examinations2022

Outcome Based Education(OBE)and Choice Based Credit System(CBCS)

(Effectivefromtheacademicyear2023-24)

III SEMESTER

Sl. No	Course	Course Code	Course Title	Teaching Department(TD) and Question Paper Setting Board(PSB)	Teaching Hours /Week				Examination				Credits
					Theoy Lectue	Tutorial	Practical/ Drawing		Durationi nhours	CIE Marks	SEE Marks	Total Marks	
					L	T	P	S					
1	PCC	BMATEC301	AV Mathematics-III for EC Engineering	TD-Maths PSB-Maths	3	0	0		03	50	50	100	3
2	IPCC	BEC302	Digital System Design using Verilog	TD:ECE PSB: ECE	3	0	2		03	50	50	100	4
3	IPCC	BEC303	Electronic Principles and Circuits	TD:ECE PSB:ECE	3	0	2		03	50	50	100	4
4	PCC	BEC304	Network Analysis	TD:E C EPSB: ECE	3	0	0		03	50	50	100	3
5	PCCL	BECL305	Analog and Digital Systems Design Lab	TD:ECE PSB: ECE	0	0	2		03	50	50	100	1
6	ESC	BXX306x	ESC/ETC/PLC	TD: PSB:	3	0	0		03	50	50	100	3
7	UHV	BSCK307	Social Connect and Responsibility	Any Department	0	0	2		01	100	---	100	1
8	AEC/SEC	BXX358x	Ability Enhancement Course/Skill Enhancement Course–III		If the course is a Theory: 1 0 0 / If a course is a laboratory: 0 0 2				01 / 02	50	50	100	1
9	MC	BNSK359	National Service Scheme(NSS)	NSS coordinator	0	0	2			100	---	100	0
		BPEK359	Physical Education(PE)(Sports and Athletics)	Physical Education Director									
		BYOK359	Yoga	Yoga Teacher									
									Total	**550**	**350**	**900**	**20**

PCC:ProfessionalCoreCourse,**PCCL**:ProfessionalCoreCourselaboratory,**UHV**:UniversalHumanValueCourse,**MC**:MandatoryCourse(Non-credit),**AEC**:Ability EnhancementCourse,**SEC**:SkillEnhancementCourse,**L:**Lecture,**T**:Tutorial,**P**:Practical**S=SDA**:SkillDevelopmentActivity,**CIE**:ContinuousInternalEvaluation,**SEE**: SemesterEndEvaluation.K:Thisletterinthecoursecodeindicatescommontoallthestreamofengineering.ESC:EngineeringScience Course, ETC: Emerging

Technology Course ,PLC: Programming Language Course

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Engineering Science Course(ESC/ETC/PLC)			
BEC306A	Electronic Devices	BEC306C	Computer Organization and Architecture
BEC306B	Sensors and Instrumentation	BEC306D	Applied Numerical Methods for ECE Engineers
Ability Enhancement Course–III			
BEC358A	LAB VIEW programming	BEC358C	C++Basics
BEC358B	MATLAB Programming	BEC358D	IOT for Smart Infrastructure

Professional Core Course (IPCC): Refers to Professional Core Course Theory Integrated with practical's of the same course. Credit for IPCC can be 04 and its Teaching– Learning hours (L : T : P) can be considered as(3 : 0 : 2) or (2 : 2 : 2). The theory part of the IPCC shall be evaluated both by CIE and SEE. The practical part shall be evaluated by only CIE (no SEE).However, questions from the practical part of IPCC shall be included in the SEE question paper. For more details, the regulation governing the Degree of Bachelor of Engineering/Technology (B.E./B.Tech.)2022-23maypleasebereferred.

National Service Scheme /Physical Education/Yoga: All students have to register for any one of the courses namely National Service Scheme (NSS),Physical Education (PE)(SportsandAthletics),andYoga(YOG)withtheconcernedcoordinatorofthecourseduringthefirstweekofIIIsemesters.ActivitiesshallbecarriedoutbetweenIII semester to the VI semester (for 4 semesters). Successful completion of the registered course and requisite CIE score is mandatory for the award of the degree. The eventsshallbeappropriatelyscheduledbythecollegesandthesameshallbereflectedinthecalendarpreparedfortheNSS, PE,andYogaactivities.Thesecoursesshall
Not be considered for vertical progression as well as for the calculation of SGPA and CGPA ,but completion of the course is mandatory for the award of degree.

S J P N Trust's
Hirasugar Institute of Technology, Nidasoshi.
Approved by AICTE, New Delhi, Permanently Affiliated to VTU, Belagavi
Recognized under 2(f) & 12B of UGC Act, 1956
Accredited at 'A' Grade by NAAC & Programmes Accredited by NBA:CSE & ECE

IQAC
File I-11
AY:2023-24 (Odd)
Rev: 01

REVISED ACADEMIC CALENDAR OF EVENTS-02 (CoE-02) OF III & V SEM FOR THE AY: 2023-24

Ref:
1. VTU CoE Notification No.: VTU/BGM/ACA/2023-24/3252, Dated 30th Sept. 2023
2. VTU CoE Notification No.: VTU/BGM/ACA/2023-24/2668, Dated 25th Aug. 2023
3. VTU Revised CoE Notification No.: VTU/BGM/ACA/2023-24/3681, Dated 20th Oct. 2023

Calendar

October -2023

Sun	Mon	Tue	Wed	Thu	Fri	Sat
1	2	3	4	5	6	7
8	9	10	11	12	13	14
15	16	17	18	19	20	21
22	23	24	25	26	27	28
29	30	31				

November -2023

Sun	Mon	Tue	Wed	Thu	Fri	Sat
			1	2	3	4
5	6	7	8	9	10	11
12	13	14	15	16	17	18
19	20	21	22	23	24	25
26	27	28	29	30		

December -2023

Sun	Mon	Tue	Wed	Thu	Fri	Sat
					1	2
3	4	5	6	7	8	9
10	11	12	13	14	15	16
17	18	19	20	21	22	23
24	25	26	27	28	29	30
31						

January -2024

Sun	Mon	Tue	Wed	Thu	Fri	Sat
	1	2	3	4	5	6
7	8	9	10	11	12	13
14	15	16	17	18	19	20
21	22	23	24	25	26	27
28	29	30	31			

February -2024

Sun	Mon	Tue	Wed	Thu	Fri	Sat
				1	2	3
4	5	6	7	8	9	10
11	12	13	14	15	16	17
18	19	20	21	22	23	24
25	26	27	28	29		

March -2024

Sun	Mon	Tue	Wed	Thu	Fri	Sat
31					1	2
3	4	5	6	7	8	9
10	11	12	13	14	15	16
17	18	19	20	21	22	23
24	25	26	27	28	29	30

Date	Events & Holidays
28th Sept.2023	GH: Eid-Milad
2nd Oct. 2023	GH: Gandhi Jayanthi
14th Oct.2023	GH: Mahalaya Amavasya
17th Oct. 2023	Fresher's day: A Welcome Function for 1st year students
23rd -24th Oct. 2023	GH: Mahanavami, Ayudhapooja, Vijayadasami
25th Oct to 23rd Nov. 2023	V Sem Innovation/Entrepreneurship/Societal Internship (2021 Scheme)
28th Oct. 2023	Valmiki Jayanti
1st Nov. 2023	GH: Kannada Rajyothsava
14th Nov. 2023	GH: Balipadyami, Deepavali
15th Nov. 2023	Commencement of III Semester Classes
25th Nov. 2023	Commencement of V Semester Classes
30th Nov. 2023	GH: Kanakadasa Jayanti
8th-9th Dec. 2023	International Conference
25th Dec. 2023	GH: Christmas
21st-23rd Dec.2023	1st IA Test for III & V Semesters
23rd Dec. 2023	1st Feedback on Teaching-Learning (III & V Sems.)
27th Dec. 2023	Display of 1st IA Test Marks (III & V Sems.)
12th Jan. 2024	National Youth Day
15th Jan. 2024	GH: Uttarayana Punya Kala Sankrathi (Tentative)
19th -20th Jan. 2024	Lab IA Test-I (III Sem. 2022 Scheme & V Sem. 2021 Scheme)
22nd-24th Jan. 2024	2nd IA Test for III & V Semesters
24th Jan. 2024	2nd Feedback on Teaching-Learning (III & V Sems.)
26th Jan. 2024	Republic Day
29th Jan. 2024	Display of 2nd IA Test Marks (III & V Sems.)
9th -10th Feb. 2024	Lab IA Test-II (III Sem. 2022 Scheme)
15th-17th Feb. 2024	3rd IA Test for III Semester
19th Feb. 2024	Display of 3rd IA Test Marks (III Sem.)
20th Feb. 2024	Last Working Day of the III Semester
21st -29th Feb. 2024	III Semester VTU Practical Examination
04th -23rd March. 2024	III Semester VTU Theory Exams (SEE)
1st & 2nd March 2024	Lab IA Test-II (V Sem. 2021 Scheme)
5th -7th March 2024	3rd IA Test for V Sem
9th March 2024	Display of 3rd IA Test Marks
8th March 2024	GH: Mahashivaratri & International Women's Day
9th March 2024	Last Working Day of the V Semester
11th-20th March. 2024	V Semester Practical Examination
1st April 2024	Commencement of IV Semester
22nd March-20th April 24	V Semester VTU Theory Exams (SEE)
22nd April 2024	Commencement of VI Semester
29th March 2024	GH: Good Friday

GH: General Holiday, LH: Local Holiday

Dr.S.N.Topannavar
IQAC Coordinator & Dean (Academics)

Dr.S.C.Kamate
Principal

Nidasoshi, Taq: Hukkeri, Dist: Belagavi, Karnataka - 591 236
Phone:+91-8333-278887, Fax:278886, Web:www.hsit.ac.in, Mail:principal@hsit.ac.in

Subject Title	**AV Mathematics-III for EC Engineering**		
Subject Code	**BMATEC301**	**IA Marks**	50
Number of Lecture Hrs /	03	**Exam Marks**	50
Total Number of Lecture	40	**Exam Hours**	03
		CREDITS – 03	

FACULTY DETAILS:		
Name: Dr. S. L. Patil	Designation: Asst. Professor	Experience: 14.5
No. of times course taught: 01	**Specialization:** Mathematics	

1.0 Prerequisite Subjects:

Sl. No	Branch	Semester	Subject
01	Electronics and Communication Engineering	II	Advanced Calculus & Numerical Methods

2.0 Course Objectives

Course Learning Objectives:

- To have an insight into Fourier series, Fourier transforms, Difference equations and Z- Transforms.
- Learn to use the Fourier series to represent periodical physical phenomena in engineering analysis and to Enable the student to express non-periodic functions to periodic functions using the Fourier series and Fourier Transforms. Analyze signals in terms of Fourier transforms.
- Develop the knowledge of solving differential equations and their applications in ECE.
- To find the association between attributes and the correlation between two variables

3.0 Course Outcomes

Having successfully completed this course, the student will be able to

Course Code	Course Outcome	RBTL	POs
C201.1	Demonstrate the Fourier series to study the behavior of periodic functions and their applications in system communications, digital signal processing, and	L1,L2,L3	1,2,3, 12
C201.2	To use Fourier transforms to analyze problems involving continuous-time signals	L1,L2,L3	1,2,3,12
C201.3	To apply Z-Transform techniques to solve difference equations	L1,L2,L3	1,2,3,12
C201.4	Understand that physical systems can be described by differential equations and solve such equations	L1,L2,L3	1,2,3,12
C201.5	Make use of correlation and regression analysis to fit a suitable mathematical model for statistical data	L1,L2,L3	1,2,3,12
Total Hours of instruction		**40**	

4.0 Course Content

Module-1: Fourier series and practical harmonic analysis:
Periodic functions, Dirichlet's condition. Fourier series expansion of functions with period 2π and with arbitrary period: periodic rectangular wave, Half-wave rectifier, rectangular pulse, Saw tooth wave. Half-range Fourier series. Triangle and half range expansions, Practical harmonic analysis, variation of periodic current. **(8 hours)**

Module -2: Infinite Fourier Transforms:
Infinite Fourier transforms, Fourier cosine and sine transforms, Inverse Fourier transforms, Inverse Fourier cosine and sine transforms, discrete Fourier transform (DFT), Fast Fourier transform (FFT). **(8 hours)**

Module -3: Z Transforms
Definition, Z-transforms of basic sequences and standard functions. Properties: Linearity, scaling, first and second shifting, multiplication by n. Initial and final value theorem. Inverse Z- transforms. Application to difference equations. **(8 hours)**

Module -4: Ordinary Differential Equations of Higher Order
Higher-order linear ODEs with constant coefficients - Inverse differential operator, problems. Linear differential equations with variable Coefficients-Cauchy's and Legendre's differential equations– Problems. Application of linear differential equations to L-C circuit and L-C-R circuit. **(8 hours)**

Module -5: Curve fitting, Correlation, and Regressions
Principles of least squares, Curve fitting by the method of least squares in the form $y = a + bx$, $y = a + bx + cx^2$, and $y = ax^b$. Correlation, Coefficient of correlation, Lines of regression, Angle between regression lines, standard error of estimate, rank correlation.

5.0 Relevance to future subjects

Sl. No.	Semester	Subject	Topics
01	Common to all	Common to all engineering Subjects	Signal and Analysis, Field Theory, Thermodynamics, Fluid Dynamics etc

6.0 Relevance to Real World

Sl. No	Real World Mapping
01	Fourier series is that very little information is lost from the signal during the transformation. The Fourier transform maintains information on amplitude, harmonics, and phase and uses all parts of the waveform to translate the signal into the frequency domain.
02	Z-transform is used in Image processing and Filters, p-n junction, High-pass, low-pass, band-pass filters. Blur removal etc.

7.0 Gap Analysis and Mitigation

Sl. No	Delivery Type	Details
01	Tutorial	Topic: Differential equations

8.0 Books Used and Recommended to Students

Text Books

1. B.S. Grewal: "Higher Engineering Mathematics", 44th Edition 2021, Khanna Publishers.
2. E. Kreyszig: "Advanced Engineering Mathematics", John Wiley & Sons, 10th Ed., 2018.

Reference Books

1. V. Ramana: "Higher Engineering Mathematics" McGraw-Hill Education, 11th Ed.2017
2. Srimanta Pal & Subodh C. Bhunia: "Engineering Mathematics" Oxford University Press,3rd, 2016.
3. N.P Bali and Manish Goyal: "A textbook of Engineering Mathematics" Laxmi Publications, 10th Ed., 2016.
4. C. Ray Wylie, Louis C. Barrett: "Advanced Engineering Mathematics" McGraw – Hill Book Co. New York, 6th Ed., 2017.
5. Gupta C.B, Sing S.R and Mukesh Kumar: "Engineering Mathematic for Semester I and II", McGraw Hill Education (India) Pvt. Ltd 2015.
6. H. K. Dass and Er. Rajnish Verma: "Higher Engineering Mathematics" S. Chand Publication 3rd Ed., 2014.
7. James Stewart: "Calculus" Cengage publications,7thEd., 2019.

9.0 Relevant Websites (Reputed Universities and Others) for Notes/Animation/Videos Recommended

Website and Internet Contents References

Web links and Video Lectures:

1. http://nptel.ac.in/courses.php?disciplineID=111
2. http://www.class-central.com/subject/math(MOOCs)
3. http://academicearth.org/
4. VTU Edusat Programme
5. VTU e-Shikshana Program
6. http://www.bookstreet.in.

10.0 Magazines/Journals Used and Recommended to Students

Sl. No	Magazines/Journals	website
1	+ Plus Magazine	https://plus.maths.org/issue44.
2	Mathematics Magazine	www.mathematicsmagazine.com

11.0 Examination Note

Assessment Details (both CIE and SEE)

The weight age of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. There are 25 marks for the CIE's Assignment component and 25 for the IA Test component.

2. Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the Coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks.

3. Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)

4. The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks. Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled time table, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks

12.0 Course Delivery Plan

Module No.	Lecture No.	Content of Lecturer	% of Portion
1	1	Introduction, Periodic functions, Dirichlet's conditions	20
	2	Fourier series of periodic functions of period 2π and with arbitrary period	
	3	Periodic rectangular wave, Half-wave rectifier	
	4	Rectangular pulse, Saw tooth wave	
	5	Half-range Fourier series	
	6	Triangle and half range expansions	
	7	Practical harmonic analysis	
	8	Variation of periodic current	
2	9	Introduction, Infinite Fourier transform	20
	10	Fourier sine transforms & Problems	
	11	Fourier cosine transforms & Problems	
	12	Inverse Fourier transforms & Problems	
	13	Inverse Fourier cosine and sine transforms	
	14	Problems	
	15	discrete Fourier transform (DFT)	
	16	Fast Fourier transform (FFT).	

3	17	Definition, Z-transforms of basic sequences & Standard z-transforms	20
	18	Properties: Linearity	
	19	Scaling property	
	20	First and second shifting property	
	21	Multiplication by n property	
	22	Initial value and final value theorems.	
	23	Inverse z-transform & Problems	
	24	Application to difference equations.	
4	25	Higher-order linear ODEs with constant coefficients	20
	26	Inverse differential operator	
	27	Problems	
	28	Linear differential equations with variable Coefficients-Cauchy's	
	29	Problems	
	30	Legendre's differential equations	
	31	Problems	
	32	Application of linear differential equations to L-C circuit and L-C-R circuit.	
5	33	Principles of least squares,	20
	34	Curve fitting by the method of least squares in the form $y = a + bx$	
	35	Curve fitting of the form $y = a + bx + cx^2$	
	36	Curve fitting of the form $y = ax^b$	
	37	Correlation, Coefficient of correlation	
	38	Lines of regression, Angle between regression lines	
	39	Standard error of estimate,	
	40	Rank correlation	

13.0 Assignments

Sl. No.	Title	Outcome expected	Allied study	Week No.	Individual / Group activity	Reference: book/website /Paper
1	Assignment 1: University Questions	Students study the Topics and write the Answers. Get practice to solve university questions.	Module 1,2&3 of the syllabus	6	Individual Activity.	Book 1, of the reference list. Website of the Reference list
2	Assignment 2: University Questions	Students study the Topics and write the Answers. Get practice to solve university questions.	Module 4, &5 of the syllabus	10	Individual Activity.	Book 1, 2 of the reference list. Website of the Reference list

14.0 QUESTION BANK

Module-1: Fourier series and practical harmonic analysis:

1. Obtain a Fourier series to represent e^{-ax} from $(-\pi, x)$
2. Expand $f(x) = x \sin x, 0 < x < 2$, in a Fourier series**.**
3. For a function $f(x)$ defined by $f(x) = |x|, -\pi < x < \pi,$ obtain a Fourier series. Deduce that $\frac{1}{1^2} + \frac{1}{3^2} + \frac{1}{5^2} + \frac{1}{7^2} = \frac{\pi^2}{8}$
4. Find the Fourier series for the function $f(x) = \frac{\pi - x}{2}$ in $(0, 2\pi)$. Hence deduce that $\frac{\pi}{4} = 1 - \frac{1}{3} + \frac{1}{5} - - -$

5. Find the Fourier series to represent $f(x) = x + x^2$ from $x = -\pi$ to $x = \pi$ and deduce that $\frac{1}{1^2} - \frac{1}{2^2} + \frac{1}{3^2} - \frac{1}{4^2} = \frac{\pi^2}{12}$
6. Expand $f(x) = e^{-x}$ as a Fourier series in the interval $(-l, l)$
7. Obtain Fourier series for the function

$f(x) = \begin{cases} \pi x, & 0 \le x \le 1 \\ \pi(2-x), & 1 \le x \le 2 \end{cases}$ and deduce that $\frac{1}{1^2} + \frac{1}{3^2} + \frac{1}{5^2} + \frac{1}{7^2}$-------

8. Develop f(x) in Fourier series in the interval (-2, 2) if $f(x) = \begin{cases} 0, & -2 < x < 0 \\ 1, & 0 < x < 2 \end{cases}$
9. Find the half range cosine series for the function $f(x) = x^2$ in the range $0 \le x \le 1$
10. Find the complex form of the Fourier series of the periodic function $f(x) = \cos ax$, in $-\pi < x < \pi$.
11. The following table gives the variation of periodic current over a period

t sec	0	T/6	T/3	T/2	2T/3	5T/6	T
A amp	1.98	1.30	1.05	1.30	-0.88	-0.25	1.98

Show that there is a direct current part of 0.75 amp in the variable current and obtain the amplitude of the first harmonic.

12. Obtain the Fourier expansion of $f(x) = 2x - x^2$ in $0 \le x \le 2$
13. Obtain the constant term and the coefficient of the first sine and cosine terms in the Fourier expansion of y as given below.

x	0	1	2	3	4	5
y	9	18	24	28	26	20

Module-2: Infinite Fourier Transforms:

1. Find the Fourier transform of $f(x) = \begin{cases} 1, & |x| < 1 \\ 0, & |x| < 1 \end{cases}$. Hence evaluate $\int_0^\infty \frac{\sin x}{x} dx$
2. Find the Fourier transform of the function $f(x) = \begin{cases} x, & |x| \le \\ 0, & |x| > \alpha \end{cases}$. Where α is a positive constant?
3. Find the Fourier transform of $\cos ax^2$
4. Find the Fourier sine transform of e^{-ax}/x
5. Find the Fourier sine and cosine transform of $f(x) = \begin{cases} 1, & 0 \le x < a \\ 0, & x \ge a \end{cases}$
6. Find the finite Fourier sine and cosine transform of $f(x) = 2x, \quad 0 < x < 4$.
7. Find the cosine transform of $f(x) = \frac{1}{1+x^2}$
8. Find the Fourier sine transform of $e^{-|x|}$
9. Find the Fourier transform of $f(x) = \begin{cases} a^2 - x^2, & |x| < a \\ 0, & |x| > a \end{cases}$ and Evaluate $\int_0^\infty \frac{\sin x - x\cos x}{x^3} dx$.
10. Find the Fourier sine transform of $f(x) = \frac{e^{-ax}}{x}$, $a > 0$.
11. Find the Fourier cosine transform of $(x) = \begin{cases} x, & 0 < x < 1 \\ 2 - x, & 1 < x < 2 \\ 0, & x > 2 \end{cases}$.
12. Find the Fourier transform of $f(x) = e^{-|x|}$ and Evaluate $\int_0^\infty \frac{x \sin mx}{1+x^2} dx$.

Module-3: Z Transform

1. P.T. $z_T(n^2) = \frac{z^2+z}{(z-1)^3}$
2. P.T. $z_T(n^3) = \frac{z^3+4z^2+2}{(z-1)^4}$
3. P.T. $z_T(cos\theta) = \frac{z(z-cos\theta)}{z^2-2zcos\theta+1}$
4. P.T. $z_T(sin\theta) = \frac{(zsin\theta)}{z^2-2zcos\theta+1}$
5. P.T. $z_T(a^n cosn\theta) = \frac{z(z-acos\theta)}{z^2-2azcos\theta+a^2}$
6. Find the Z-transform of $cos\ hn\theta$ & $sinhn\theta$.
7. Find the Z-transform of $(n+1)^2$
8. Using the inversion integral method find the inverse Z-transform of $\frac{3z}{(z-1)(z-2)}$
9. Solve $y_{n+2} + 6y_{n+1} + 9y_n = 2^n$ $y_{n+2} + 6y_{n+1} + 9y_n = 2^n$ with $y_0 = y_n = 0$ using Z-transform
10. Solve the difference equation $y_{n+2} + 2y_{n+1} + y_n = n$ with $y_0 = y_n = 0$ using Z-Transform.
11. Obtain the z-transform of $cos\ n\theta$ and $sin\ n\theta$
12. Find the Inverse z-transform of $\frac{2z^2+3z}{(z+2)(z-4)}$.
13. If $\bar{u}(z) = \frac{2z^2+3z+12}{(z-1)^4}$, find the value of $u_0,\ u_1,\ u_2,\ u_3$.
14. Solve the difference equation $u_{n+2} + 6u_{n+1} + 9u_n = 2^n$, $u_0 = u_1 = 0$.

Module-4: Ordinary Differential Equations of Higher Order

1. Solve $\frac{d^2y}{dx^2} - 2\frac{dy}{dx} = e^x sinx$
2. Solve $\frac{d^2y}{dx^2} + y = \frac{1}{1+sinx}$
3. Solve $x\frac{d^2y}{dx^2} - 2\frac{y}{x} = \frac{x+1}{x2}$.
4. Solve $x^3\frac{d^3y}{dx^3} + 3x^2\frac{d^2y}{dx^2} + x\frac{dy}{dx} + 8y = 65cos(logx)$
5. Solve $x^3\frac{d^3y}{dx^3} + 2x^2\frac{d^2y}{dx^2} + 2y = 10(\frac{x+1}{x})$.
6. Solve $x^2\frac{d^2y}{dx^2} + x\frac{dy}{dx} + y = logx\ sin(logx)$
7. Solve $(2x+3)^2\frac{d^2y}{dx^2} - (2x+3)\frac{dy}{dx} - 12y = 6x$
8. Solve $(1+x)^2\frac{d^2y}{dx^2} + (1+x)\frac{dy}{dx} + y = sin[2log(1+x)]$.
9. Solve: $\frac{d^2y}{dx^2} + 4\frac{dy}{dx} + 5y = -2coshx$. Also find y when $y = 0, \frac{dy}{dx} = 1\ at\ x = 0$.
10. Solve: $\frac{d^3y}{dx^3} + 2\frac{d^2y}{dx^2} + \frac{dy}{dx} = e^{-x} + sin2x$.
11. Solve: (D^2-4D+3) y= sin3xcos2x.
12. Solve: $\frac{d^2y}{dx^2} + 2\frac{dy}{dx} + y = e^{2x} - cos2x$.
13. Solve: $\frac{d^2y}{dx^2} + -4y = cosh(2x-1) + 3^x$.
14. Solve: $(D^3-D)y=2x+1+4cosx+2e^x$.

15. Solve: $(D^4-1)y=e^x\cos x$.
16. Solve: $(D^2-4D+4)y = 8x^2e^{2x}\sin 2x$
17. Solve: $(D^2+a^2)y = \tan ax$.
18. Solve: $\frac{dx}{dt} + y = sint, \frac{dy}{dx} + x = cost;\ given\ that\ x = 2\ \&\ y = 0\ when\ t = 0.$
19. Solve: $(D-1)x+Dy = 2t+1$, ; $(2D+1)x+2Dy = t$
20. A body weighing 10 kg is hung from a spring. A pull of 20 kg. wt. will stretch the spring to 10 cm. The body is pulled down to 20 cm below the static equilibrium position and then released. Find the displacement of the body from its equilibrium position at time t sec., the maximum velocity and the period of oscillation.
21. A spring of negligible weight which stretches 1 inch under tension of 2 lb is fixed at one end and is attached to a weight of w lb at the other. It is found that resonance occurs when an axial periodic force 2 cos 2t lb acts on the weight. Show that when the free vibrations have died out, the forced vibrations are given by x = ct sin 2t, and find the values of w and c.
22. In an LCR circuit, the charge q on a plate of a condenser is given by $L\frac{d^2q}{dt^2} + R\frac{dq}{dt} + \frac{q}{C} = E\sin pt$. The circuit is tuned to resonance so that $p^2 = \frac{1}{LC}$. If initially the current i and the charge q be zero, show that, for small values of R/L, the current in the circuit at time t is given by (Et/2L) sin pt.
23. An uncharged condenser of capacity C is charged by applying an e.m.f. $\frac{Esint}{\sqrt{LC}}$ through leads of self inductance L and negligible resistance. Prove that at any time t, the charge on one of the plates is $\frac{EC}{2}\left\{sin\frac{t}{\sqrt{LC}} - \frac{t}{\sqrt{LC}}\cos\frac{t}{\sqrt{LC}}\right\}$

Module-5: Curve fitting, Correlation, and Regressions

1. Find the correlation coefficient and regration lines of y and x and x and y for the following data

x	1	2	3	4	5
y	2	5	3	8	7

2. Find the coefficient of correlation for the following data.

x	10	14	18	22	26	30
y	18	12	24	6	30	36

3. Compute the rank correlation coefficient for the following data

x	68	64	75	50	64	80	75	40	55	64
y	62	58	68	45	81	60	68	48	50	70

4. Ten students got the following % of marks in two subjects x and y. Compute their rank correlation coefficient.

Marks in x	78	36	98	25	75	82	90	62	65	39
Marks in y	84	51	91	60	68	62	86	58	53	47

5. Find the equation of the best fitting straight line for the data

x	0	1	2	3	4	5
y	9	8	24	28	26	20

6. A simply supported beam carries a concentrated load p at its midpoint corresponding to various Values of p the maximum deflection y is measured & is given below

p	100	120	140	160	180	200
y	0.45	0.55	0.60	0.70	0.80	0.85

Find the law of the form $y = a + bp$ & hence estimate y when p = 150.

7. Fit a second degree parabola of best fit $y = a+bx+cx^2$

x	1.0	1.5	2.0	2.5	3.0	3.5	4.0
y	1.1	1.3	1.6	2.0	2.7	3.4	4.1

8. Fit a second degree parabola $y = a+bx+cx^2$ in the least square sense for the following data

x	0	1	2	3	4
y	1	1.8	1.3	2.5	2.3

9. Fit a least square geometric curve $y = ax^b$ from the following data

x	1	2	3	4	5
y	0.5	2.0	4.5	8.0	12.5

10. The voltage v across a capacitor at time t sec is given by the following table

t	0	2	4	6	8
v	150	63	28	12	5.6

Use the method of least square of to fit a curve of the form $v= ae^{kt}$ to this data

16.0 University Result

Examination	FCD (S+, S, A)	FC (B)	SC (C, D, E)	% Passing

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Prepared by	Checked by		
Dr. S. L. Patil	Prof. S. A. Patil	HOD Electronics & Commn. Engg. Dept. HSIT HOD SOSHI	Principal

Subject Title	**Digital System Design Using Verilog**		
Subject Code	BEC302	**IA Marks (15) +Assignments (10) +lab continuous evaluation and Lab IA (15+10)**	50
Number of Lecture Hrs/Week /	03(L)	**Exam Marks**	50
Total Number of Lecture Hrs	40Theory + 8-10 Lab Slots	**Exam Hours**	03
CREDITS – 04			

FACULTY DETAILS:		
Name: Prof. S.R.Malluramath	**Designation:** Assistant Professor	**Experience:**10 years
No. of times course taught:01	**Specialization:** Industrial Electronics	

1.0 Prerequisite Subjects:

Sl. No	**Branch**	**Semester**	**Subject**
01	Students should have the knowledge of basic subjects	1 & 2	Basic Electronics

2.0 Course Objectives

This course will enable students to :

1. To impart the concepts of simplifying Boolean expression using K-map techniques and Quine-McCluskey minimization techniques.
2. To impart the concepts of designing and analyzing combinational logic circuits.
3. To impart design methods and analysis of sequential logic circuits.
4. To impart the concepts of verilog HDL data flow and behavioral models for the design of digital systems.

3.0 Course Outcomes

Having successfully completed this course, the student will be able to

	Course Outcome	**Cognitive Level**	**PO's**
CO1	Simplify Boolean functions using K-map & Quine-McCluskey minimization technique.	U	1,2,3,4,6,7,9,10,11,12
CO2	Analyze and design for combinational logic circuits.	U	1,2,3,4,5,6,7,9,
CO3	Analyze the concepts of Flip Flops (SR, D, T & JK) and design the synchronous sequential circuits using flip flops.	U	1,2,3,4,5,6,7,9, 10,11,12
CO4	Model Combinational circuits (adders, subtractors, multiplexers) and sequential circuits using Verilog descriptions.	U	1,2,3,4,5,6,7,9, 10,11,12
Total Hours of instruction		**40**	

4.0 Course Content

Theory		
Modules	**Teaching Hours**	**Bloom's Taxonomy (RBT) level**
Module 1		
Principles of combinational logic: Definition of combinational logic, canonical forms, generation of switching equations from truth tables, karnaugh maps up to 4 variables, Quine-McCluskey minimization technique, Quine-McCluskey donot care terms.	08	L1,L2,L3
Module -2		
Logic Design with MSI Components and Programmable Logic Devices: Binary adders and subtractors, comparators, Decoders, Encoders, Multiplexers, Programmable Logic Devices.	08	L1,L2,L3
Module-3		
Flip-Flops and its applications: The master-slave flip-flops(pulse triggered flip-flops): SR flip-flops, JK flip-flops, characteristics equations, registers, binary ripple counters, synchronous binary counters, counters based on shift registers, design of synchronous mod-n counter using clocked T, JK, D and SR flip-flops.	08	L1,L2,L3
Module-4		
Introduction to Verilog: Structure of verilog module, operators, data types, styles of description. **Verilog Data flow description:** Highlights of data flow description, structure of data flow description.	08	L1,L2,L3
Module-5		
Verilog Behavioral Description: Structure, variable assignment statement, sequential statements, loop statements, verilog behavioral description of multiplexers. **Verilog Structural Description:** Highlights of structural description, organization of structural description and structural description of ripple carry adder.	08	L1,L2,L3
Practical		
PART-A 1. To simplify the given boolean expressions and realize using verilog program. 2. To realize adder/subtractor (Full/Half) circuits using verilog data flow description. 3. To realize 4-bit ALU using verilog program. 4. To realize the following code converters using verilog behavioral description a) Gray to Binary & vice versa b) Binary to excess-3 & vice versa 5. To realize using verilog behavioral description: 8:1 mux, 8:3 encoder, Priority encoder. 6. To realize using verilog behavioral description: 1:8 mux, 3:8 decoder, 2-bit comparator. 7. To realize using verilog behavioral description: flip-flops: JK, SR, T and D. 8. To realize counters up/down (BCD and binary) using verilog behavioral description. **PART-B** 9. Verilog program to interface stepper motor to the FPGA/CPLD and rotate the motor in the specified direction (by N steps.) 10. Verilog programs to interface switches and LEDs to the FPGA /CPLD and demonstrate its working.	2 Hours per Batch	

5.0 Relevance to future subjects

Sl. No	Semester	Subject	Topics
01	VI	Mini Project	HDL
02	VIII	Project Work	Embedded system & HDL based projects

6.0 Relevance to Real World

SL.No	Real World Mapping
01	Analyze digital circuits in real time applications
02	Integrated Circuits (Chip)
03	Model creation for analysis

7.0 Gap Analysis and Mitigation

Sl. No	Delivery Type	Details
01	Tutorial	Topic: Solving different types of problems.

8.0 Books Used and Recommended to Students

Text Books
1. Digital Logic Applications and Design by John M. Yarbough, Thomson Learning, 2001. **2.** Digital Principles and Design by Donald D. Givone, McGraw Hill, 2002. **3.** HDL Programming VHDL and Verilog by Nazeih M. Botros, 2009 reprint, Dreamtech Press.
Reference Books
1. Fundamentals of logic design by Charles H Roth Jr., Cengage Learning. 2. Logic Design by Sudhakar Samuel, Pearson / Sanguine, 2007. **3.** Fundamentals of HDL by Cyril P. R. Pearson/Sanguine 2010.

9.0 Relevant Websites (Reputed Universities and Others) for Notes/Animation/Videos Recommended

Website and Internet Contents References
1) https://nptel.co.in
2) http://www.slideshare.net/farohalolya/HDL
3) https://www.youtube.com

10.0 Magazines/Journals Used and Recommended to Students

Sl.No	Magazines/Journals	Website
1	IEEE Explorer	http://ieeexplore.ieee.org/Xplore/home.jsp
2	International Journal of Science and Technology	http://www.sciencedirect.com/science/journal/00207683
3	PC World	http://www.pcworld.com/article/146957/components/article.html

11.0 Examination Note

Assessment Details both (CIE and SEE):

The weight age of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

CIE for the theory component of IPCC:

Two tests each of **15 marks (duration 01 hour)**

i) First test at the end of 5th week of the semester.
ii) Second test at the end of the 10th week of the semester.

Two assignments each of **10 marks**

i) First assignment at the end of 4th week of the semester.
ii) Second assignment at the end of 9th week of the semester.

Scaled down marks of two tests and two assignments added will be CIE marks for the theory component of IPCC for 30 marks.

CIE for the practical component of IPCC:

- 15 marks for the conduction of the experiment and preparation of laboratory record, and 10 marks for the test to be conducted after the completion of all the laboratory sessions.
- On completion of every experiment/program in the laboratory, the students shall be evaluated including viva-voce and marks shall be awarded on the same day.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to 15 marks.
- The laboratory test (duration 02/03 hours) after completion of all the experiments shall be conducted for 50 marks and scaled down to 10 marks.
- Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for 25 marks.
- The student has to secure 40% of 25 marks to qualify in the CIE of the practical component of the IPCC.

SEE for IPCC:

Theory SEE will be conducted by university as per the scheduled time table with common question papers for the course (duration 03 hours).

- The question paper will have ten questions. Each question is set for 20 marks.
- There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub questions), should have a mix of topics under that module.
- The students have to answer 5 full questions, selecting one full question from each module.

The theory portion of the IPCC shall be for both CIE & SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper shall include questions from the practical component.

- The minimum marks to be secured in CIE to appear for SEE shall be 10 (40% of maximum marks-25) in the theory component and 10 (40% of maximum marks -25) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included. The maximum of 04/05 subquestions are to be set from the practical component of IPCC, the total marks of all questions should not be more than 20 marks.

- SEE will be conducted for 100 marks and students shall secure 35% of the maximum marks to qualify in the SEE. Marks secured will be scaled down to 50.

- The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

12.0 Course Delivery Plan

Module No.	Lecture No.	Content of Lecture	Teaching Method	% Of Portion
1 Principles of Combinational Logic	1	Definition of combinational logic	Chalk and talk & YouTube Videos	20
	2	canonical forms	Chalk and talk	
	3	generation of switching equations from truth tables	Chalk and talk	
	4	karnaugh maps 2 variables	Chalk and talk	
	5	karnaugh maps 3 variables	Chalk and talk	
	6	karnaugh maps 4 variables	Chalk and talk	
	7	Quine-McCluskey 2,3 variables minimization technique	Chalk and talk	
	8	Quine-McCluskey 4 variables minimization technique & Quine-McCluskey donot care terms.	Chalk and talk	

2 Logic Design with MSI components and Programmable Logic Devices	9	Binary adders	Chalk and talk	20
	10	Binary Subtractors	Chalk and talk	
	11	Binary Comparators	Chalk and talk	
	12	Types of comparators	Chalk and talk	
	13	Decoders	Chalk and talk	
	14	Encoders	Chalk and talk	
	15	Multiplexers	Chalk and talk	
	16	Programmable Logic Devices	Chalk and talk & YouTube Videos	
3 Flip-Flops and Its Applications	17	The master-slave flip-flops(pulse triggered flip-flops)	Chalk and talk & YouTube Videos	20
	18	SR flip-flops	Chalk and talk	
	19	JK flip-flops, characteristics equations	Chalk and talk	
	20	registers, binary ripple counters,	Chalk and talk	
	21	synchronous binary counters,	Chalk and talk	
	22	counters based on shift registers,	Chalk and talk	
	23	Design of synchronous mod-n counter using clocked T, JK, D and SR flip-flops.	Chalk and talk	
	24	Design of synchronous mod-n counter using clocked D and SR flip-flops.	Chalk and talk	
4 Introduction to Verilog and Verilog Data Flow Description	25	Introduction to Verilog	Chalk and talk & YouTube Videos	20
	26	Structure of verilog module	Chalk and talk	
	27	operators	Chalk and talk	
	28	data types	Chalk and talk	
	29	styles of description	Chalk and talk	
	30	Verilog Data flow description	Chalk and talk	
	31	Highlights of data flow description,	Chalk and talk	
	32	structure of data flow description	Chalk and talk	
5 Verilog Behavioral Description and Verilog Structural Description	33	Verilog Behavioral Description	Chalk and talk & YouTube Videos	20
	34	Structure, variable assignment statement	Chalk and talk	
	35	sequential statements, loop statements	Chalk and talk	
	36	verilog behavioral description of multiplexers	Chalk and talk	
	37	Verilog Structural Description:	Chalk and talk	
	38	Highlights of structural description	Chalk and talk	
	39	organization of structural description	Chalk and talk	
	40	structural description of ripple carry adder	Chalk and talk	

13.0 Assignments, Pop Quiz, Mini Project, Seminars

Sl.No.	Title	Outcome expected	Allied study	Week No.	Individual / Group activity	Reference: book/website /Paper
1	Assignment 1: University Questions on canonical forms, K-map problems and QM method with & without do not care conditions problems.	Students study the Topics and will prepare for Final Exam.	Module-1 of the syllabus	3	Individual Activity	Text Book 1
2	Assignment 2: University Questions on arithmetic operators & programmable logic devices	Students study the Topics and will prepare for Final Exam.	Module-2 of the syllabus	6	Individual Activity.	Text Book 2
3	Assignment 3: University Questions on types of flip-flops, register & counters.	Students study the Topics and will prepare for Final Exam.	Module-3 of the syllabus	9	Individual Activity.	Text Book 2
4	Assignment 4: University Questions on operators, data types, data flow description, & its structure.	Students study the Topics and will prepare for Final Exam.	Module-4 of the syllabus	12	Individual Activity	Text Book 3
5	Assignment 5: University Questions on variable assignment & sequential statements, loop statements, organization & ripple carry adder of structural description	Students study the Topics and will prepare for Final Exam.	Module-5 of the syllabus	15	Individual Activity	Text Book 3

14.0 University Result

Examination	S+	S	A	B	C	D	E	F	% of passing
First Time Introduced	-	-	-	-	-	-	-	-	-

15.0 QUESTION BANK

Theory

Module – 1

1. Draw a model representing combinational circuits. Label the input & output variables. Write a general expressions showing the input & output relationship.
2. Describe what is mean by combinational logic in your own words.
3. How does a “truth table” express a combinational circuit?
4. Construct a truth table & write the Boolean output equations for the following verbal problem statements-

a. A single output variable, Z, is to be true when the input variables a and b true and when b is false but a and c are true.
b. An output is to be true (logical 1) when the value of the inputs exceeds 3. The weighting for each input variable is as follows: w=3 x = 3 y =2 z = -1

5. Convert the following equations into their requested canonical forms:
   a. (SOP) X = a'b + bc
   b. (POS) P = (w' + x) (y + z')
   c. (SOP) T = p(q' + s)
   d. (SOP) R = L + M'(N'M + M'L)
   e. (POS) U = r' + s(t + r) + s't

6. Simplify the following using Karnaugh maps:
   a. X = a'bc + ab'c' + abc
   b. Y= f(a, b, c) =Σ(1, 3, 5, 6, 7)
   c. T = w'xy + wz' + xyz'
   d. P = f(w, x, y, z) = Σ(0, 2, 8, 10)
7. Convert the given Boolean function f(x, y, z) = [x + xz (y + z)] into maxterm canonical formula and hence highlight the importance of canonical formula.
8. Distinguish the prime implicants and essential prime implicants. Determine the same of the function f(w, x, y, z) = Σ m(0, 1, 4, 5, 9, 11, 13, 15)
9. Design a combinational logic circuit, which converts BCD code into Excess – 3 code and draw the circuit diagram.
10. Simply the following noncanonical expressions using Karnaugh maps:
    a. T = a'b'c'de + a'bc'de + abcde + ab'c'de
    b. P = v'w' + v'wy' + vw'z
    c. G = y'z + w'xy' + w'xy + xy'z
11. Using Quine – Mcluskey method and prime implicant reduction table, obtain the minimal sum expression for the Boolean function f(w, x, y, z) = Σ m(1, 4, 6, 7, 8, 9, 10, 11, 15).
12. Obtain the minimal product of the following Boolean functions using QM technique: f(w, x, y, z) = Σ m(1, 5, 7, 10, 11) + dc(2, 3, 6, 13)

Module -2

1. Shortly explain the decoder.
2. Design 4:16 decoder using two 3:8 decoder.
3. Design 5:32 decoder using one 2:4 & four 3:8 decoder IC's.
4. Explain realization of multiple output function using Binary decoder.
5. Implement following function using 3:8 decoder – f1(A,B,C) = m(1,4,5,7) and f2(A,B,C) = M(2,3,6,7).
6. Design combinational circuit of BCD to 7 segment display using decoder.
7. Write short note on – encoder.
8. Design keypad interface to digital system using 10 lines to BCD encoder.
9. Design octal to binary encoder.
10. Briefly explain priority encoder.

11. Design 32:5 priority encoder using four 74LS148 & gates.
12. Implement full adder & full substractor using decoder & write its truth table.
13. Write short note on – multiplexer and de-multiplexer.
14. Design 32:1 MUX using two 74LS150 ICs.
15. Design 32:1 MUX using four 8:1 MUX & 2:4 decoder.
16. Implement following functions using 4:1, 8:1 & 16:1 MUX - f1(A,B,C,D) = Σ m(0,1,2,4,6,9,12,14) and f2(A,B,C,D) =Σ m(0,1,3,4,8,9,15).
17. Implement following expression – F(A, B, C, D) = ABD + ACD + BCD + ACD using 8:1 MUX.
18. Construct 8:1 MUX using 2:1 MUX.
19. Implement full adder & full substractor using DeMUX.
20. Explain the concept of carry look ahead adder. Design 4-bit carry look ahead circuit.
21. Design 2-bit comparator.
22. Explain full adder & full substractor circuit.
23. Explain the programmable logic devices

Module -3

1. Explain the difference between combinational & sequential circuits.
2. Explain the difference between synchronous & asynchronous sequential circuits.
3. Explain the operation of SR Flip Flop.
4. Explain the working of switch Debouncer using SR latch.
5. Explain SR latch using NOR gate & Gated SR latch using NOR & NAND gate.
6. Explain Characteristics of SR Latch & its state Transition Diagram.
7. Explain the race around condition in detail. How it is eliminated?
8. Draw the master slave SR flip – flop. Explain flip-flop action during control signal & also give the truth table.
9. Draw & explain master slave JK flip-flop.
10. Explain JK , T & D-flip-flop.
11. Draw & explain edge triggered flip-flop.
12. Convert SR flip flop to JK flip flop.
13. Explain Left shift serial in serial out register with D flip flop.
14. Explain serial in parallel out shift register.
15. Explain parallel in serial out shift register.
16. Explain Ring counter & Johnson Counter.
17. Explain binary ripple counters.
18. Explain synchronous binary counter.

Module – 4

1. Explain the introduction to verilog.
2. Explain the types of data.
3. Explain the styles of description.
4. Explain the data flow description.
5. Explain the structure of the verilog module.
6. Explain the verilog operators.

7. Explain the data flow description.

Module – 5

1. Explain the verilog behavioral description of multiplexer.
2. Explain the verilog structural description of 4 bit ripple carry adder.
3. Explain the structure of verilog behavioral description.
4. Explain variable assignment statement.
5. Explain sequential statements.
6. Explain the loop statements.
7. Explain the verilog structural description.
8. Explain the organization of structural description.

Subject Title	**Digital System Design Using Verilog Lab**		
Subject Code	BEC302	**Laboratory work (25)**	25
Number of Lecture Hrs/Week /	2(P)	**Exam Marks**	50
Total Number of Lecture Hrs	10 Lab Slots	**Test Hours**	02
CREDITS – 04			

FACULTY DETAILS:		
Name: Prof. K.S. Patil	**Designation:** Assistant Professor	**Experience:**30 years
No. of times course taught: 01	**Specialization:** VLSI & Embedded Systems	

1.0 Prerequisite Subjects:

Sl. No	Branch	Semester	Subject
01	Students should have the knowledge of basic subjects	1 & 2	Basic Electronics

2.0 Course Objectives

This course will enable students to:

- Familiarize with the CAD tool to write HDL programs.
- Understand simulation and synthesis of digital design.
- Program FPGAs/CPLDs to synthesise the digital designs.
- Interface hardware to programmable ICs through I/O ports.
- Choose either Verilog or VHDL for a given Abstraction level.

3.0 Course Outcomes

Having successfully completed this course, the student will be able to

	Course Outcome	Cognitive Level	PO's
CO1	Write the Verilog/VHDL programs to simulate Combinational circuits in Dataflow, Behavioral and Gate level Abstractions.	U	1,2,3,4,6,7,9, 10,11,12
CO2	Describe sequential circuits like flip flops and counters in Behavioral description and obtain simulation waveforms.	U	1,2,3,4,5,6,7, 9,10,11,12
CO3	Synthesize Combinational and Sequential circuits on programmable ICs and test the hardware.	U	1,2,3,4,5,6,7, 9,10,11,12
CO4	Interface the hardware to the programmable chips and obtain the required output.	U	1,2,3,4,5,6,7, 9,10,11,12
CO5	Write the Verilog/VHDL programs to simulate Combinational circuits in Dataflow, Behavioral and Gate level Abstractions.	U	1,2,3,4,5,6,7, 9,10,11,12

Total Hours of instruction	24

4.0 Course Content

Practical		
Experiments	**Teaching Hours**	**Bloom's Taxonomy (RBT) level**
PART-A 11. To simplify the given boolean expressions and realize using verilog program.	02	L3
12. To realize adder/subtractor (Full/Half) circuits using verilog data flow description.	02	L3
13. To realize 4-bit ALU using verilog program.	02	L3
14. To realize the following code converters using verilog behavioral description b) Gray to Binary & vice versa b) Binary to excess-3 & vice versa	02	L3
15. To realize using verilog behavioral description: 8:1 mux, 8:3 encoder, Priority encoder.	02	L3
16. To realize using verilog behavioral description: 1:8 mux, 3:8 decoder, 2-bit comparator.	02	L3
17. To realize using verilog behavioral description: flip-flops: JK, SR, T and D.	02	L3
18. To realize counters up/down (BCD and binary) using verilog behavioral description.	02	L3
PART-B	02	L3
19. Verilog program to interface stepper motor to the FPGA/CPLD and rotate the motor in the specified direction (by N steps.)	02	L3
20. Verilog programs to interface switches and LEDs to the FPGA /CPLD and demonstrate its working.	02	L3

5.0 Relevance to future subjects

Sl. No	Semester	Subject	Topics
01	VI	Mini Project	HDL
02	VIII	Project Work	Embedded system.

6.0 Relevance to Real World

SL.No	Real World Mapping
01	Analyze digital circuits in real time applications

7.0 Gap Analysis and Mitigation

Sl. No	Delivery Type	Details
01	Tutorial	Topic: Solving different types of programs

8.0 Books Used and Recommended to Students

4. Lab Manual

9.0 Relevant Websites (Reputed Universities and Others) for Notes/Animation/Videos Recommended

Website and Internet Contents References
4) https://nptel.co.in

10.0 Magazines/Journals Used and Recommended to Students

Sl.No	Magazines/Journals	website
1	IEEE Explorer	http://ieee.com
2	International Journal of Science and Technology	http://www.sciencedirect.com/science/journal/00207683
3	Journal of Communication Engineering	http://ieee.com

11.0 Examination Note

CIE for the practical component of IPCC:

- 15 marks for the conduction of the experiment and preparation of laboratory record, and 10 marks for the test to be conducted after the completion of all the laboratory sessions..
- On completion of every experiment/program in the laboratory, the students shall be evaluated including viva-voce and marks shall be awarded on the same day
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to 15 marks.
- The laboratory test (duration 02/03 hours) after completion of all the experiments shall be conducted for 50 marks and scaled down to 10 marks.
- Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for 25 marks.
- The student has to secure 40% of 25 marks to qualify in the CIE of the practical component of the IPCC.

12.0 Course Delivery Plan

Experiments	% of portion
PART-A	
1. To simplify the given Boolean expressions and realize using verilog program.	10
2. To realize adder/sub tractor (Full/Half) circuits using verilog data flow description.	20
3. To realize 4-bit ALU using verilog program.	30
4. To realize the following code converters using verilog behavioral description c) Gray to Binary & vice versa b) Binary to excess-3 & vice versa	40
5. To realize using verilog behavioral description: 8:1 mux, 8:3 encoder, Priority encoder.	50
6. To realize using verilog behavioral description: 1:8 mux, 3:8 decoder, 2-bit comparator.	60
7. To realize using verilog behavioral description: flip-flops:a) JK, b)SR, c)T and d) D.	70
8. To realize counters up/down (BCD and binary) using verilog behavioral description.	80
PART-B	
9. Verilog program to interface stepper motor to the FPGA/CPLD and rotate the motor in the specified direction (by N steps.)	90

10. Verilog programs to interface switches and LEDs to the FPGA /CPLD and demonstrate its working.	100

13.0 University Result

Examination	S+	S	A	B	C	D	E	F	% of passing
First Time Introduced	-	-	-	-	-	-	-	-	-

14.0 VIVA BANK

1. HDL stands for_____.
2. VHDL stands for_____.
3. Explain the structure of Verilog module.
4. Explain Verilog Ports.
5. List the logical operators. Explain any one with example.
6. List the Relational operators. Explain any one with example.
7. List the Arithmetic operators. Explain any one with example.
8. Explain Shift and Rotate operators.
9. What is Data type?
10. Explain the Verilog Data types.
11. Compare VHDL and Verilog.
12. If A and B are two unsigned variables, with A=1100 and B=1001, find the value of

The following expressions:

a. (A AND B) b. (A ^ B) c. (A & B) d. (A NOR B) e. (A && B) f. !(B) g. ~|(A) h. A >>1 i. B ror 2

13. What do you mean concurrent statements?
14. Draw the simulation wave form for 2x1 MUX.
15. What is logic synthesis?
16. Explain Signal declaration and assignment statements.
17. What is sensitivity list?
18. Explain the structure of PROCEDURE in Verilog.
19. Explain the structure of TASKS in Verilog.
20. Explain the structure of FUNCTIONS in Verilog.
21. Which IDE is used for Verilog code development?
22. How many windows get open when you open the Xilinx Project Navigator?
23. FPGA stands for_____.
24. JTAG stands for_____.
25. Which simulator is used in Lab.

Prepared by	Checked by		
Prof. K.S.Patil	Prof.D.B.Madihalli	HOD Electronics & Comm. Engg. Dept. HSIT NIDASOSHI	Principal

Subject Title	**Electronic Principles and Circuits**		
Subject Code	**BEC303**	**IA Marks 15 +Assignments GD/Quiz/Seminar10 + Lab 15 +10**	50(100)
Number of Lecture Hrs/Week /	03	**Exam Marks (appearing for)**	50 (100)
Total Number of Lecture Hrs	40	**Exam Hours**	03
CREDITS – 03			

FACULTY DETAILS:		
Name: Prof. D M Kumbhar	**Designation:** Assistant Professor	**Experience :Teach- 16** years (07years)
No. of times course taught: 01	**Specialization:**Digital Electronics	

1.0 Prerequisite Subjects:

Sl. No	Branch	Semester	Subject
01	Students should have the knowledge of basic subjects	I, II & III	Basic electronics

2.0 Course Objectives

This course will enable students to

- Design and analyze the BJT circuits as an amplifier and voltage regulation.
- Design of MOSFET Amplifiers and analyze the basic amplifier configurations using small signal equivalent circuit models
- Design of operational amplifiers circuits as Comparators, DAC and filters.
- Understand the concept of positive and negative feedback.
- Analyze Power amplifier circuits in different modes of operation.
- Construct Feedback and Oscillator circuits using FET.
- Understand the thyristor operation and the different types of thyristors.

3.0 Course Outcome

Having successfully completed this course, the student will be able to

	Course Outcome	**Cognitive Level**	**PO's**
203.1	Understand the characteristics of BJTs and FETs for switching and amplifier circuits.	U	1,2,3,4,5,6,7,8,9, 10,11,12
203.2	Design and analyze amplifiers and oscillators with different circuit configurations and biasing conditions.	U	1,2,3,4,5,6,7,8,9, 10,11,12
203.3	Understand the feedback topologies and approximations in the design of amplifiers and oscillators.	U	1,2,3,4,5,6,7,8,9, 10,11,12
203.4	Design of circuits using linear ICs for wide range applications such as ADC, DAC, filters and timers.	U	1,2,3,4,5,6,7,8,9, 10,11,12
203.5	Understand the power electronic device components and its functions for basic power electronic circuits.	U	1,2,3,4,5,6,7,8,9, 10,11,12
Total Hours of instruction		**40**	

4.0 Course Content

Modules	Teaching Hours	Bloom's Taxonomy (RBT) level
Module 1		
Transistor Biasing: Voltage Divider Bias, VDB Analysis, VDB Load line and Q point; Two supply Emitter Bias, Other types of Bias. **BJT AC models**: Base Biased Amplifier, Emitter Biased Amplifier, Small Signal Operation, AC Beta, AC Resistance of the emitter diode, Two transistor models, Analyzing an amplifier, H parameters, Relations between R and H parameters. **Voltage Amplifiers**: Voltage gain, Loading effect of Input Impedance. **CC Amplifiers:** CC Amplifier, Output Impedance.	**08**	**L1, L2,L3**
Module -2		
MOSFET Biasing in MOS amplifier circuits: Fixing VGS, Fixing VG, Drain to Gate feedback resistor. Small signal operation and modelling: The DC bias point, signal current in drain, voltage gain, and small signal equivalent circuit models, transconductance, The T equivalent circuit model. MOSFET Amplifier configuration: Basic configurations, characterizing amplifiers, CS amplifier with and without source resistance, The Common Gate Amplifier, Source follower.	**08**	**L1, L2,L3**
Module-3		
Linear Opamp Circuits: Summing Amplifier and D/A Converter, Nonlinear Op-amp Circuits: Comparator with zero reference, Comparator with non-zero references. Comparator with Hysteresis. **Oscillator:** Theory of Sinusoidal Oscillation, The Wein-Bridge Oscillator, RC Phase Shift Oscillator, The Colpitts Oscillator, Hartley Oscillator, Crystal Oscillator. **The 555 timer**: Monostable Operation, Astable Operation.	**08**	**L1, L2,L3**
Module-4		
Negative Feedback: Four Types of Negative Feedback, VCVS Voltage gain, Other VCVS Equations, ICVS Amplifier, VCIS Amplifier, ICIS Amplifier (No Mathematical Derivation). **Active Filters:** Ideal Responses, First Order Stages, VCVS Unity Gain Second Order Low pass Filters, VCVS Equal Component Low Pass Filters, VCVS High Pass Filters, MFB Bandpass Filters, Bandstop Filters.	**08**	**L1, L2,L3**
Module-5		
Power Amplifiers: Amplifier terms, Two load lines, Class A Operation, Class B operation, Class B push pull emitter follower, Class C Operation. **Thyristors:** The four layer Diode, SCR, SCR Phase control, Bidirectional Thyristors, IGBTs, and Other Thyristors.	**08**	**L1, L2, L3**

5.0 Relevance to future subjects

Sl. No	Semester	Subject	Topics
01	VIII	Project work	Digital transmission of voice, video and data.
02	IV	Communication	AM. FM. PM, Noise Analysis

6.0 Relevance to Real World

SL.No	Real World Mapping
01	Design of electronic circuits for different applications.
02	Hobby/Mini projects
03	Home appliances/ controlling of equipments.

7.0 Gap Analysis and Mitigation

Sl. No	Delivery Type	Details
01	Tutorial	Topic: Simulation software like Simulink, PSpice and Proteus.
02	NPTEL	Basics, Assembly &Application

8.0 Books Used and Recommended to Students

Text Books
1. Albert Malvino, David J Bates, Electronic Principles, 7th Edition, Mc Graw Hill Education, 2017, ISBN:978-0-07-063424-4. 2. Microelectronic Circuits, Theory and Applications, Adel S Sedra, Kenneth C Smith, 6thEdition, Oxford, 2015.ISBN:978-0-19-808913-1
Reference Books
1. Integrated Electronics: Analog and Digital Circuits and Systems, Jacob Millman, Christos C. Halkias, McGraw-Hill, 2015. 2. Electronic Devices and Circuit, Boylestad & Nashelsky, Eleventh Edition, Pearson, January 2015.

9.0 Relevant Websites (Reputed Universities and Others) for Notes/Animation/Videos Recommended

Website and Internet Contents References
5) https://nptel.co.in 6) http://m.noteboy.in/vtuflies/machine%20drawing.pdf

10.0 Magazines/Journals Used and Recommended to Students

Sl.No	Magazines/Journals	website
1	IEEE Xplorer	http://ieee.com
2	International Journal of Science and Technology	http://www.sciencedirect.com/science/journal/00207683
3	Journal of Communication Engineering	http://ieee.com

11.0 Examination Note

Assessment Details (both CIE and SEE)

The weight age of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

The IPCC means the practical portion integrated with the theory of the course. CIE marks for the theory component are **25 marks** and that for the practical component is **25 marks**.

CIE for the theory component of the IPCC

- 25 marks for the theory component are split into **15 marks** for two Internal Assessment Tests (Two Tests, each of 15 Marks with 01-hour duration, are to be conducted) and **10 marks** for other assessment methods mentioned in 22OB4.2. The first test at the end of 40-50% coverage of the syllabus and the second test after covering 85-90% of the syllabus.

- Scaled-down marks of the sum of two tests and other assessment methods will be CIE marks for the theory component of IPCC (that is for **25 marks)**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the theory component of IPCC.

CIE for the practical component of the IPCC

- **15 marks** for the conduction of the experiment and preparation of laboratory record, and **10 marks** for the test to be conducted after the completion of all the laboratory sessions.
- On completion of every experiment/program in the laboratory, the students shall be evaluated including vivavoce and marks shall be awarded on the same day.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to **15 marks**.
- The laboratory test **(duration 02/03 hours)** after completion of all the experiments shall be conducted for 50 marks and scaled down to **10 marks.**
- Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **25 marks**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the practical component of the IPCC.

SEE for IPCC

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**)

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored by the student shall be proportionally scaled down to 50 Marks

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper may include questions from the practical component.

- The minimum marks to be secured in CIE to appear for SEE shall be 10 (40% of maximum marks-25) in the theory component and 10 (40% of maximum marks -25) in the practical component. The laboratory
- component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included**.** The maximum of 04/05 sub-questions are to be set from the practical
- component of IPCC, the total marks of all questions should not be more than 20 marks.
- SEE will be conducted for 100 marks and students shall secure 35% of the maximum marks to qualify for the SEE. Marks secured will be scaled down to 50.
- The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

12.0 Course Delivery Plan

Module No.	Lecture No.	Content of Lecture	Teaching Method	% Of Portion
1	1	Voltage Divider Bias, VDB Analysis, VDB Load line and Q point	Chalk and talk, PPT	20
	2	Two supply Emitter Bias, Other types of Bias.	Chalk and talk, PPT	
	3	Base Biased Amplifier, Emitter Biased Amplifier	Chalk and talk, PPT	
	4	Small Signal Operation, AC Beta,	Chalk and talk, PPT	
	5	AC Resistance of the emitter diode	Chalk and talk, PPT	
	6	Two transistor models, Analyzing an amplifier, H parameters, Relations between R and H parameters.	Chalk and talk, PPT	
	7	Voltage gain, Loading effect of Input Impedance	Chalk and talk, PPT	
	8	CC Amplifier, Output Impedance.	Chalk and talk, PPT	
2	9	Biasing in MOS amplifier circuits: Fixing VGS, Fixing VG	Chalk and talk, PPT	20
	10	Drain to Gate feedback resistor.	Chalk and talk, PPT	
	11	Small signal operation and modeling: The DC bias point, signal current in drain, voltage gain	Chalk and talk, PPT	
	12	Small signal equivalent circuit models	Chalk and talk, PPT	
	13	Transconductance, The T equivalent circuit model.	Chalk and talk, PPT	
	14	MOSFET Amplifier configuration: Basic configurations, characterizing amplifiers	Chalk and talk, PPT	
	15	CS amplifier with and without source resistance,	Chalk and talk, PPT	
	16	The Common Gate Amplifier, Source follower.	Chalk and talk, PPT	
3	17	**Linear Op-amp Circuits:** Summing Amplifier	Chalk and talk, PPT	20
	18	D/A Converter	Chalk and talk, PPT	
	19	Nonlinear Op-amp Circuits: Comparator with zero reference	Chalk and talk, PPT	
	20	Comparator with non-zero references	Chalk and talk, PPT	
	21	Comparator with Hysteresis	Chalk and talk, PPT	
	22	**Oscillator:** Theory of Sinusoidal Oscillation, The Wein-Bridge Oscillator, RC Phase Shift Oscillator	Chalk and talk, PPT	
	23	The Colpitts Oscillator, Hartley Oscillator, Crystal Oscillator.	Chalk and talk, PPT	
	24	**The 555 timer**: Mono stable Operation, Astable Operation.	Chalk and talk, PPT	
4	25	**Negative Feedback:** Four Types of Negative Feedback	Chalk and talk, PPT	20
	26	VCVS Voltage gain, Other VCVS Equations	Chalk and talk, PPT	
	27	ICVS Amplifier, VCIS Amplifier, ICIS Amplifier	Chalk and talk, PPT	
	28	**Active Filters:** Ideal Responses, First Order Stages	Chalk and talk, PPT	
	29	VCVS Unity Gain Second Order Low pass Filters	Chalk and talk, PPT	
	30	VCVS Equal Component Low Pass Filters	Chalk and talk, PPT	
	31	VCVS High Pass Filters	Chalk and talk, PPT	
	32	MFB Bandpass Filters, Bandstop Filters	Chalk and talk, PPT	
5	33	**Power Amplifiers:** Amplifier terms, Two load lines	Chalk and talk, PPT	20
	34	Class A Operation	Chalk and talk, PPT	
	35	Class B operation	Chalk and talk, PPT	
	36	Class B push pull emitter follower	Chalk and talk, PPT	
	37	Class C Operation	Chalk and talk, PPT	
	38	**Thyristors:** The four layer Diode, SCR	Chalk and talk, PPT	
	39	SCR Phase control, Bidirectional Thyristors	Chalk and talk, PPT	
	40	IGBTs, Other Thyristors	Chalk and talk, PPT	

13.0 Assignments, Pop Quiz, Mini Project, Seminars

Sl.No.	Title	Outcome expected	Allied study	Week No.	Individual / Group activity	Reference: book/website /Paper
1	Assignment 1: University Questions on random process and Amplitude modulation	Students study the Topics and will prepare for Final Exam.	Module-1, 2 & 3 of the syllabus	7	Individual Activity	Book 1, 2 of the reference list. Website of the Reference list
2	Assignment 2: University Questions on module Angle Modulation and Noise in communication system	Students study the Topics and will prepare for Final Exam.	Module-4 & 5 of the syllabus	14	Individual Activity.	Book 1, 2 of the reference list. Website of the Reference list

14.0 University Result

NEW SCHME

Prepared by	Checked by		
Prof. D. M. Kumbhar	Prof. P. V. Patil	HOD Electronics & Commn. Engg. Dept HSIT NIDASOSHI	Principal

Subject Title	**Electronic Principle Circuits Lab**		
Subject Code	**BECL305**	**CIE Marks**	50
Number of Lecture Hrs/Week /	02 Hours Laboratory	**SEE Marks**	50
RBT Level	L1, L2, L3	**Exam Hours**	03
CREDITS – 01			

FACULTY DETAILS:		
Name: Prof. K.S.Patil	**Designation:** Assistant Professor	**Experience :Teach- 30** years
No. of times course taught: 00	**Specialization:** VLSI& Embedded Systems	

1.0 Prerequisite Subjects:

Sl. No	Branch	Semester	Subject
01	ECE	I & II	Analog Electronics Circuits
02	ECE	I & II	Op-Amp

Sl. No	Branch	Semester	Subject
01	Students should have the knowledge of basic subjects	I & II	Basic electrical & electronics subjects

2.0 Course Objectives

This laboratory course enables students to

- Understand the electronic circuit schematic and its working
- Realize circuits of Bridge Rectifier, clippers& Clampers, JFET Characteristics & Amplifier
- Realize the op-amp circuits for precision rectifiers.
- Study the Full Wave Controlled Rectifier using RC triggering circuit.
- Design and test RC phase shift oscillator
- .

3.0 Course Outcomes

Having successfully completed this course, the student will be able to

	Course Outcome	Cognitive	PO's
CO1	Understand the characteristics of BJTs& FETs for switching &amplifier circuits	U	1,2,3,4,5,6,7,8,9, 10,11,12
CO2	Design and analyze amplifiers and oscillator with different configurations & biasing conditions.	U	1,2,3,4,5,6,7,8,9, 10,11,12
CO3	Understand the feedback topologies & approximations in design of amplifiers and oscillators	U	1,2,3,4,5,6,7,8,9, 10,11,12
CO4	Design of circuits using liner ICs in ADC ,DAC ,filters & timers	U	1,2,3,4,5,6,7,8,9, 10,11,12
CO5	Understanding the power electronic device in power electronic circuits	U	1,2,3,4,5,6,7,8,9,
Total Hours of instruction		**40**	

4.0 Course Content

Laboratory Experiments:

1	Design and Test (i) Bridge Rectifier with Capacitor Input Filter (ii)Zener voltage regulator
2	Design and Test Biased Clippers – a)Positive, b) Negative , c)Positive-Negative Positive and Negative Clampers with and without Reference
3	Plot the transfer and drain characteristics of a JFET and calculate its drain resistance, mutual conductance and amplification factor
4	Plot the transfer and drain characteristics of n-channel MOSFET and calculate its parameters, namely; drain resistance, mutual conductance and amplification factor
5	Design and test (i) Emitter Follower , (ii)Darlington Connection
6	Design and plot the frequency response of Common Source JFET/MOSFET amplifier
7	Test the Op amp Comparator with zero and non zero reference and obtain the Hysteresis curve
8	Design and test Full wave Controlled rectifier using RC triggering circuit
9	Design and test Precision Half wave and full wave rectifiers using Op-amp
10	Design and test RC phase shift oscillator

5.0 Relevance to future subjects

Sl. No	Semester	Subject	Topics
01	VII/VIII	Project work	Analog & Digital Circuits based concept

6.0 relevance to real world

SL No	Real World Mapping
01	Design analog circuits using diodes for different applications
02	Design circuits using SCR for different applications
02	Hobby/Mini projects
03	Home appliances/controlling of equipments.

7.0 Gap Analysis and Mitigation

Sl. No	Delivery Type	Details
01	Tutorial	Topic: Simulation software like Simulink, PSpice and Proteus.
02	NPTEL	Assembly Application

8.0 Books Used and Recommended to Students

Text Books

1. Fundamentals of Electronic Devices and Circuits Lab Manual, David A Bell, 5th Edition, 2009, Oxford University Press.
2. Fundamentals of Logic Design, Charles H RothJr., Larry L Kinney, Cengage Learning, 7th Edition.

9.0 Relevant Websites (Reputed Universities and Others) for Notes/Animation/Videos Recommended

Website and Internet Contents References
7) https://nptel.co.in 8) http://m.noteboy.in/vtuflies/machine%20drawing.pdf 9) Web links and Video Lectures (e-Resources): 1. Integrated Electronics: Analog and Digital Circuits and Systems, Jacob Millman, Christos C. Halkias, McGraw-Hill, 2015. 2. Electronic Devices and Circuit, Boylestad & Nashelsky, Eleventh Edition, Pearson, January 2015.

10.0 Magazines/Journals Used and Recommended to Students

Sl.No	Magazines/Journals	website
1	IEEE Xplorer	http://ieee.com
2	International Journal of Science and Technology	http://www.sciencedirect.com/science/journal/00207683
3	Journal of Communication Engineering	http://ieee.com

11.0 Examination Note

Assessment Details (both CIE and SEE)

The weight age of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

CIE for the practical component of the IPCC

- 15 marks for the conduction of the experiment and preparation of laboratory record, and 10 marks for the test to be conducted after the completion of all the laboratory sessions
- On completion of every experiment/program in the laboratory, the students shall be evaluated including viva voce and marks shall be awarded on the same day.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write ups are added and scaled down to 15 marks.
- The laboratory test (duration 02/03 hours) after completion of all the experiments shall be conducted for 50 marks and scaled down to 10 marks.
- Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for 25 marks
- The student has to secure 40% of 25 marks to qualify in the CIE of the practical component of the IPCC

12.0 Course Delivery Plan

Experiment	Lecture No.	Content	% of Portion
1	1	Design and Test (i) Bridge Rectifier with Capacitor Input Filter (ii)Zener voltage regulator	10
2	2	Design and Test Biased Clippers – a)Positive, b) Negative , c)Positive-Negative Positive and Negative Clampers with and without Reference	20
3	3	Plot the transfer and drain characteristics of a JFET and calculate its drain resistance, mutual conductance and amplification factor	30
4	4	Plot the transfer and drain characteristics of n-channel MOSFET and calculate its parameters, namely; drain resistance, mutual conductance and amplification factor.	40
5	5	Design and test (i) Emitter Follower , (ii)Darlington Connection	50
6	6	Design and plot the frequency response of Common SourceJFET/MOSFET amplifier	60
7	7	Test the Op amp Comparator with zero and non zero reference and obtain the Hysteresis curve	70
8	8	Design and test Full wave Controlled rectifier using RC triggering circuit	80
9	9	Design and test Precision Half wave and full wave rectifiers using Op-amp	90
10	10	Design and test RC phase shift oscillator	100

13.0 VIVA BANK

1. **What is meant by rectifier?**
2. **Define peak inverse voltage (PIV) of a diode. What is the difference between PIV of a center tapped FWR and bridge rectifier?**
3. **What is ripple factor for full-wave rectifier?**
4. **What is efficiency for full-wave rectifier?**
5. Explain what is a ***zener diode***?
6. Explain what is zener voltage?
7. Explain what is meant by the temperature coefficient?
8. List the applications of the ***Zener diode***.
9. Define clipper
10. List different types of clippers
11. Define clamper
12. List different types of clampers
13. Define positive clamper
14. Define negative clamper
15. **What is the major difference between a bipolar and a unipolar device**
16. **Why is terminology "field effect" appropriate for this terminal device ?**
17. **How is drain current controlled in a JFET?**
18. **What is meant by drain characteristic of FETs?**
19. **What is dynamic resistance of a JFET?**

20. State the full form of MOSET
21. How many terminals of MOSFET(4)
22. Is MOSFET voltage controlled or current controlled device?
23. What are modes of operation of MOSFET
24. What type of amplifier is an emitter follower amplifier? ...
25. How is the current gain of an emitter follower amplifier?
26. What is a Darlington pair mainly used for?
27. What is use of comparator
28. Why SCR is used in rectifiers
29. Another name for SCR
30. What is precision rectifier
31. **What is the frequency of RC phase shift oscillator?**
32. **What is a phase shift oscillator?**
33. **Why RC oscillators cannot generate high frequency oscillations?**
34. **What are the applications of RC phase shift oscillators?**
35. How many RC sections are considered
36. What is the frequency of oscillation
37. Sate SCR operation
38. What are the requirements for producing sustained oscillations in feedback circuits? For sustained oscillations,
39. What are the different oscillators?
40. List the classification of oscillators?

13.0 University Result

Examination	Total Students	S+	S	A	B	C	D	E	F	% Passing
← New Scheme →										

Prepared by	Checked by		
Prof. K.S.Patil	Prof.S.S.Malaj	HOD Electronics & Commn. Engg. Dept. HSIT NIDASOSHI	Principal

Subject Title	**Network Analysis**		
Subject Code	BEC304	**CIE Marks**	50
Number of Lecture Hrs / Week	3:0:0	**Semester End Exam Marks**	50
Total Number of Lecture Hrs	40	**Exam Hours**	03

FACULTY DETAILS:		
Name: Prof. P.V.Patil	**Designation:** Asst Professor	**Experience:** 11yrs 05 Months.
No. of times course taught: 08	**Specialization:** VLSI Design & Embedded Systems.	

1.0 Prerequisite Subjects:

Sl. No	Branch	Semester	Subject
01	ECE	I	Engineering Mathematics I
02	ECE	II	Engineering Mathematics II
03	EEE	I/II	Basic Electrical

2.0 Course Objectives

This course will enable students to:

- Describe basic network concepts emphasizing source transformation, source shifting, mesh and nodal techniques to solve for resistance/impedance, voltage, current and power.
- Explain network Thevenin‘s, Millman‘s, Superposition, Maximum Power transfer and Norton‘s Theorems and apply them in solving the problems related to Electrical Circuits.
- Explain the behavior of networks subjected to transient conditions.
- Use applications of Laplace transforms to network problems.
- Study two port network parameters like Z, Y, T and h and their inter-relationships and applications.
- Study of RLC Series and parallel tuned circuit.

3.0 Course Outcomes

Having successfully completed this course, the student will be able to draw and analyze.

	Course Outcome	RBT Leve	POs
C202.1	Determine currents and voltages using source transformation/source shifting/mesh/nodal analysis and reduce given network using star delta	L1 , L2, L3,	PO1, PO2, PO3, PO4, PO12
C202.2	Solve network problems by applying superposition/Reciprocity/Thevenin’s Norton’s/Maximum power transfer/Milliman’s network theorems and electrical laws to reduce circuit complexities and to arrive at feasible solutions.	L1 , L2, L3, L4	PO1, PO2, PO3, PO4, PO12
C202.3	Calculate current and voltage for the given circuit under transient conditions.	L1 , L2, L3,	PO1, PO2, PO3, PO4, PO12

C202.4	Apply Laplace transform to solve the given network.	L1 , L2, L3,	PO1, PO2, PO3, PO4, PO12
C202.5	Evaluate for RLC elements/frequency response related parameters like resonant frequency, quality factor ,half power frequencies, voltage across inductor and capacitor, current through RLC elements in resonant circuits.	L1 , L2, L3, L4	PO1, PO2, PO3, PO4, PO12

4.0 Course Content

Course Content:

Module	Teaching Hours	Bloom's Taxonomy (RBT) level
Module 1: Basic Concepts: Practical sources, Source transformations, Network reduction using Star – Delta transformation, Loop and node analysis with linearly dependent and independent sources for DC and AC networks.	**10 Hours**	**L1 , L2, L3, L4**
Module 2: Network Theorems: Superposition, Millman's theorems, Thevinin's and Norton's theorems, Maximum Power transfer theorem.	**10 Hours**	**L1 ,L2,L3 ,L4**
Module 3: Transient behavior and initial conditions: Behavior of circuit elements under switching condition and their Representation, evaluation of initial and final conditions in RL, RC and RLC circuits for AC and DC excitations.	**10 Hours**	**L1 ,L2,L3**
Module 4: Laplace Transformation & Applications: Solution of networks, step, ramp and impulse responses, waveform Synthesis.	**10 Hours**	**L1 ,L2,L3 ,L4**
Module 5: **Two port network parameters:** Definition of Z, Y, h and Transmission parameters, modeling with these parameters, relationship between parameters sets. **Resonance: Series Resonance:** Variation of Current and Voltage with Frequency, Selectivity and Bandwidth, Q-Factor, Circuit Magnification Factor, Selectivity with Variable Capacitance, Selectivity with Variable Inductance. **Parallel Resonance:** Selectivity and Bandwidth, Maximum Impedance Conditions with C, L and f Variable, current in Anti-Resonant Circuit, The General Case-Resistance Present in both Branches.	**10 Hours**	**L1 ,L2,L3 ,L4**

5.0 Relevance to future subjects

Sl No	Semester	Subject	Topics
01	V	Analog Communication	Network analysis concepts
02	VI	CMOS VLSI design	Network analysis concepts

6.0 Relevance to Real World

SL. No	Real World Mapping
01	Analyze different types of Network
02	Design of different types of Networks

7.0 Gap Analysis and Mitigation

Sl. No	Delivery Type	Details
01	Tutorial	Topic: Network Analysis
02	NPTEL	Application

8.0 Books Used and Recommended to Students

Text Books

1. M.E. Van Valkenberg (2000), "Network analysis", Prentice Hall of India, 3rd edition, 2000, ISBN: 9780136110958.
2. 2. Roy Choudhury, "Networks and systems", 2nd edition, New Age International Publications, 2006, ISBN: 9788122427677.

Reference Books

1. Hayt, Kemmerly and Durbin "Engineering Circuit Analysis", TMH 7th Edition, 2010.
2. J.David Irwin/R.Mark Nelms,",Basic Engineering Circuit Analysis",John Wiley,8 th ed,2006
3. Charles K Alexander and Mathew N O Sadiku,"Fundamentals of Electric circuits",Tata McGraw-Hill,3 rd edition,2009

Additional Study material & e-Books

1. J. David Irwin /R. Mark Nelms, "Basic Engineering Circuit Analysis", John Wiley, 8th edition, 2006
2. VTU on line notes.

9.0 Relevant Websites (Reputed Universities and Others) for Notes/Animation/Videos Recommended

Website and Internet Contents References

01) https://nptel.co.in
02) http://m.noteboy.in/vtuflies/machine%20drawing.pdf

10.0 Magazines/Journals Used and Recommended to Students

Sl. No	Magazines/Journals	Website
1	IEEE Xplorer	http://ieee.com
2	International Journal of Science and Technology	http://www.sciencedirect.com/science/journal/00207683
3	Journal of Communication Engineering	http://ieee.com

11.0 Examination Note

Internal Assessment: 40 Marks
Three IA will be conducted and average of three will be accounted.

Scheme of Evaluation for Internal Assessment (40 Marks)
30 marks for IA Test & 10 marks for Assignment.

SCHEME OF EXAMINATION:
Two main questions to be set from the syllabus covered.
Question 1 or 2
Answer both main questions.
Question 1 = 15 marks.
Question 2 = 15 marks.
Total = 30 marks

12.0 Course Delivery Plan

Course Delivery Plan:

MODULE	LECTURE NO.	CONTENT OF LECTURE	% OF PORTION
1	1	Practical sources	20
	2	Source transformations	
	3	Network reduction using Star – Delta transformation	
	4	Loop analysis With linearly dependent and independent sources for DC Networks.	
	5	Loop analysis With linearly dependent and independent sources for DC Networks.	
	6	Loop analysis With linearly dependent and independent sources for AC Networks.	
	7	Loop analysis With linearly dependent and independent sources for AC Networks.	
	8	Node analysis With linearly dependent and independent sources for DC networks	
	9	Node analysis With linearly dependent and independent sources for AC networks	
	10	Problems	
2	1	Superposition theorem,	40
	2	Problems on Superposition Theory	
	3	Thevenins theorem	
	4	Problems on Thevenins theorem	
	5	Nortons Theorem	
	6	Problems on Nortons Theorem	
	7	Millimans Theorem	
	8	Problems on Millimans Theorem.	
	9	Maximum power transfer Theorem	
	10	Problems on Maximum power transfer Theorem	
3	1	Behavior of circuit elements under switching conditions and their representation	60
	2	Behavior of circuit elements under switching conditions and their representation	
	3	Behavior of circuit elements under switching conditions and their representation	
	4	Behavior of circuit elements under switching conditions and their representation	
	5	Evaluation of initial and final conditions in RL circuits for DC excitations	
	6	Evaluation of initial and final conditions in RC circuits for DC excitations	
	7	Evaluation of initial and final conditions in RLC circuits for DC excitations	
	8	Evaluation of initial and final conditions in RL circuits for AC excitations	
	9	Evaluation of initial and final conditions in RC circuits for AC excitations	
	10	Evaluation of initial and final conditions in RLC circuits for AC excitations	
4	1	Solution of networks, Step response	80
	2	Solution of networks, Step response	
	3	Solution of networks, Ramp response	
	4	Solution of networks, Ramp response	
	5	Solution of networks, Impulse response	
	6	Solution of networks, Impulse response	

	7	Waveform Synthesis.	
	8	Waveform Synthesis.	
	9	Waveform Synthesis.	
	10	Waveform Synthesis.	
5	1	Definition of z, y, h parameters	100
	2	Definition of transmission parameters	
	3	Modeling with these parameters	
	4	Relationship between parameter sets.	
	5	Series Resonance: Variation of Current and Voltage with Frequency.	
	6	Selectivity and Bandwidth, Q-Factor, Circuit Magnification Factor	
	7	Selectivity with Variable Capacitance, Selectivity with Variable Inductance	
	8	Parallel Resonance: Selectivity and Bandwidth	
	9	Maximum Impedance Conditions with C, L and f Variable current in Anti-	
	10	The General Case-Resistance Present in both Branches	

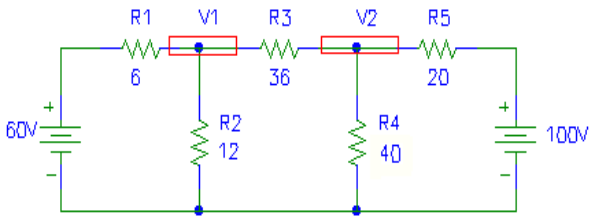
13.0 Assignments, Pop Quiz, Mini Project, Seminars

Sl. No.	Title	Outcome expected	Allied study	Week No.	Individual / Group activity	Reference: book/website /Paper
1	Assignment 1: University Questions on Basic Concepts	Students study the Topics and write the Answers. Get practice to solve university questions.	Module 1 of the syllabus	2	Individual Activity. Printed solution expected.	Book 1, 2 of the reference list. Website of the Reference list
2	Assignment 2: University Questions on Network theorems	Students study the Topics and write the Answers. Get practice to solve university questions.	Module 2, of the syllabus	4	Individual Activity. Printed solution expected.	Book 1, 2 of the reference list. Website of the Reference list
3	Assignment 3: University Questions on Transient Behavior & Initial Conditions, Laplace transformation and application	Students study the Topics and write the Answers. Get practice to solve university questions.	Module 3 of the syllabus	6	Individual Activity. Printed solution expected.	Book 1, 2 of the reference list. Website of the Reference list
4	Assignment 4: University Questions Resonant Circuits and Two port network parameters.	Students study the Topics and write the Answers. Get practice to solve university questions.	Module 4 of the syllabus	8	Individual Activity. Printed solution expected.	Book 1, 2 of the reference list. Website of the Reference list
5	Assignment 5: University Questions Resonant Circuits and Two port network parameters.	Students study the Topics and write the Answers. Get practice to solve university questions.	Module 5 of the syllabus	12	Individual Activity. Printed solution expected.	Book 1, 2 of the reference list. Website of the Reference list

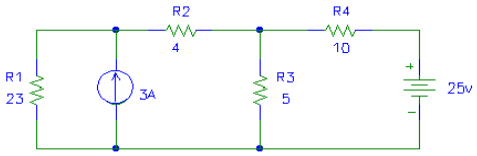
14.0 QUESTION BANK

MODULE -1

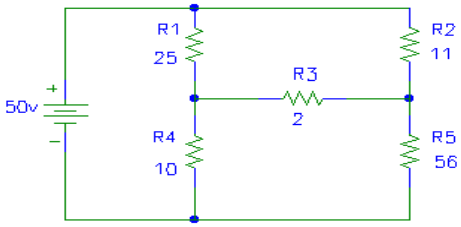
1. State Ohm's law and its limitations.
2. Name different network elements.
3. What is meant by Electric Circuits?
4. State two salient points of a series combination of resistance.
5. State two salient points of a parallel combination of resistance
6. Give two applications of both series and parallel combination.
7. State Kirchhoff's law.
8. Give two applications of both series and parallel combination.
9. Find the equivalent current source for a voltage source of 100 V with series resistance of 2 ohm.
10. Write the expression for converting delta connected resistances into an equivalent star connected resistances.
11. A Y-connected resistive network consists of 2 ohm in each arm. Draw the equivalent delta-connected network and Define the dependent source of a circuit.
12. Write the voltage division and current division rule.
13. What is meant by Mesh Analysis?
14. What is meant by Nodal analysis?
15. Define an ideal voltage source.
16. Define an ideal current source
17. Draw the symbolic representation of the voltage source and current source.
18. Explain how voltage source with a source resistance can be converted into an equivalent current source.
19. Explain how current source with a parallel resistance can be converted into an equivalent voltage source.
20. Define the dependent source of a circuit.
21. Define the current division rule
22. A bulb is as rated 230V, 230W. Find the rated current, resistance of the filament and the energy consumed when it is operated for 10 hours.
23. Draw the V-I relationship of an ideal voltage source
24. Find the node voltages V1 and V2.



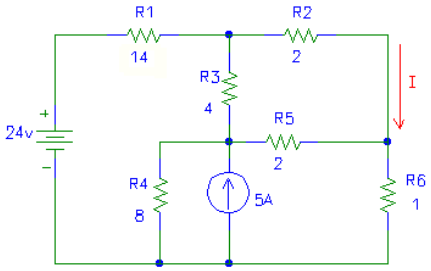
25. Find the current through R2 and R3 using mesh analysis.



26. Find the voltage across R3 using Nodal analysis.

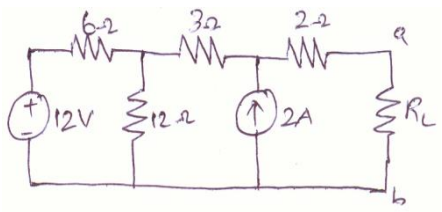


27. Find the current labeled "I" using both mesh and node analysis.

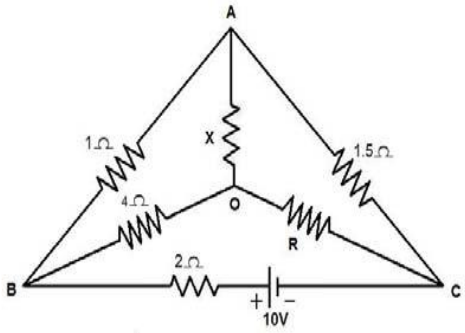


MODULE -2

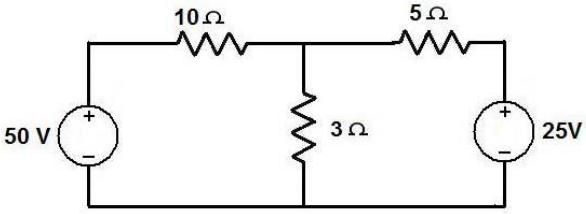
1. State Superposition theorem.
2. State and Explain Thevenin's Theorem.
3. State and explain Norton's theorem.
4. State Maximum Power Transfer Theorem.
5. Determine Thevenin's equivalent across the terminals AB for the circuit shown in figure below.
6. State reciprocity theorem.
7. Write some applications of Maximum power transfer theorem.
8. The power delivered is maximum, if the load impedance is equal to the supply circuit impedance – True or False.
9. What is the condition for maximum power transfer?
10. Find the value of RL for maxim um power transfer in the circuit of figure. Find the maximum power



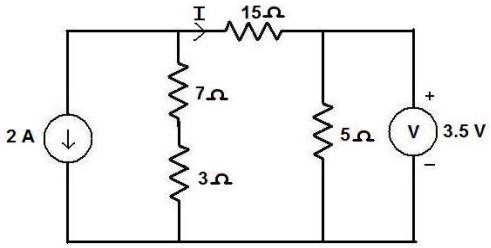
11. (i) Find the value of R and the current flowing through it in the circuit shown when the current in the branch OA is zero.



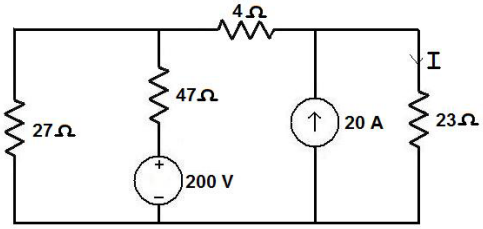
12. Find the current in each resistor using superposition principle of figure.



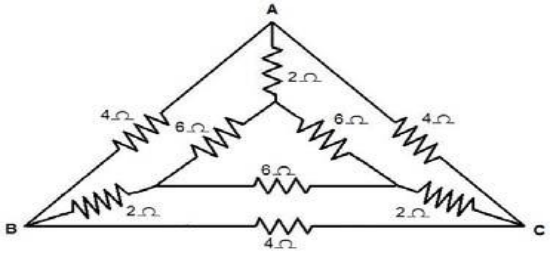
13. For the circuit shown, use superposition theorem to compute current I.



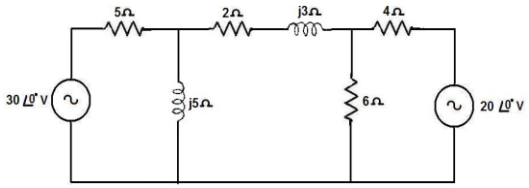
14. (i)Compute the current in 23 ohm resistor using super position theorem for the circuit shown below.



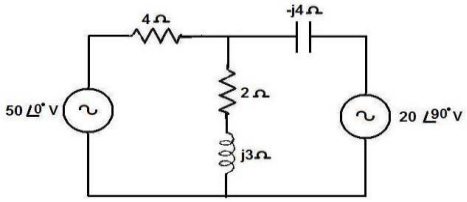
(ii) Find the equivalent resistance between B and C in figure



15. Using superposition theorem calculate current through (2+j3) ohm impedance branch of the circuit shown.



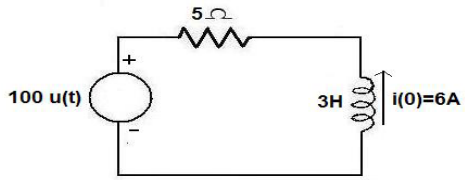
16. For the circuit shown, determine the current in (2+j3) ohm by using superposition theorem.



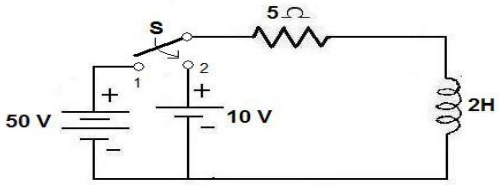
MODULE -3

1. The transients are due to the presence of energy storing elements in the circuit –True or false.
2. What is a step function?
3. What is an initial condition?
4. What is a transient?
5. What is the steady state value?
6. Write the transient current equation when RL series circuit is connected to a step voltage of volts.
7. A DC voltage of 100 volts is applied to a series RL circuits with R = 25 ohm what will be the current in the circuit in the circuits at twice the time constant?
8. Sketch the current given by I (t) = 5 – 4 e-20 t.
9. Distinguish between free and forced response.
10. Draw the equivalent circuit for inductor and capacitor at t = 0+ when there is no initial energy.
11. Define a time constant of a RL circuit.
12. Draw the equivalent circuits for the inductor and capacitor at t=0+ with presence of initial energy.
13. Distinguish between the steady state and the transient response of an electrical circuit.
14. Define a time constant of a RC circuit.
15. Draw the equivalent circuit at t = 0+ for a capacitor with initial charge of q 0.
16. Sketch the response of RC network for a unit step input.
17. What are the periodic inputs?
18. What are critical frequencies? Why are they so called?
19. Draw the transient response of R-L circuits for step input.
20. Define the time constant of a transient response.
21. Find the time constant of RL circuits having R = 10 ohm and L = 0.1 mH.
22. What is meant by critical damping?

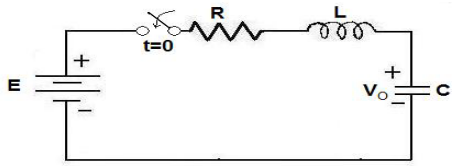
23. In the circuit of the figure shown below, find the expression for the transient current and the initial rate of growth of the transient current .



24. In the circuit shown in figure, switch S is in position 1 for a long time and brought to position 2 at time t=0. Determine the circuit current.



25. A resistance R and 2 microfarad capacitor are connected in series across a 200V direct supply. Across the capacitor is a neon lamp that strikes at 120V. Calculate R to make the lamp strike 5 sec after the switch has been closed. If R = 5Megohm,how long will it take the lamp to strike?
26. A Series RLC circuits has R=50 ohm, L= 0.2H, and C = 50 microfarad. Constant voltage of 100V is impressed upon the circuit at t=0. Find the expression for the transient current assuming initially relaxed conditions.
27. A Series RLC circuits with R=300 ohm, L=1H and C=100x10-6 F has a constant voltage of 50V applied to it at t= 0. Find the maximum value of current (Assume zero initial conditions)
28. A step voltage V(t) = 100 u(t) is applied to a series RLC circuit with L=10H, R=2ohm and C= 5F. The initial current in the circuit is zero but there is an initial voltage of 50V on the capacitor in a direction which opposes the applied source. Find the expression for the current in the circuit.



29. In the circuit shown in Fig.6.56, the switch is thrown from position 1 to 2 at t = 0.Just before the switch is thrown, the initial conditions are i(O-) =2A and vc(O-) =2V. Find i(t) after the switching action, using Laplace transform method.

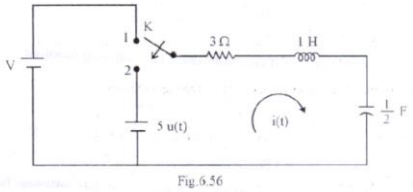


Fig.6.56

30. In the circuit shown in Fig.6.57, the switch. is closed at t. = 0, with zero initial conditions. Find i(t) using L.T. method.

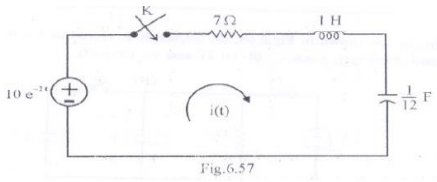


Fig.6.57

31. In the circuit shown in Fig.6.58, find i_2 (t) after the switch is closed at t = 0, using transformed circuit.

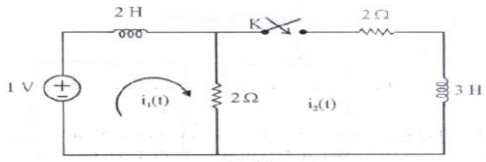


Fig.6.58

32. In the circuit shown in 6.59,the switch is closed at t=0, find V_L(t) using transformed circuit.

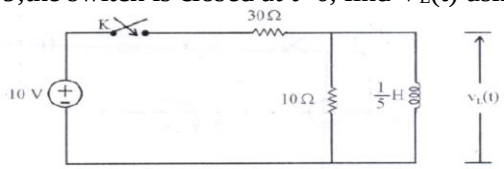


Fig.6.59

33. In the circuit shown in Fig.6.60, the switch K is closed at t = 0, after steady state is reached. Find v(t), given $V_{C1}(0-) = 2V$ and $v_{C2}(0-) = 0$ v .

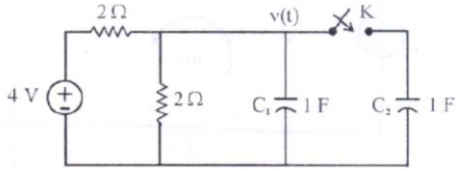


Fig.6.60

34. At t = 0, the switch K is opened in the network shown in Fig.6.61. Find the value of V1 (t) and V2 (t) for all t > 0, using L.T method.

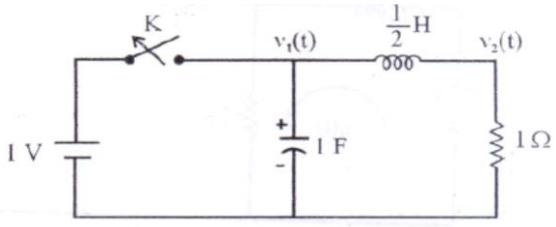


Fig.6.61

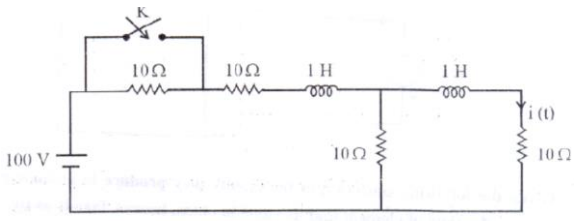


Fig.6.64

MODULE -4

1. A pulse voltage of width 'a' and magnitude 20 V is applied at t = 0, to an R-L series circuit consisting of R =5Ω and L =3H. Find i (t) using L.T method. Assume zero initial conditions.
2. A voltage pulse of width 'a' and magnitude 10 V is applied at t =0 to an R-C series circuit consisting of R =1 Ω and C =1/5F. Find i(t). Assume zero charge on C, before the application of the voltage pulse.
3. Find the response current of a series R-L circuit consisting of R =4 Ω and L =2 H, when each of the Following driving force voltages are applied.
4. i) Unit ramp voltage r *(t* - 5) ii) Unit impulse voltage δ *(t* - 5) iii) Unit step voltage u (t) - Assume zero initial conditions.
5. Find the current i(t) in a series R-C circuit consisting of R =4 Ω and C =1/5 F, when each of the following voltages are applied. Assume zero initial conditions.
6. i) r *(t* - 2) ii) u *(t* - 2) iii)δ *(t* - 2)

7. Find the impulse response in the circuit shown in Fig.6.65, if the output is V_L (t).

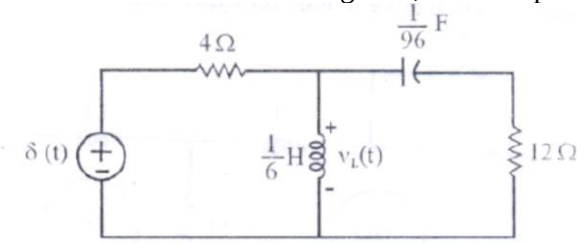


Fig.6.65

8. The network shown in Fig.6.66 is initially in relaxed state. When the source is 10 u (t) volts, the transform of the input current is 10 / (2s + 4). The circuit is brought to its initial state once again. Find the impedance and input response Vs(t), when the source is a current generator of 5 e^{-2t} amperes.

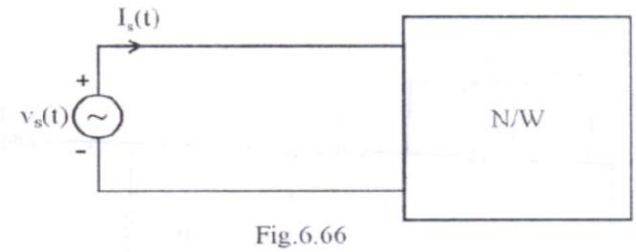


Fig.6.66

9. Given the following sources and the results they produce in a single element circuit. Deduce the type of element and its value in-ohms, henrys, farads as the case may be. If the source is a voltage, the response is current and vice versa.

	Source	Response
i)	i (t) = 5 δ(t)	10 u(t)
ii)	i (t) = 5 u(t)	3 δ(t)
iii)	e (t) = 10 u(t)	5 δ(t)
iv)	i (t) = 3/2 δ(t)	9/4 δ(t)
v)	e(t) = 1/3 δ(t)	3 u(t)

10. The periodic current waveform is as shown in Fig.6.67. Find its Laplace transform equation.

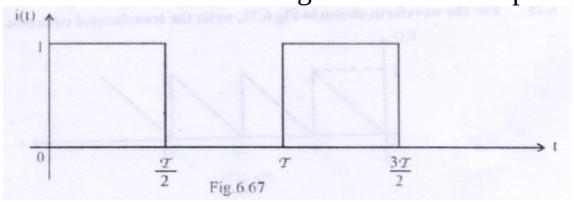


Fig.6.67

11. Find the Laplace transform of the following functions.
    i) $10\,t^3 - 5\cos 3t + 8\sin t$ ii) $e^{-3t}\sin^3 3t$ iii) $t\cos(wt+\theta)$
    iv) $e^{3t}\cos^3 2t$ v) $t^2 e^{-at}\cos wt$

12. Find the inverse Laplace transforms of the following questions:

i) $\dfrac{2s+6}{s^2+6s+5}$ ii) $\dfrac{2s}{(s^2+4)(s^2+5)}$ iii) $\dfrac{s+5}{s^2+2s+5}$

iv) $\dfrac{1}{(s+1)(s+1)^2}$ v) $\dfrac{s^3-s^2-3s+9}{(s+2)(s^2+4)}$ vi) $\dfrac{s+2}{s^2-4s+12}$

vii) $\dfrac{2s^2-6s+5}{s^3-6s^2+11s-6}$ viii) $\dfrac{s^3-s^2-3s+9}{s^2(s^2+9)}$

13. Solve the following differential equations using Laplace transform method.

i) $\dfrac{d^2i}{dt^2} + 4\dfrac{di}{dt} + 8i = 8\,u(t)$, given $i(0+) = 3$ and $\dfrac{di}{dt}(0+) = -4$

ii) $\dfrac{d^2x}{dt^2} - 2\dfrac{dx}{dt} + x = e^t$, given $x(0+) = 2$ and $x^1(0+) = -1$

iii) $\dfrac{d^2i}{dt^2} + 2\dfrac{di}{dt} + 4i = -4\sin 2t$, given $i(0+) = 1$ and $i(0+) = -1$

iv) $\dfrac{d^2i}{dt^2} + 4\dfrac{di}{dt} + 3i = -12\,e^{-3t}$, given $i(0+) = 0$ and $i^1(0+) = 4$

v) $2\dfrac{d^3i}{dt^3} + 9\dfrac{d^2i}{dt^2} + 13\dfrac{di}{dt} + 6i = 0$, given $i(0+) = 0$, $i^1(0+) = 1$ and $i^{11}(0+) = -1$

14. Find the initial and final values of the following functions:

i) $\dfrac{1}{s(s^2-a^2)}$ ii) $\dfrac{s^3+7s^2+5}{s(s^3+3s^2+4s+s)}$ iii) $\dfrac{2s+3}{(s+1)(s+3)}$ iv) $\dfrac{e^{-2s}(s+2)}{s^3+5s}$

v) $\dfrac{2(s+1)(s+3)}{(s+2)(s+6)}$ vi) $\dfrac{(s+1)\sin\theta + b\cos\theta}{(s+a)^2+b^2}$ vii) $\dfrac{8(s^2+2s+1)}{(s+2)(s^2+4)}$

15. Find the inverse Laplace transform of the following functions, using convolution theorem.

i) $\dfrac{s}{(s^2-a^2)^2}$ ii) $\dfrac{s}{(s^2+a)(s^2+25)}$ iii) $\dfrac{1}{s(s^2-a^2)}$ iv) $\dfrac{s+1}{s(s^2+4)}$ v) $\dfrac{5}{s^2(s+2)^2}$

16. Using convolution theorem, find v(t), in the circuit shown in Fig.6.54.

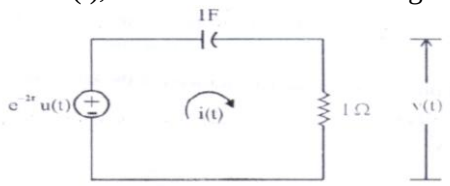
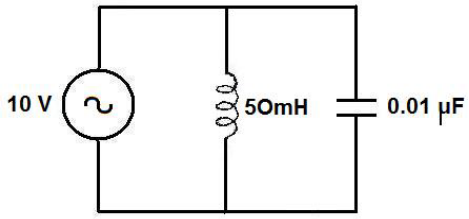


Fig. 6.54

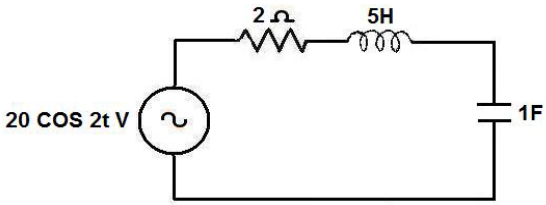
MODULE -5

A. RESONANCE

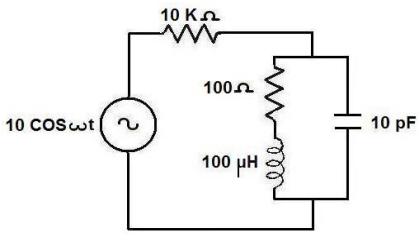
1. Define Q-factor of a coil.
2. Define bandwidth of a resonant circuit.
3. Find the resonant frequency in the ideal parallel LC circuit shown below



4. Find the impedance offered to the source by the load.



5. State the condition for resonance in RLC series circuit.
6. A resistance 5 ohms, inductance 0.02H and capacitor 5 microfarads are connected in series. Find the resonance frequency and the power factor at resonance.
7. Two capacitances C1 and C2 of values 10μF and 5μF are connected in series. What is the equivalent capacitance of this combination?
8. Derive bandwidth for a series RLC circuit as a function of resonant frequency.
9. (i) For the circuit below, find the value of ω so that current and source emf are in phase. Also find the current at this frequency.



(ii) Discuss the characteristics of parallel resonance of a circuit having G,L and C.

10. (i) A Pure resistor, a pure capacitor and a pure inductor are connected in parallel across a 50Hz supply, find the impedance of the circuit as seen by the supply. Also find the resonant frequency.
    (ii) When connected to a 230V, 50Hz single phase supply, a coil takes 10kVA and 8kVAR. For this coil calculate resistance, inductance of coil and power consumed.
11. (i) In an RLC series circuit if ω1 and ω2 are two frequencies at which the magnitude of the current is the same and if ωr is the resonant frequency, prove that $\omega r^2 = \omega 1 \omega 2$.
    (ii) A series RLC circuit has Q = 75 and a pass band (between half power frequencies) of 160 Hz. Calculate the resonant frequency and the upper and lower frequencies of the pass band.
12. (i) Explain and derive the relationships for bandwidth and half power frequencies of RLC series circuit.
    (ii) Determine the quality facto of a coil R = 10 ohm, L = 0.1H and C = 10 μf
13. A series RLC circuit has R=20 ohm, L=0.005H and C = 0.2 x 10-6 F. It is fed from a 100V ariable frequency source. Find i) frequency at which current is maximum ii) impedance at this frequency and
    iii) voltage across inductance at this frequency.
14. A series RLC circuit consists of R=100 ohm, L = 0.02 H and C = 0.02 microfarad. Calculate frequency of resonance.
    A variable frequency sinusoidal voltage of constant RMS value of 50V is applied to the circuit. Find the frequency at which voltage across L and C is maximum. Also calculate voltage across L and C is maximum. Also calculate voltages across L and C at frequency of resonance. Find maximum current in the circuit.
15. In the parallel RLC circuit, calculate resonant frequency, bandwidth, Q-factor and power dissipated at half power frequencies.

B. Two Port Networks

1. For the network of Fig. 7.69, find z-parameters. Hence find y-parameters, Find whether the network is Reciprocal and symmetrical.

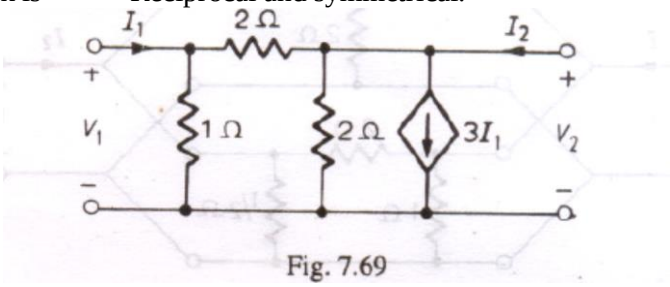


Fig. 7.69

2. For the network of Fig. 7.70, find y-parameters. Hence find z-parameters. Find whether the network is reciprocal and symmetrical

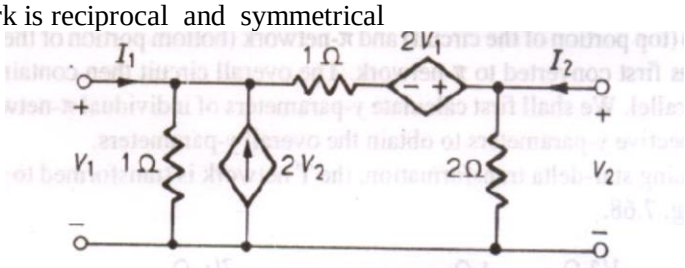


Fig. 7.70

3. For the network of Fig. 7.71 find the h-parameters. Hence find g-parameters. Find whether the network is reciprocal and symmetrical.

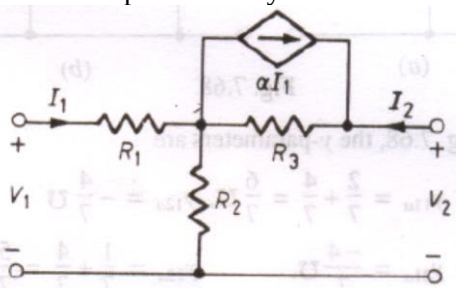


Fig. 7.71

4. For the network shown in Fig. 7.72 find the transmission *(ABCD)* parameters. Find whether the network is reciprocal and symmetrical.

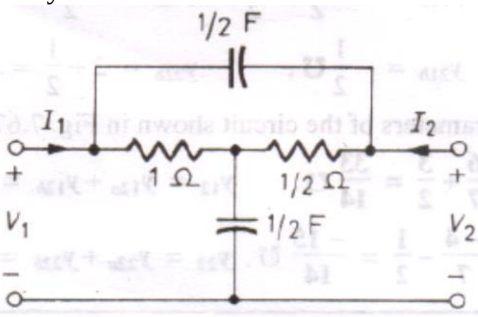


Fig. 7.72

5. The z-parameters of a certain two-port network are Z_{ll}=5 , Z_{12}=Z_{21} =3 ,Z_{22}=4. Find

   (a) ABCD parameters (b)abcd parameters (c)h parameters (d) g parameters.

6. The transmission (ABCD) parameters of a certain two-port network are A = 1,B = 2,C = 1 and D = 3.

7. Calculate (a) z-parameters (b) h-parameters. Is the network (i) reciprocal (ii) symmetrical?

8. A symmetrical lattice network has series arm impedance of 5 ohm and cross-arm impedance of 10Ohm.

   Find (a) z-parameters (b) image parameters.

9. For the network shown in Fig. 7.73, find (a) h-parameters (b) ABCD parameters (c) z-parameters.

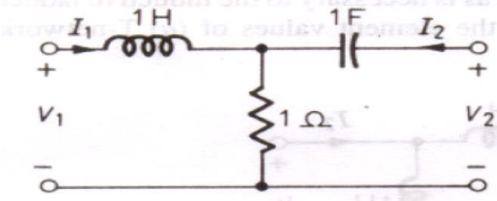


Fig. 7.73

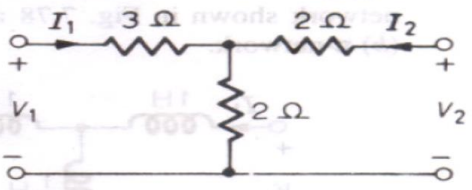


Fig. 7.74

10. Starting from fundamentals calculate the Network parameters of the network shown in Fig. 7.74.

11. Obtain the y-parameters of the network shown in Fig. 7.75 considering it as a parallel combination of two circuits.

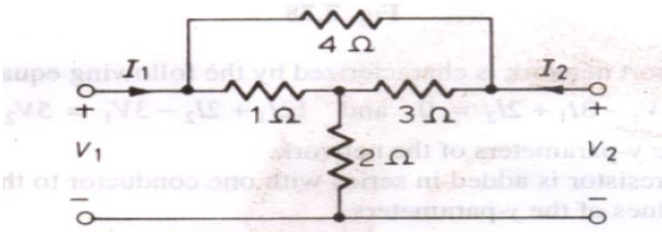


Fig. 7.75

12. For the network shown in Fig. 7.77, calculate the y-parameters.

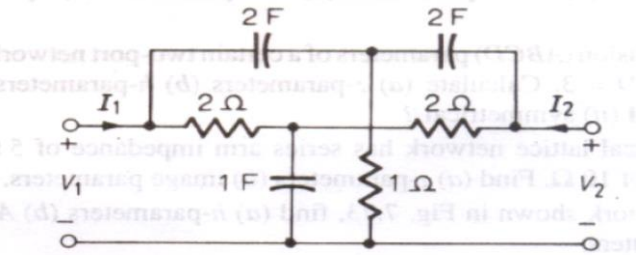


Fig. 7.77

13. (a) A two-port network is characterized by the following equations

$$6V_1 - 3I_1 + 2I_2 = 0 \quad \text{and} \quad 12I_1 + 2I_2 - 3V_1 = 5V_2$$

Find the y-parameters of the network.

(b) A 5-il resistor is added in series with one conductor to the output port. Find new values of the y-parameters.

14. The block N of the network shown in Fig. 7.79 has following z-parameters :

$$z_{11} = 0.1\ \text{k}\Omega,\ z_{12} = -0.5\ \text{k}\Omega,\ z_{21} = 1\ \text{k}\Omega,\ z_{22} = 10\ \text{k}\Omega.$$

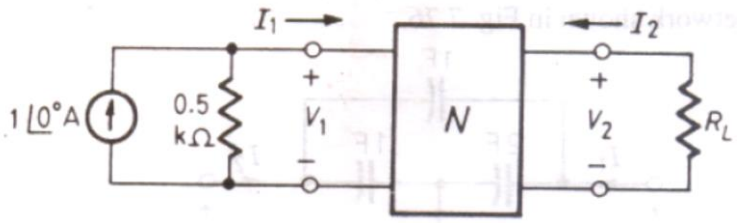


Fig. 7.79

a. Find the r m s value of voltage across R_L if R_L=5 kΩ

b. Find the optimum value of R_L which would result in maximum power being delivered to it.

c. Find the y-parameters of the block N.

15. Find the z-parameters of the network shown in Fig. 7.80.

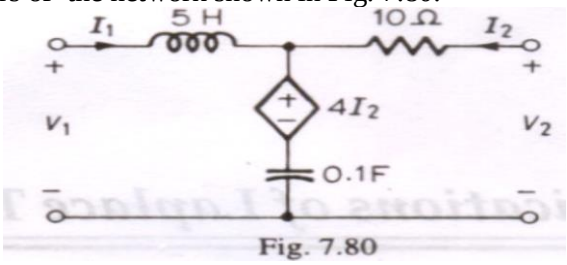


Fig. 7.80

16. The two-port network *N* shown in Fig. 7.81 has following h-parameters :

$h_{11} = 1\ \text{k}\Omega,\ h_{12} = 0.0015,\ h_{21} = 100,\ h_{22} = 100\ \mu\text{℧}$.

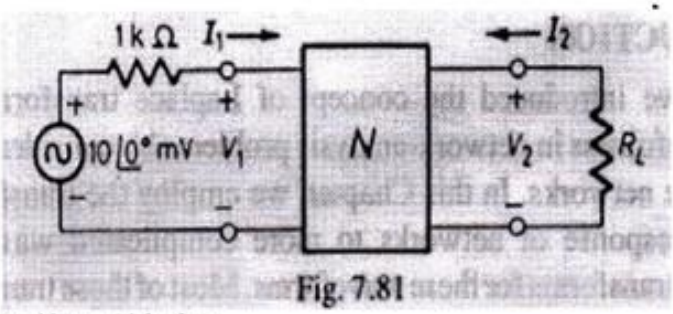


Fig. 7.81

(a) Find the output voltage V_2 if R_L= 10 k ohm.
(b) Find R_L which would result in maximum power being delivered to it.
(c) Find z-parameters of the two port network N.

17. Determine the input impedance Z_{in} of a two-port network, if a load resistor of 4 ohm is connected across its output port. The z-parameters of the network are

$z_{11} = 5\ \Omega,\ z_{12} = z_{21} = 3\ \Omega,\ z_{22} = 2\Omega$

18. The network equations for a two-port network give the currents I_1 and I_2 at the two ports as

$$I_1 = 0.25V_1 - 0.2V_2 \quad \text{and} \quad I_2 = -0.2V_1 + 0.1V_2$$

Determine the transmission *(ABCD)* parameters for the network and hence write the network equations Using these parameters.

19 . For the resistive network shown in Fig. 7.82, calculate the y-parameters.

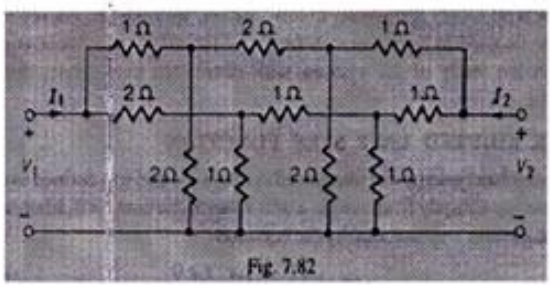


Fig. 7.82

Examination	S+	S	A	B	C	D	E	F	% Passing
Mar-2021	-	-	-	-	-	-	-	05	83.33
Mar-2022	-	-	-	-	-	-	26	20	56.52

Prepared by	Checked by		
Prof.P.V.Patil	Prof.D.M.Kumbhar	HOD Electronics & Commn. Engg. Dept HSIT NIDASOSHI HOD	Principal

Subject Title	**Analog and Digital Electronics Lab**		
Subject Code	**BECL305**	**CIE Marks**	50
Number of Lecture Hrs/Week /	02 Hours Laboratory	**SEE Marks**	50
RBT Level	L1, L2, L3	**Exam Hours**	03
CREDITS – 01			

FACULTY DETAILS:		
Name: Prof. S.S.Malaj	**Designation:** Assistant Professor	**Experience :Teach- 25** years
No. of times course taught: 00	**Specialization:** Digital Electronics	

1.0 Prerequisite Subjects:

Sl. No	Branch	Semester	Subject
01	ECE	I & II	Analog Electronics Circuits
02	ECE	I & II	Op-Amp
03	ECE	I & II	Digital Electronics

Sl. No	Branch	Semester	Subject
01	Students should have the knowledge of basic subjects	I & II	Basic electrical & electronics subjects

2.0 Course Objectives

This laboratory course enables students to

- Understand the electronic circuit schematic and its working
- Realize and test amplifier and oscillator circuits for the given specifications
- Realize the op-amp circuits for the applications such as DAC, implement mathematical functions and precision rectifiers.
- Study the static characteristics of SCR and test the RC triggering circuit.
- Design and test the combinational and sequential logic circuits for their functionalities.
- Use the suitable ICs based on the specifications and functions.

3.0 Course Outcomes

Having successfully completed this course, the student will be able to

	Course Outcome	Cognitive Level	PO's
CO1	Design and analyze the BJT/FET amplifier and oscillator circuits.	U	1,2,3,4,5,6,7,8,9, 10,11,12
CO2	Design and test Op-amp circuits to realize the mathematical computations, DAC and precision rectifiers.	U	1,2,3,4,5,6,7,8,9, 10,11,12
CO3	Design and test the combinational logic circuits for the given specifications.	U	1,2,3,4,5,6,7,8,9, 10,11,12
CO4	Test the sequential logic circuits for the given functionality.	U	1,2,3,4,5,6,7,8,9, 10,11,12
CO5	Demonstrate the basic circuit experiments using 555 timers.	U	1,2,3,4,5,6,7,8,9, 10,11,12
Total Hours of instruction		**40**	

4.0 Course Content

Laboratory Experiments:

1	Design and set up the BJT common emitter voltage amplifier with and without feedback and determine the gain- bandwidth product, input and output impedances.
2	Design and set-up BJT/FET i) Colpitts Oscillator, ii) Crystal Oscillator
3	Design and setup the circuits using op-amp: i)Adder, ii)Integrator, iii)Differentiator and iv) Comparator
4	Design 4 bit R – 2R Op-Amp Digital to Analog Converter (i) using 4 bit binary input from toggle switches and (ii) by generating digital inputs using mod-16 counter.
5	Design and implement (a) Half Adder & Full Adder using basic gates and NAND gates, (b) Half subtract or & Full subtract or using NAND gates, (c) 4-variable function using IC74151 (8:1MUX).
6	Realize (i) Binary to Gray code conversion & vice-versa (IC74139), (ii) BCD to Excess-3 code conversion and vice versa
7	a) Realize using NAND Gates: i) Master-Slave JK Flip-Flop, ii) D Flip-Flop and iii)T Flip-Flop b) Realize the shift registers using IC7474/7495: (i) SISO (ii) SIPO (iii) PISO (iv) PIPO (v) Ring counter and (vi) Johnson counter.
8	Realize a) Design Mod –N Synchronous Up Counter & Down Counter using 7476 JK Flip-flop b) Mod-N Counter using IC 7490/7476 c) Synchronous counter using IC 74192
9	Design and Test second-order Active Filters and plot the frequency response. d) Low pass Filter e) High Pass Filter.
10	Design and test the following using 555 Timer i) Monostable Multivibrator. ii) Astable Multivibrator
11	Design and Test a Regulated Power supply.
12	Design and test an audio amplifier by connecting a microphone input and observe the output using a loud speaker.

5.0 Relevance to future subjects

Sl. No	Semester	Subject	Topics
01	VII/VIII	Project work	Analog & Digital Circuits based concept

6.0 relevance to real world

SL No	Real World Mapping
01	Design analog circuits using OPAMPs for different applications
02	Design digital circuits using digital IC's for different applications
02	Hobby/Mini projects
03	Home appliances/controlling of equipments.

7.0 Gap Analysis and Mitigation

Sl. No	Delivery Type	Details
01	Tutorial	Topic: Simulation software like Simulink, PSpice and Proteus.
02	NPTEL	Assembly Application

8.0 Books Used and Recommended to Students

Text Books

3. Fundamentals of Electronic Devices and Circuits Lab Manual, David A Bell, 5th Edition, 2009, Oxford University Press.
4. Op-Amps and Linear Integrated Circuits, Ramakant A Gayakwad, 4th Edition, Pearson Education, 2018. ISBN: 978-93-325-4991-3.
5. Fundamentals of Logic Design, Charles H RothJr., Larry L Kinney, Cengage Learning, 7th Edition.

9.0 Relevant Websites (Reputed Universities and Others) for Notes/Animation/Videos Recommended

Website and Internet Contents References

10) https://nptel.co.in
11) http://m.noteboy.in/vtuflies/machine%20drawing.pdf

10.0 Magazines/Journals Used and Recommended to Students

Sl.No	Magazines/Journals	website
1	IEEE Xplorer	http://ieee.com
2	International Journal of Science and Technology	http://www.sciencedirect.com/science/journal/00207683
3	Journal of Communication Engineering	http://ieee.com

11.0 Examination Note

Assessment Details (both CIE and SEE)

The weight age of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation (CIE):

CIE marks for the practical course are 50 Marks.

The split-up of CIE marks for record/ journal and test are in the ratio 60:40.

- Each experiment is to be evaluated for conduction with an observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments are designed by the faculty who is handling the laboratory session and are made known to students at the beginning of the practical session.
    - Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated• for 10 marks.
    - Total marks scored by the students are scaled down to 30 marks (60% of maximum marks).
- Weight age to be given for neatness and submission of record/write-up on time.
- Department shall conduct a test of 100 marks after the completion of all the experiments listed in the syllabus.
- In a test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a• weight age of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.
- The marks scored shall be scaled down to 20 marks (40% of the maximum marks)
- The Sum of scaled-down marks scored in the report write-up/journal and marks of a test is the total CIE marks scored by the student.

2.0 Course Delivery Plan

Experiment	Lecture No.	Content	% of Portion
1	1	Design and set up the BJT common emitter voltage amplifier with and without feedback and determine the gain- bandwidth product, input and output impedances.	7
2	2	Design and set-up BJT/FET i) Colpitts Oscillator, ii) Crystal Oscillator	14
3	3	Design and setup the circuits using op-amp: i)Adder, ii)Integrator, iii)Differentiator and iv) Comparator	21
4	4	Design 4 bit R – 2R Op-Amp Digital to Analog Converter (iii) using 4 bit binary input from toggle switches and (iv) by generating digital inputs using mod-16 counter.	29
5	5	Design and implement (d) Half Adder & Full Adder using basic gates and NAND gates, (e) Half subtractor & Full subtractor using NAND gates, (f) 4-variable function using IC74151 (8:1MUX).	36
6	6	Realize (iii) Binary to Gray code conversion & vice-versa (IC74139), (iv) BCD to Excess-3 code conversion and vice versa	43
7	7	c) Realize using NAND Gates: i) Master-Slave JK Flip-Flop, ii) D Flip-Flop and iii)T Flip-Flop d) Realize the shift registers using IC7474/7495: (i) SISO (ii) SIPO (iii) PISO (iv) PIPO (v) Ring counter and (vi) Johnson counter.	50
8	8	Realize a) Design Mod –N Synchronous Up Counter & Down Counter using 7476 JK Flip-flop b) Mod-N Counter using IC 7490/7476 c) Synchronous counter using IC 74192	64
9	9	Design and Test second-order Active Filters and plot the frequency response. f) Low pass Filter g) High Pass Filter.	72
10	10	Design and test the following using 555 Timer i) Monostable Multivibrator. ii) Astable Multivibrator	86
11	11	Design and Test a Regulated Power supply.	93
12	12	Design and test an audio amplifier by connecting a microphone input and observe the output using a loud speaker.	100

13.0 VIVA BANK

41. Define amplifier. Why it is called as RC Coupled amplifier.
42. What is the difference between With and Without Feddback.
43. What is meant by input and output impedance.
44. Define Oscillator.
45. What are the advantages of integrated circuits?
46. What are the popular IC packages available
47. What is an operational amplifier
48. What is the Internal Structure of op-amp and explain each block in brief?
49. What are the characteristics of an ideal op-amp
50. What are the DC, AC Characteristics of OP-Amp?
51. What is input offset voltage?
52. Define input offset current.
53. Define CMRR of an opamp ?
54. What is the effect of high frequency on its performance?
55. What is the need for frequency compensation in practical op-amps?
56. What are the frequency compensation methods?
57. Define slew rate.
58. Can we use IC 741 for high frequency applications?
59. Why slew rate is not infinite in Ideal op-amp?
60. What are the applications of op-amps?
61. What are the limitations of the basic differentiator circuit?
62. What are the limitations of the basic Integrator circuit?
63. What is a comparator?
64. What are the applications of comparator?
65. Why can't we use comparator to convert sin wave into square wave?
66. What is a multivibrator?
67. What is monostable multivibrator?
68. What is an astable multivibrator?
69. What is a bistable multivibrator?
70. What is the op Amp based Mono stable multivibrator out put signal pulse width?
71. What is the op Amp based Astable multivibrator out put signal time period and frequency?
72. What are the requirements for producing sustained oscillations in feedback circuits? For sustained oscillations,
73. What are the different oscillators?
74. List the broad classification of ADCs.
75. List out the direct type ADCs.
76. List out some integrating type converters.
77. What is integrating type converter
78. Explain in brief the principle of operation of successive Approximation ADC.
79. What are the main advantages of integrating type ADCs?

80. Where are the successive approximation type ADC's used?
81. What is the main drawback of a dual slope ADC?
82. State the advantages of dual slope ADC.
83. Define conversion time.
84. Define resolution of a data converter.
85. Define Register. Explain the different types of Registers.
86. Define Flip-Flop. What is Master Slave JK Flip-Flop.
87. What is Ring and Johnson Counter.
88. Define Multivibrator.
89. Define Filter. What is meant by second order Filter.
90. Define Half Adder and Full Adder.
91. Define Half subtractor & Full subtractor.

13.0 University Result

Examination	Total Students	S+	S	A	B	C	D	E	F	% Passing
← New Scheme →										

Prepared by	Checked by		
Prof. S.S.Malaj	Prof. D. M. Kumbhar	HOD Electronics & Commn. Engg. Dept. HSIT NIDASOSHI	Principal

Subject Title	**Sensors and Instrumentation**		
Subject Code	**BEC306B**	**IA Marks IA 25 +Assignments / GD/Quiz/Seminar25**	50(100)
Number of Lecture Hrs/Week /	03	**Exam Marks (appearing for)**	50 (100)
Total Number of Lecture Hrs	40	**Exam Hours**	03
CREDITS – 03			

FACULTY DETAILS:		
Name: Prof. D M Kumbhar	**Designation:** Assistant Professor	**Experience :Teach- 16** years (Ind 07years)
No. of times course taught: 01	**Specialization:**Digital Electronics	

1.0 Prerequisite Subjects:

Sl. No	**Branch**	**Semester**	**Subject**
01	Students should have the knowledge of basic subjects	I, II	Basic electrical &electronics

2.0 Course Objectives

This course will enable students to

- Understand various technologies associated in manufacturing of sensors
- Acquire knowledge about types of sensors used in modern digital systems
- Get acquainted about material properties required to make sensors
- Understand types of instrument errors and circuits for multirange Ammeters and Voltmeters.
- Describe principle of operation of digital measuring instruments and Bridges.
- Understand the operations of transducers and instrumentation amplifiers.

3.0 Course Outcome

Having successfully completed this course, the student will be able to

	Course Outcome	**Cognitive Level**	**PO's**
206B.1	Understand the material properties required to make sensors.	U	1,2,3,4,5,6, 7,8,9,
206B.2	Describe the manufacturing process of sensors	U	1,2,3,4,5,6, 7,8,9,
206B.3	Analyze the instrument characteristics and errors.	U	1,2,3,4,5,6, 7,8,9,
206B.4	Describe the principle of operation and develop circuits for multirange Ammeters, Voltmeters and Bridges to measure passive component values and frequency.	U	1,2,3,4,5,6, 7,8,9, 10,11,12
206B.5	Understand the principle of transducers for measuring physical parameters.	U	1,2,3,4,5,6, 7,8,9,

4.0 Course Content

Modules	Teaching Hours	Bloom's Taxonomy (RBT) level
Module 1		
General concepts and terminology, sensor classification, Primary Sensors, material for sensors, microsensor technology.	**08**	**L1, L2,L3**
Module -2		
Self-generating Sensors-Thermoelectric sensors, piezoelectric sensors, pyroelectric sensors, photovoltaic sensors, electrochemical sensors.	**08**	**L1, L2,L3**
Module-3		
Principles of Measurement: Static Characteristics, Error in Measurement, Types of Static Error. Multirange Ammeters, Multirange voltmeter. **Digital Voltmeter:**Ramp Technique, Dual slope integrating Type DVM, Direct Compensation type and Successive Approximations type	**08**	**L1, L2,L3**
Module-4		
Digital Multimeter: Digital Frequency Meter and Digital Measurement of Time, Function Generator. **Bridges:** Measurement of resistance: Wheatstone's Bridge, AC Bridges - Capacitance and Inductance Comparison bridge, Wien's bridge.	**08**	**L1, L2,L3**
Module-5		
Transducers: Introduction,Electrical Transducer,Resistive Transducer,Resistive position Transducer, Resistance Wire Strain Gauges, Resistance Thermometer, Thermistor, LVDT. Instrumentation Amplifier using Transducer Bridge, Temperature indicators using Thermometer, Analog Weight Scale	**08**	**L1, L2, L3**

5.0 Relevance to future subjects

Sl. No	Semester	Subject	Topics
01	VIII	Project work	Sensors , signal conditioning
02	VI	Mini Project	Sensors , signal conditioning

6.0 Relevance to Real World

SL.No	Real World Mapping
01	Design of signal conditioning circuits for different applications.
02	Hobby/Mini projects
03	Home appliances/ controlling of equipment's.

7.0 Gap Analysis and Mitigation

Sl. No	Delivery Type	Details
01	Tutorial	Topic: Simulation software like Simulink, PSpice and Proteus.
02	NPTEL	Basics&Application

8.0 Books Used and Recommended to Students

Text Books
1. Sensors and Signal Conditioning", Ramon Pallas Areny, JohnG. Webster,2ndedition, John Wiley and Sons,2000 2. H.S.Kalsi, "Electronic Instrumentation", Mc Graw Hill,3rdEdition,2012,ISBN:9780070702066
Reference Books
1. DavidA. Bell,"Electronic Instrumentation & Measurements", Oxford University Press PHI 2ndEdition, 2006,ISBN 81-203-2360-2. 2. D. HelfrickandW.D. Cooper, "Modern Electronic Instrumentation and Measuring Techniques", Pearson, 1stEdition, 2015, ISBN: 9789332556065.

9.0 Relevant Websites (Reputed Universities and Others) for Notes/Animation/Videos Recommended

Website and Internet Contents References
12) https://nptel.co.in 13) http://m.noteboy.in/vtuflies/machine%20drawing.pdf

10.0 Magazines/Journals Used and Recommended to Students

Sl.No	Magazines/Journals	website
1	IEEE Xplorer	http://ieee.com
2	International Journal of Science and Technology	http://www.sciencedirect.com/science/journal/00207683
3	Journal of Communication Engineering	http://ieee.com

11.0 Examination Note

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)

- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks

12.0 Course Delivery Plan

Module No.	Lecture No.	Content of Lecture	Teaching Method	% Of Portion
1	1	General concepts and terminology	Chalk and talk, PPT	20
	2	Sensor classification	Chalk and talk, PPT	
	3	Primary Sensors	Chalk and talk, PPT	
	4	Primary Sensors	Chalk and talk, PPT	
	5	Material for sensors	Chalk and talk, PPT	
	6	Material for sensors	Chalk and talk, PPT	
	7	Microsensor technology	Chalk and talk, PPT	
	8	Microsensor technology	Chalk and talk, PPT	
2	9	**Self-generating** Sensors-	Chalk and talk, PPT	20
	10	Thermoelectric sensors	Chalk and talk, PPT	
	11	Piezoelectric sensors	Chalk and talk, PPT	
	12	Pyroelectric sensors	Chalk and talk, PPT	
	13	Photovoltaic sensors	Chalk and talk, PPT	
	14	Photovoltaic sensors	Chalk and talk, PPT	
	15	Electrochemical sensors	Chalk and talk, PPT	
	16	Electrochemical sensors	Chalk and talk, PPT	
3	17	**Principles of Measurement:**Static Characteristics, Error in Measurement,.	Chalk and talk, PPT	20
	18	Types of Static Error	Chalk and talk, PPT	
	19	Multirange Ammeters	Chalk and talk, PPT	
	20	Multirange voltmeter	Chalk and talk, PPT	
	21	**Digital Voltmeter:**Ramp Technique	Chalk and talk, PPT	
	22	Dual slope integrating Type DVM	Chalk and talk, PPT	
	23	Direct Compensation type	Chalk and talk, PPT	
	24	Successive Approximations type	Chalk and talk, PPT	

4	25	**Digital Multimeter:** Digital Frequency Meter and,. **Bridges:**	Chalk and talk, PPT	20
	26	Digital Measurement of Time	Chalk and talk, PPT	
	27	Function Generator	Chalk and talk, PPT	
	28	Measurement of resistance: Wheatstone's Bridge	Chalk and talk, PPT	
	29	Wheatstone's Bridge	Chalk and talk, PPT	
	30	Capacitance Comparison bridge	Chalk and talk, PPT	
	31	Inductance Comparison bridge	Chalk and talk, PPT	
	32	Wien's bridge	Chalk and talk, PPT	
5	33	**Transducers:** Introduction,Electrical Transducer	Chalk and talk, PPT	20
	34	Resistive Transducer,Resistive position Transducer	Chalk and talk, PPT	
	35	Resistance Wire Strain Gauges	Chalk and talk, PPT	
	36	Resistance Thermometer	Chalk and talk, PPT	
	37	Thermistor, LVDT	Chalk and talk, PPT	
	38	Instrumentation Amplifier using Transducer Bridge	Chalk and talk, PPT	
	39	Temperature indicators using Thermometer	Chalk and talk, PPT	
	40	Analog Weight Scale	Chalk and talk, PPT	

13.0 Assignments, Pop Quiz, Mini Project, Seminars

Sl.No.	Title	Outcome expected	Allied study	Week No.	Individual / Group activity	Reference: book/website /Paper
1	Assignment 1: University Questions on random process and Amplitude modulation	Students study the Topics and will prepare for Final Exam.	Module-1,2,3 of the syllabus	7	Individual Activity	Book 1, 2 of the reference list. Website of the Reference list
2	Assignment 2: University Questions on module Angle Modulation and Noise in communication system	Students study the Topics and will prepare for Final Exam.	Module-4,5 of the syllabus	14	Individual Activity.	Book 1, 2 of the reference list. Website of the Reference list

14.0 University Result

NEW SCHME

Prepared by	Checked by		
Prof. D. M. Kumbhar	Prof. D. B. Madihalli	HOD Electronics & Commn. Engg. Dept. HSIT NIDASOSHI	Principal

Subject Title	**MATLAB Programming**		
Subject Code	BEC358B	**IA Marks +Assignments + Quiz/Seminar out of 100 scale down to 50 Marks**	50
Number of Lecture Hrs/Week /	01(L)	**Exam Marks (appearing for)**	50
Total Number of Lecture Hrs	14 Theory	**Exam Hours**	01
CREDITS – 01			

FACULTY DETAILS:		
Name: Dr. S. S. Ittannavar	**Designation:** Associate Professor	**Experience:**11 years
No. of times course taught: 01	**Specialization:** Digital Signal Processing	

1.0 Prerequisite Subjects:

Sl. No	Branch	Semester	Subject
01	Students should have the knowledge of basic subjects	1 & 2	C Programming

2.0 Course Objectives

This course will enable students to:

- Understand the MATLAB commands and functions.
- Create and Execute the script and function files
- Work with built in function, saving and loading data and create plots.
- Work with the arrays, matrices, symbolic computations, files and directories.
- Learn MATLAB programming with script, functions and language specific features..

3.0 Course Outcomes

Having successfully completed this course, the student will be able to

	Course Outcome	Cognitive Level	PO's
CO1	Understand the syntax of MATLAB for arithmetic computations, arrays, matrices. for the given specifications	U	1,2,3,4,6,7,9,10 ,11,12
CO2	Understand the built in function, saving and loading data, and create plots	U	1,2,3,4,5,6,7,9, 10,11,12
CO3	Create program using symbolic computations, Importing and exporting data and files	U	1,2,3,4,5,6,7,9, 10,11,12
CO4	Create program using character strings, Command line functions and Built-in functions.	U	1,2,3,4,5,6,7,9, 10,11,12
Total Hours of instruction		**40**	

4.0 Course Content

Modules	Teaching Hours	Bloom's Taxonomy (RBT) level
Module 1		
Introduction: Basics of MATLAB, Simple arithmetic calculations, Creating and working with arrays and numbers.	**02**	**L1, L2**
Module -2		
Creating and printing simple plots, Creating, saving and executing a script file, Creating and executing a function file, Working with arrays and matrices.	**03**	**L1, L2,L3**
Module-3		
Working with anonymous functions, Symbolic Computations, Importing and exporting data, Working with files and directories.	**03**	**L1, L2,L3**
Module-4		
Interactive computations: Matrices and vectors, Matrix and array operations, Character strings, Command line functions, Built-in functions, Saving and loading data, Plotting simple plots.	**03**	**L1, L2,L3**
Module-5		
Programming in MATLAB: Script Files, Function Files, Language specific Features.	**03**	**L1, L2, L3**

5.0 Relevance to future subjects

Sl. No	Semester	Subject	Topics
01	VIII	Project work	Design using MATLAB
02	IV	DSP	Signal Processing Operations

6.0 Relevance to Real World

SL.No	Real World Mapping
01	MATLAB is software tool that is digital tool that we can develop any signal processing operations.

7.0 Gap Analysis and Mitigation

Sl. No	Delivery Type	Details
01	Tutorial	Topic: MATLAB Programming,
02	NPTEL	MATLAB Programming,

8.0 Books Used and Recommended to Students

Text Books
1. Rudra Pratap, Getting Started with MATLAB – A quick Introduction for scientists and Engineers, Oxford University Press, 2010.

9.0 Relevant Websites (Reputed Universities and Others) for Notes/Animation/Videos Recommended

Website and Internet Contents References
14) https://in.mathworks.com/products/matlab/programming-with-matlab.html?requestedDomain=
15) https://in.mathworks.com/help/matlab/programming-and-data-types.html
16) https://www.tutorialspoint.com/matlab/index.htm

10.0 Magazines/Journals Used and Recommended to Students

Sl.No	Magazines/Journals	website
1	IEEE Transactions on Communication systems	ieeexplore.ieee.org/xpl/RecentIssue.jsp?punumber=4547466
2	Digital Communications and Networks - Journal - Elsevier	www.journals.elsevier.com/digital-communications-and-networks/
3	International Journal of Digital Communication and Networks	ijdcn.co.in
4	Journal of Communication - Wiley Online Library	onlinelibrary.wiley.com

11.0 Examination Note

Assessment Details (both CIE and SEE)

The weight age of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together

Continuous internal Examination (CIE)

- For the Assignment component of the CIE, there are 25 marks and for the Internal Assessment Test component, there are 25 marks.
- The first test will be administered after 40-50% of the syllabus has been covered, and the second test will be administered after 85-90% of the syllabus has been covered
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned.
- For the course, CIE marks will be based on a scaled-down sum of two tests and other methods of assessment.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examinations (SEE)

SEE paper shall be set for 50 questions, each of the 01 marks. The pattern of the question paper is MCQ (multiple choice questions). The time allotted for SEE is **01 hour.** The student has to secure a minimum of 35% of the maximum marks meant for SEE.

OR

MCQ (Multiple Choice Questions) are preferred for 01 credit courses, however, if course content demands the general question paper pattern that followed for 03 credit course, then

1. The question paper will have ten questions. Each question is set for 10 marks.
2. There will be 2 questions from each module. Each of the two questions under a module may or may not have the sub-questions (with maximum sub-questions of 02, with marks distributions 5+5, 4+6, 3+7).
3. The students have to answer 5 full questions, selecting one full question from each module.
4. The duration of the examinations shall be defined by the concerned board of studies

12.0 Course Delivery Plan

Module No.	Lecture No.	Content of Lecture	Teaching Method	% of Portion
1.	1	**Introduction:** Basics of MATLAB, Simple arithmetic calculations,	Chalk and talk	20
	2	Creating and working with arrays and numbers.	Chalk and talk	
2.	3	Creating and printing simple plots,	Chalk and talk	20
	4	Creating, saving and executing a script file,	Chalk and talk	
	5	Creating and executing a function file, Working with arrays and matrices.	Chalk and talk	
3.	6	Working with anonymous functions,	Chalk and talk	20
	7	Symbolic Computations,	Chalk and talk	
	8	Importing and exporting data, Working with files and directories.	Chalk and talk	
4.	9	**Interactive computations:** Matrices and vectors,	Chalk and talk	20
	10	Matrix and array operations, Character strings, Command line functions,	Chalk and talk	
	11	Built-in functions, Saving and loading data, Plotting simple plots.	Chalk and talk	
5.	12	**Programming in MATLAB:** Script Files,	Chalk and talk	20
	13	Function Files,.	Chalk and talk	
	14	Language specific Features	Chalk and talk	

13.0 Assignments, Pop Quiz, Mini Project, Seminars

Sl.No.	Title	Outcome expected	Allied study	Week No.	Individual / Group activity	Reference: book/website /Paper
1	Assignment 1: University Questions on Introduction and creating different arrays and matrices	Students study the Topics and will prepare for Final Exam.	Module-1, 2 of the syllabus	9	Individual Activity	Text Book 1
2	Assignment 2: University Questions on symbolic computations, Interactive computations and Programming in MATLAB	Students study the Topics and will prepare for Final Exam.	Module-3,4 & 5 of the syllabus	12	Individual Activity.	Text Book 1

14.0 University Result

Examination	S+	S	A	B	C	D	E	F	% of passing
First Time Introduced	-	-	-	-	-	-	-	-	-

Prepared by	Checked by	HOD	Principal
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