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First/Second Semester B.E. Degree Examination, June 2012

Basic Electronics

Time: 3 hrs.

Max. Marks:100

Note: 1. Answer any FIVE full questions, choosing at least two from each part.**2. Answer all objective type questions only on OMR sheet page 5 of the answer booklet.****3. Answer to objective type questions on sheets other than OMR will not be valued.**

PART – A

- 1 a. Choose your answers for the following : (04 Marks)**
- Zener diode can be used for rectification. This statement is _____.
 A) True B) False
 C) Neither True Nor False D) None of these
 - PIV in case of half wave rectifier for an input signal of $V_m \sin \omega t$ is _____.
 A) V_m B) $2V_m$
 C) $\frac{V_m}{2}$ D) $\frac{V_m}{\sqrt{2}}$
 - If frequency of input is 60 Hz for a fullwave rectifier, the frequency of ripple is _____.
 A) 30 Hz B) 60 Hz
 C) 120 Hz D) 180 Hz
 - If peak to peak voltage is 4 V then RMS voltage is _____.
 A) $\sqrt{2}$ Volts B) 2 Volts
 C) 2.82 Volts D) Both (A) and (C).
- b. Calculate the reverse saturation current for silicon diode which passes a current of 10 mA at 27°C, for a forward bias of 700 mV. (04 Marks)**
- c. Explain the effect of temperature on the diode characteristics and also on the power rating of the diode. (06 Marks)**
- d. Explain the operation of full wave center tap rectifier with neat circuit diagram and waveforms. (06 Marks)**
- 2 a. Choose your answers for the following : (04 Marks)**
- Bipolar junction transistor is _____ controlled device.
 A) Voltage B) Current
 C) Power D) Temperature
 - Operating point must be _____ for proper functioning of transistor.
 A) Increasing B) Decreasing
 C) Stable D) High
 - The DC load line of a transistor is a _____.
 A) Curved line B) '-ve' slope line
 C) '+' slope line D) Zero slope line
 - In a transistor α and β are related by _____.
 A) $\alpha = \frac{1}{1-\beta}$ B) $\alpha = \frac{\beta}{1+\beta}$
 C) $\beta = \frac{\alpha}{1+\alpha}$ D) $\frac{1}{1-\alpha}$
- b. Explain the characteristics of common base transistor configuration with neat circuit diagram. (08 Marks)**

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
 2. Any revealing of identification, appeal to evaluator and /or equations written eg. 42+8 = 50, will be treated as malpractice.

- 2 c. What is a d.c. load line? Explain with a fixed bias circuit diagram. (04 Marks)
- d. For the fixed bias circuit shown in Fig. Q2 (d), $V_{BE} = 0.7 \text{ V}$, $\beta = 60$, find
- Quiescent values of base and collector currents.
 - Quiescent value of V_{CE} .
 - Base-ground and collector-ground voltages.
 - Base-collector voltage.

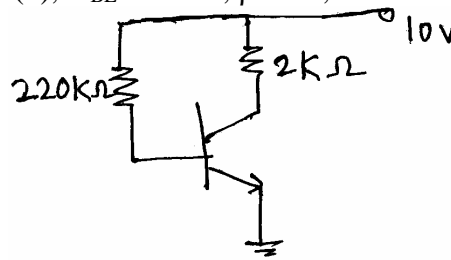


Fig. Q2 (d)

(04 Marks)

- 3 a. Choose your answers for the following : (04 Marks)
- In voltage divider bias circuit R_E is used for
 - Stabilization
 - As a load
 - As a bypass element
 - All of these
 - For exact analysis of voltage divider bias circuit _____ theorem is used.
 - Nortons
 - Thevenins
 - Superposition
 - Any one of these
 - _____ is the linear region of transistor characteristics.
 - Saturation
 - Cutoff
 - Active
 - Both (A) and (C)
 - Stability factor of fixed bias circuit is,
 - β
 - $\beta - 1$
 - $1 + \beta$
 - None of these
- b. List the factors which affect the stability of operating point. (04 Marks)
- c. With a neat circuit diagram, explain voltage divider biasing circuit and derive the expressions for V_{CE} and I_C using exact analysis. (08 Marks)
- d. For the circuit shown in Fig. Q3 (d), using silicon transistor with $V_{BE} = 0.7 \text{ V}$ and $\beta = 80$, find V_{CE} and V_B . (04 Marks)

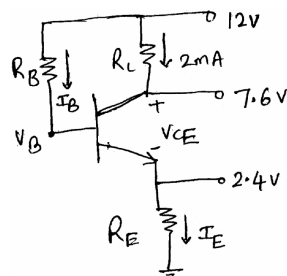


Fig. Q3 (d)

- 4 a. Choose your answers for the following : (04 Marks)
- The device which has wide application in pulse generator is _____
 - FET
 - BJT
 - Diode
 - UJT
 - FET is _____ controlled device.
 - Current
 - Voltage
 - Power
 - Temperature
 - The device which is known as Thyristor is _____
 - Diode
 - FET
 - Transistor
 - SCR
 - In FET the gate source junction is _____
 - Forward biased
 - Reverse biased
 - Unbiased
 - None of these

- 4 b. Explain the working of FET with neat circuit diagram and relevant characteristics. Indicate each region of the characteristics. (08 Marks)
- c. Explain the working of UJT with neat circuit diagram. Indicate all regions in the characteristics. (08 Marks)

PART – B

- 5 a. Choose your answers for the following : (04 Marks)
- The coupling capacitors in RC coupled amplifier affect _____ frequency response.
A) Low B) High
C) Very high D) Above 100 kHz.
 - The frequency at which oscillator will operate is the frequency for which the phase shift of the loop gain is _____.
A) 0° B) 360°
C) 180° D) Both (A) and (B).
 - In an oscillator the phase shift produced by amplifier is _____.
A) 0° B) 180°
C) 90° D) 270°
 - The oscillator used to generate oscillations in audio frequency range is _____.
A) LC oscillator B) RC oscillator
C) Crystal oscillator D) Both (B) and (C)
- b. Explain the working of RC phase shift oscillator with neat circuit diagram and waveforms at each stage. (08 Marks)
- c. List the effects of negative feedback. (04 Marks)
- d. In a transistor Hartley oscillator, $L_1 = 10 \mu\text{H}$, $L_2 = 10 \mu\text{H}$. Find the value of C required for an oscillating frequency of 150 kHz. Take $M = 0$. (04 Marks)
- 6 a. Choose your answers for the following : (04 Marks)
- An op-amp has _____ o/p impedance.
A) ∞ B) 0
C) 10000Ω D) 600Ω
 - Voltage follower has _____ gain.
A) High B) Low
C) Unity D) None of these
 - An op-amp non-inverting amplifier has $R_1 = 1 \text{ k}\Omega$ and $R_f = 3 \text{ k}\Omega$ when $V_i = -2 \text{ V}$, the output is _____.
A) -4 V B) 4 V
C) 8 V D) -8 V
 - Op-amp configuration used as buffer is _____.
A) Inverting amplifier B) Non inverting amplifier
C) Voltage follower D) Adder
- b. List the characteristics of ideal op-amp and practical op-amp. (08 Marks)
- c. The input to the op-amp shown in Fig. Q6 (c), at the non inverting terminal is $10\sin 10t$ Volts. Draw the output waveform indicating time period and maximum value. (04 Marks)
- d. Find the output of the op-amp circuit shown in Fig. Q6 (d). (04 Marks)

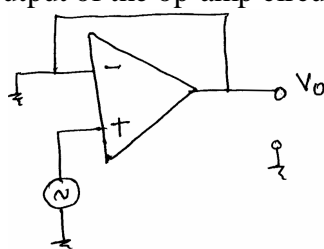


Fig. Q6 (c)

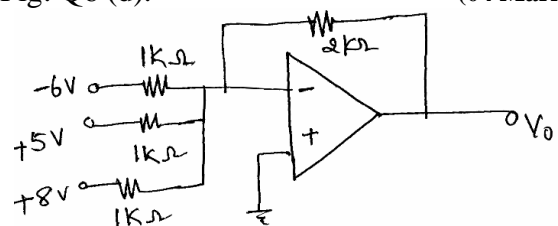


Fig. Q6 (d)

- 7 a. Choose your answers for the following : (04 Marks)
- $(100)_{10} = (?)_{16}$
 A) 64 B) 144
 C) 46 D) 80
 - 75 in binary contains _____ number of 1's.
 A) 8 B) 4
 C) 6 D) 3
 - $(16)_8 = (?)_{10}$
 A) 18 B) 20
 C) 14 D) 25
 - $(ABC)_{16} = (?)_{10}$
 A) 3000 B) 4230
 C) 2748 D) 2250
- b. Perform the following:
- $(101110)_2 = (?)_8$
 - $(110011)_2 - (11001)_2 = (?)_2$ using 2's complement method.
 - $(E10A2)_{16} - (5FF1)_{16} = (?)_{16}$ using 15's complement method.
 - $(77721)_8 - (66432)_8 = (?)_8$ using 7's complement method.
 - $(2384)_{16} = (?)_8$. (05 Marks)
- c. Explain the need for modulation. (05 Marks)
- d. Explain the working of super heterodyne receiver with neat circuit diagram and waveforms at each stage. (06 Marks)
- 8 a. Choose your answers for the following : (04 Marks)
- The EX-OR gate in which one input is connected to V_{CC} , operates as _____ gate.
 A) AND B) OR
 C) NOR D) NOT
 - The gate whose output is zero only when both the inputs are high is _____ gate.
 A) NAND B) NOR
 C) OR D) AND
 - $A + \overline{A}B + A$ is _____
 A) A B) B
 C) $A + \overline{B}$ D) $A + B$
 - Universal gates are,
 A) NAND and NOR B) AND and NAND
 C) OR and NOR D) NOR and EX-OR
- b. What is half adder and implement it using universal gates? (06 Marks)
- c. Simplify and realize the Boolean expressions, using two i/p NAND gates only.
- $ABCD + \overline{A}\overline{B}\overline{C}\overline{D}$
 - $AB + ABC + AB\overline{C} + \overline{A}BC$
 - $ABCD + \overline{A}\overline{B}\overline{C}\overline{D} + ABD$ (10 Marks)

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