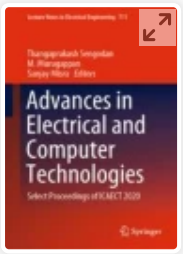

International Conference on Advances in Electrical and Computer Technologies

ICAECT 2020: **Advances in Electrical and Computer Technologies** pp 613–626

Design and Implementation of 3-bit Flash Analog to Digital Converter for Low Power and High Speed Applications with New Ex-OR Based ROM Encoder

S. S. Kamate & H. P. Rajani

Conference paper | First Online: 27 February 2021

Part of the Lecture Notes in Electrical Engineering book series (LNEE,volume 711)

Abstract

This paper presents design of 3-bit power-efficient Flash Analog to Digital Converter for high-speed applications with single inverter comparator and Ex-OR based ROM encoder circuits. The Single Inverter Comparator circuit compares applied input voltage with the reference voltage and results in ‘0’ or ‘1’ output depending upon their magnitudes. The

designed single inverter comparator consumes just 2.94pW amount of power. Outputs of these comparators form thermometer code which has to be applied to an encoder to obtain the digital code. A high speed Ex-OR based ROM encoder is designed to convert comparator outputs to the corresponding digital equivalents. A 3-bit Flash ADC is designed and simulated using Cadence analog design tools with 180 nm process technological library. The simulated results of the design show an average power consumption of 8.157uW and delay of 2.832 ns at 10 MHz. The area occupied by the design is 205.536um^2.

Keywords

TIQ comparator **LTE comparator**

Single inverter comparator

EX-OR based ROM encoder

Low power flash ADC

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About this paper

Cite this paper

Kamate, S.S., Rajani, H.P. (2021). Design and Implementation of 3-bit Flash Analog to Digital Converter for Low Power and High Speed Applications with New Ex-OR Based ROM Encoder. In: Sengodan, T., Murugappan, M., Misra, S. (eds) Advances in Electrical and Computer Technologies. ICAECT 2020. Lecture Notes in Electrical

Engineering, vol 711. Springer, Singapore.
https://doi.org/10.1007/978-981-15-9019-1_53

.RIS .ENW .BIB

DOI	Published	Publisher Name
https://doi.org/10.1007/978-981-15-9019-1_53	27 February 2021	Springer, Singapore

Print ISBN	Online ISBN	eBook Packages
978-981-15-9018-4	978-981-15-9019-1	Computer Science Computer Science (R0)

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