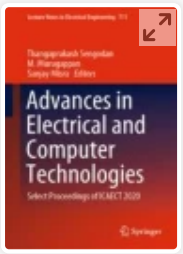

International Conference on Advances in Electrical and Computer Technologies

ICAECT 2020: **Advances in Electrical and Computer Technologies** pp 613–626

Design and Implementation of 3-bit Flash Analog to Digital Converter for Low Power and High Speed Applications with New Ex-OR Based ROM Encoder

S. S. Kamate & H. P. Rajani

Conference paper | First Online: 27 February 2021

Part of the Lecture Notes in Electrical Engineering book series (LNEE,volume 711)

Abstract

This paper presents design of 3-bit power-efficient Flash Analog to Digital Converter for high-speed applications with single inverter comparator and Ex-OR based ROM encoder circuits. The Single Inverter Comparator circuit compares applied input voltage with the reference voltage and results in ‘0’ or ‘1’ output depending upon their magnitudes. The

designed single inverter comparator consumes just 2.94pW amount of power. Outputs of these comparators form thermometer code which has to be applied to an encoder to obtain the digital code. A high speed Ex-OR based ROM encoder is designed to convert comparator outputs to the corresponding digital equivalents. A 3-bit Flash ADC is designed and simulated using Cadence analog design tools with 180 nm process technological library. The simulated results of the design show an average power consumption of 8.157uW and delay of 2.832 ns at 10 MHz. The area occupied by the design is 205.536um^2.

Keywords

TIQ comparator **LTE comparator**

Single inverter comparator

EX-OR based ROM encoder

Low power flash ADC

Buy Chapter

eBook EUR 245.03

Price includes VAT (India)

- Available as EPUB and PDF
- Read on any device
- Instant download
- Own it forever

Buy eBook

Softcover Book EUR 299.99

Price excludes VAT (India)

- Compact, lightweight edition
- Dispatched in 3 to 5 business days
- Free shipping worldwide - see info

Buy Softcover Book

Hardcover Book EUR 299.99

Price excludes VAT (India)

- Durable hardcover edition
- Dispatched in 3 to 5 business days
- Free shipping worldwide - see info

Buy Hardcover Book

Tax calculation will be finalised at checkout

Purchases are for personal use only

Learn about institutional subscriptions

References

1. S.S. Kamate, A. Naikar, S.S. Malaj, Design and implementation of low power flash ADC using cadence tool. J. Adv. Sci. Technol. **12**(25), (2016)

2. J. Yoo, K. Choi, D. Lee, Comparator generation and selection for highly linear CMOS flash analog-to-digital converter. Analog Integr. Circuits Signal Process. **35**,179–187 (2003). https://doi.org/10.1023/A:1024134700921

3. M. Kulkarni, V. Sridhar, G. H. Kulkarni, 4-bit Flash analog to digital converter design using CMOS-LTE comparator. in *2010 IEEE Asia Pacific Conference on Circuits and Systems*, Kuala Lumpur, (2010), pp. 772–775. https://doi.org/10.1109/APCCAS.2010.5774817.

4. I. Perumal, J. Perumal, V. Yuvaraj, Design of analog to digital converter using CMOS logic. in *2009 International Conference on in Advances in Recent Technologies Communication and Computing, Kottayam, Kerala*(2009), pp. 74–76. https://doi.org/10.1109/ARTCom.2009.84

5. A. Kar, A. Majumder, A. J. Mondal, N. Mishra, Design of ultra low power flash ADC using TMCC & bit referenced encoder in 180nm technology. in *2015 International Conference on VLSI Systems, Architecture, Technology and Applications (VLSI-SATA)*, Bangalore (2015), pp.

1–6. https://doi.org/10.1109/VLSI-SATA.2015.7050458

6. K. N. Hosur et al., Design of 4 bit flash ADC using TMCC & NOR ROM encoder in 90nm CMOS technology. *in 2015 International Conference on Trends in Automation, Communications and Computing Technology (I-TACT-15)*, Bangalore (2015), pp. 1–6

7. Y. Gupta, L. Garg, S. Khandelwal, S. Gupta, S. Jain, S. Saini, A 4-bit, 3.2 GSPS flash analog to digital converter with a new multiplexer based encoder. in *2014 11th International Conference on Electrical Engineering/Electronics, Computer, Telecommunications and Information Technology (ECTI-CON)*, Nakhon Ratchasima (2014), pp. 1–6. https://doi.org/10.1109/ECTICon.2014.6839721

8. N. Kalyani, M. Monica, Design and analysis of high speed and low power 6-bit flash ADC. in *2018 2nd International Conference on Inventive Systems and Control (ICISC)*, Coimbatore (2018), pp. 742–747. https://doi.org/10.1109/ICISC.2018.8398897.

9. D.O. Budanov, M.M. Pilipko, D.V. Morozov, Encoders for flash analog-to-digital converters. in *2018 IEEE Conference of Russian Young Researchers in Electrical and Electronic*

Engineering (EIConRus), Moscow (2018), pp. 173–177.https://doi.org/10.1109/EIConRus.2018.8317058

Author information

Authors and Affiliations

Hirasugar Institute of Technology, Nidasoshi, Karnataka, India

S. S. Kamate

K. L. E's Dr. M.S.S College of Engineering and Technology, Belagavi, Karnataka, India

H. P. Rajani

Corresponding author

Correspondence to S. S. Kamate .

Editor information

Editors and Affiliations

Department of Electrical and Electronics Engineering, SVS College of Engineering, Coimbatore, Tamil Nadu, India

Thangaprakash Sengodan

Department of Electronic and Communication Engineering, Kuwait College of Science and Technology, Doha, Kuwait

M. Murugappan

Department of Computer and Information Sciences, Covenant University, Ota, Nigeria

Sanjay Misra

Rights and permissions

Reprints and permissions

Copyright information

About this paper

Cite this paper

Kamate, S.S., Rajani, H.P. (2021). Design and Implementation of 3-bit Flash Analog to Digital Converter for Low Power and High Speed Applications with New Ex-OR Based ROM Encoder. In: Sengodan, T., Murugappan, M., Misra, S. (eds) Advances in Electrical and Computer Technologies. ICAECT 2020. Lecture Notes in Electrical Engineering, vol 711. Springer, Singapore. https://doi.org/10.1007/978-981-15-9019-1_53

.RIS .ENW .BIB

DOI	Published	Publisher Name
https://doi.org/10.1007/978-981-15-9019-1_53	27 February 2021	Springer, Singapore

Print ISBN	Online ISBN	eBook Packages
978-981-15-9018-4	978-981-15-9019-1	Computer Science Computer Science (R0)

Publish with us

Policies and ethics