Static and Dynamic power optimization using Leakage Feedback approach for nanoscale CMOS VLSI circuits

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Abstract:

Packaging density and operating speed are common considerable issues in today's deep submicron regime. If packaging density has to be increased then transistor size and channel length should be decreased. Due to short channel effects in submicron regime. Decreasing channel length decreases the threshold voltage. Decreasing threshold voltage also increases the power dissipation due the subthreshold leakage current. By carefully designing the sleep transistors with an added leakage current feedback transistor, effectively decreases the static and dynamic power dissipation along with delay introduced due to sleep transistors. The proposed technique is applied to design a logic circuit to efficiently reduce static, dynamic power dissipation with increase performance.

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I. Introduction

The main sources of power dissipation are static power dissipation and dynamic power dissipation. scaling down of the supply voltage proportionally decreases the threshold voltage it increases the subthreshold leakage current. Till today many leakage current minimisation techniques were tried but they only targeted to reduce the static power dissipation not the dynamic power dissipation and also has the adverse effect of decreasing the operating speed.in this paper firstly by carefully designing the extra sleep transistors which are introduced in MTCMOS structure to reduce static power dissipation and to increase the performance in terms of speed. Secondly dynamic power dissipation.it takes nearly half of the total power supply.By reducing power dissipation can be reduced by adiabatic switching and charge recycling logic. but drawbacks of these are it requires (1)more hardware, (2)pulse power supplies,(3)delay will be more,(4)high supply voltage, so these techniques are not suitable for scaling down of supply voltage to alleviate power dissipation.in this paper it addresses the issues of static power dissipation through MTCMOS and dynamic power dissipation through leakage current feedbacking and also the delay and ground bounce noise through proper sizing of sleep transistors. This technique achieves the best results to minimize power dissipation with high performance.

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Figures

References

Keywords

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