Design of Programmable FFT-IFFT Processor

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ABSTRACT
Orthogonal Frequency Division Multiplexing system is famous for its robustness against frequency selective fading channel. The Fast Fourier Transform/Inverse Fast Fourier Transform processors are used as the modulation/demodulation kernel in the OFDM systems. The sizes of FFT-IFFT processors are varied in the different applications of OFDM systems. We suggest a programmable FFT-IFFT processor to cover the different specifications of OFDM applications. The cached-memory architecture is our suggested VLSI system architecture. The chip can operate up to 80 MHz and meet most of the standard requirements.
Key Words: OFDM, FFT-IFFT Processor, VLSI.

I. INTRODUCTION

Fourth-Generation wireless and mobile systems are currently the focus of research and development. Broadband wireless systems based on Orthogonal Frequency Division Multiplexing (OFDM) will allow packet-based high-data-rate communication suitable for video transmission and mobile-Internet applications. The IEEE 802.11a standard defines the principle functions and architecture of such a high data rate communication system. Apart from the high speed of operation, the system demands low power consumption since it is primarily aimed at portable and mobile applications. We can show through simulation that the most computationally intensive parts of such a high-data-rate system are the 64-2048 point Inverse Fast Fourier Transform (IFFT) in the transmit direction. We describe a novel programmable 64-2048 point FFT/IFFT processor, a more detailed and complete description of the entire design is provided. The processor performs a forward 64-2048 point FFT in 40 to 49 clock cycles making it suitable for high-speed data communication systems.

In present day wireless technology, the OFDM is generally used, by adopting FFT processor for the wireless communication adds advantages like High Speed, Less Area requirement, Less Power Consumption and Minimal Interference with the other signals. The main motivation of this work is to derive and investigate an alternative architecture for FFT computation that satisfies the timing constraints with moderate silicon area and low power consumption. The main reason is that, if an FFT algorithm can satisfy the timing constraints, it is expected to be more power efficient.

II. LITERATURE SURVEY

1. Trio Adiono and RellaMareta. “Low latency parallel-pipelined configurable FFT/IFFT 128/256/512/1024/2048 for LTE”. In Intelligent and Advanced Systems (ICIAS), 2012 4th International Conference on, volume 2, pages 768–773. IEEE, 2012

Long Term Evolution (LTE) is one of the latest technologies in wireless communication field. It has features of higher data rates and low latency. LTE defines a number of channel bandwidths which causes FFT/IFFT in LTE must be configurable. In this paper, they present the efficient implementation of a parallel-pipelined configurable FFT/IFFT processor for Orthogonal Frequency Division Multiple Access (OFDMA) applications in LTE.

2. Chu yu, Mao-Hsu Yen “A Low power 64-point FFT/IFFT Processor for OFDM Applications” IEEE Transactions on Consumer Electronics, Vol. 57, Feb 2011.

In this paper, they present the efficient implementation of a pipeline FFT/IFFT processor for OFDM applications. Our design adopts a single-path delay feedback style as the proposed hardware architecture. To

eliminate the read-only memories (ROM's) used to store the twiddle factors, the proposed architecture applies a reconfigurable complex multiplier and bit-parallel multipliers to achieve a ROM-less FFT/IFFT processor, thus consuming lower power than the existing works. The design spends about 33.6K gates, and its power consumption is about 9.8mW at 20MHz.
This result shows that our design owns lower hardware cost and power consumption compared to the existing ones.

III. PROBLEM DEFINITION

- For various point DFT calculations different FFT programs have to be developed. We are looking forward to design a programmable FFT-IFFT processor which will choose the required point FFT as per the applications.
- Conventional methods of calculating DFT consumes more power which in turn dissipates in the form of heat, affecting the circuitry with respect to efficiency. Hence it is required to move to methods which would lead to less power consumption.
- Bandwidth is the maximum amount of data that can travel through a 'channel'. Throughput is how much data actually does travel through the 'channel' successfully. This can be limited by different things including pipeline architecture, reducing the latency.

IV. SYSTEM MODEL

The FFT processor is one of the most complex and intensive computation module of various communication systems. However, the main constraints nowadays for such processors are execution time and lower power consumption. One of the most essential arithmetic operations used in FFTs is complex multiplication. It is often the most expensive arithmetic operation and one of the dominate factors in determining the performance in terms of speed and power consumption.

It is observed that the complex multiplier may consume more than 70% of the power in an FFT processor. Therefore, an effective design of FFT processor is vital in low-power applications. The aim here is to reduce the multiplication complexity and develop architecture for use in OFDM based communication system.

One method proposed in this study to reduce the complexity is to replace the complex multiplication with less expensive real and constant multiplications. We applied this method to an efficient FFT 64-2048 point based on 4-point module.

V. BLOCK DIAGRAM

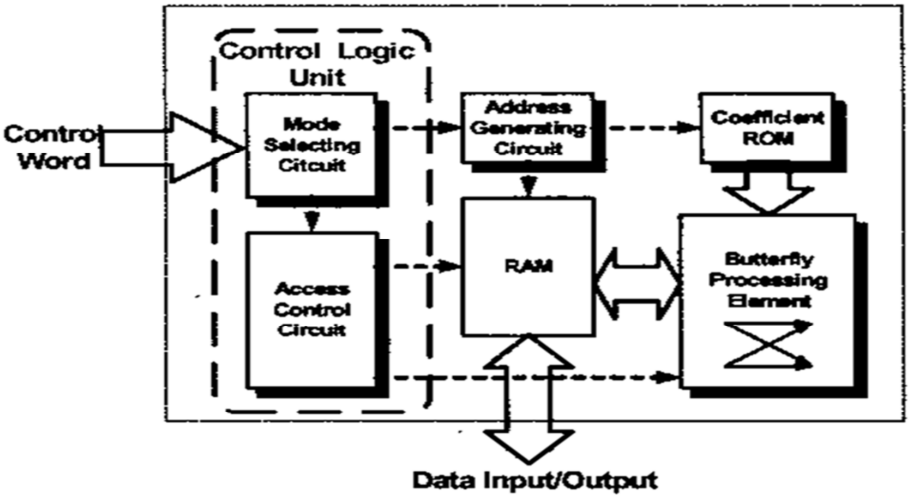

Figure 1.The proposed Programmable FFT/IFFFT Processor

VI. HARDWARE IMPLEMENTATION OF THE MODEL

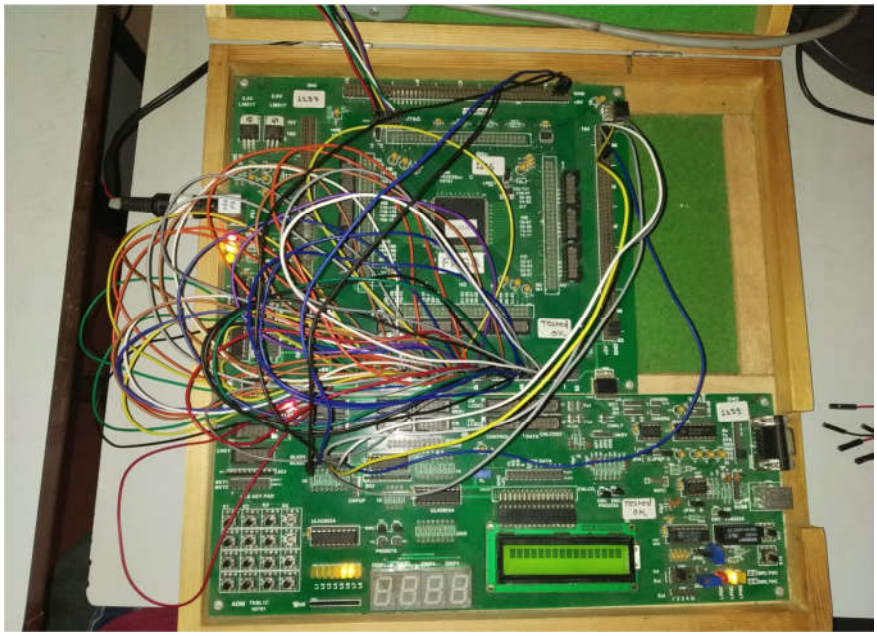

Figure 2. Hardware Connection

VII. RESULT ANALYSIS AND DISCUSSION

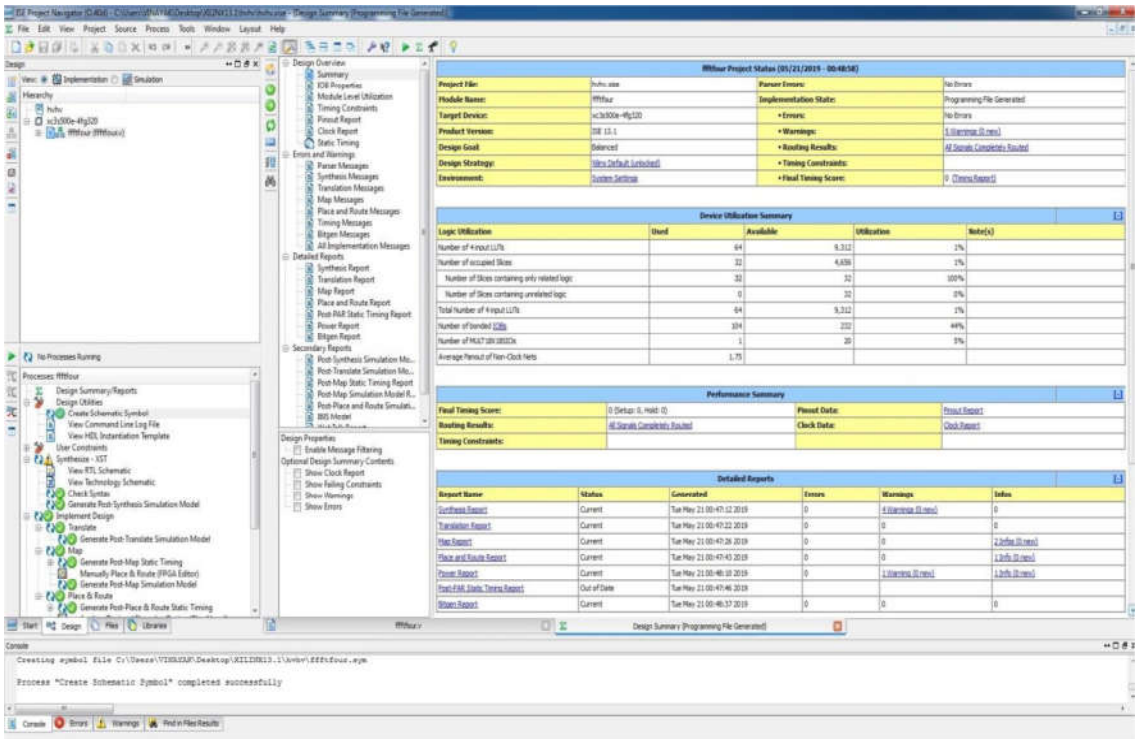

Figure 3. Design summary of 4 point FFT.

The following figure shows the Design Summary of 4-point FFT, where we can note that the number of logic slice registers usage is 100%.

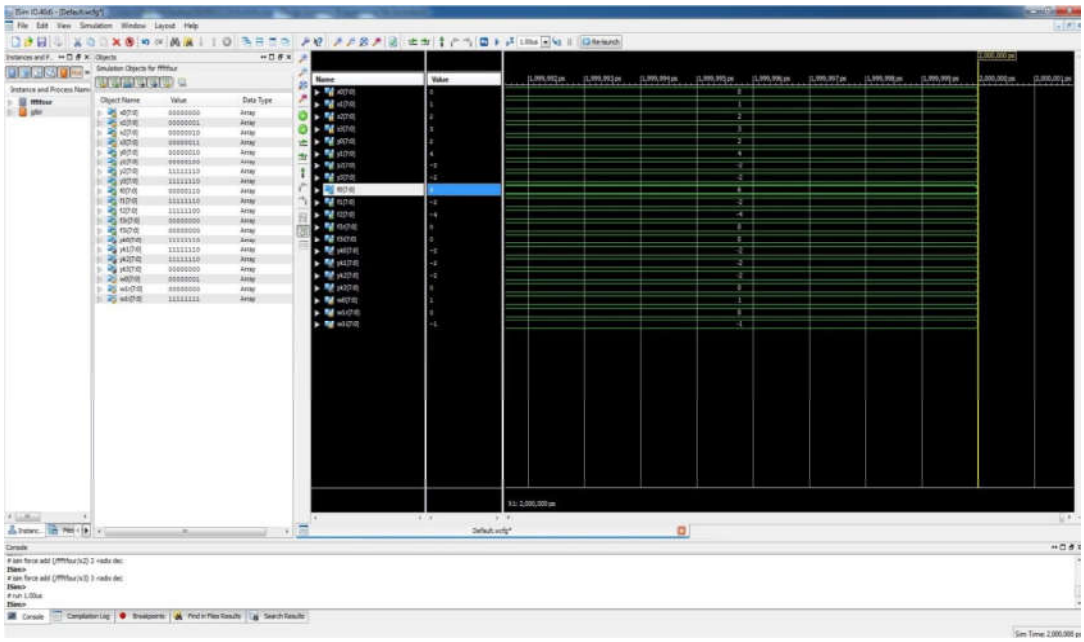

Figure 4. FFT simulation result

VIII.CONCLUSION

A novel 64-point and up to 2048-point FFT/IFFT architecture for high-speed wireless systems based on OFDM transmission has been presented. This architecture is based on a decomposition of the 64-point FFT in to two 32-point. It exhibits numerous attractive features from a VLSI point of view, which include regularity, modularity, simple wiring, and high throughput. A new low-power high-performance 64-point FFT/IFFT chip for wireless applications has been successfully designed based on the architecture described. The new design is deemed to result in a considerable reduction in cost, size, and power dissipation for the existing wireless systems.

We used 32- multipliers so that 32 multiplications are done at a single clock cycle, the operation becomes fast and we can get the output with lesser delay. And we used 128 add/subtract so that the area required for implementing the design.

The power, timing and area report are generated for FFT/IFFT processor using the Design Compiler (SYNOPSIS) tool and also an ASIC synthesis has been done for the complete system.

IX. FUTURE SCOPE

As it is discussed that the 2, 8-point FFT‟s combined to build the 16-point FFT in the same way we can design 64-point FFT by combining 2, 32-point FFT‟s.

This process can be used to build any number of FFT by using 2 blocks; for ex: 128-point FFT can be built by 2, 64-point FFT‟s, 256-point FFT by 2, 128-point FFT‟s and so on.

Some recommendations are suggested to overcome the problem encountered during development of this project. First is to use higher fixes point representation for point value representation. Floating point format also can be considered as the solution to reduce error number representation especially for twiddle factor value which is 0.7071. Although floating point consume processing time and output latency, but it is an excellence method to overcome accuracy problem.

In the same way we can use CORDIC Algorithm to implement the Complex Multiplier so that further power will be reduced.

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