A 4-bit, 3.2 GSPS Flash Analog to Digital Converter with a new multiplexer based encoder

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ABSTRACT:

A 4-bit flash Analog to Digital converter with high speed, low power, and small area for system on chip(SoC) applications is presented. The proposed ADC is designed with gpdk 180nm CMOS technology and 1.8V power supply. In comparison to the conventional analog comparators, it uses Threshold Inverter Quantization technique to generate comparators. The replacement results in a faster digital conversion and a reduction in power that make it suitable for battery powered applications. The TIQ comparator does not need a resistor ladder network because it uses built in reference voltage of the CMOS inverters for comparison. Proposed flash ADC uses a new mux based encoder which converts Thermometer code into Gray code. Gray codes are mainly used in glitches free fast circuit design and in communication for error correction in digital modulation techniques. The maximum sampling frequency of this ADC is 3.2GSPS. This ADC consumes 4:93mW power at 3:2GSPS. INL and DNL of proposed ADC are 0:775LSB and 0:15LSB respectively. The proposed A/D converter is suitable for mobile applications and other system on chip applications.

TIQ FLASH ADC ARCHITECTURE:

In TIQ technique each comparator is uniquely designed to set reference voltage internally. TIQ technique uses two cascaded CMOS inverters as a comparator. This technique proposed here has to be developed for better implementation in Soc applications. The TIQ technique reduces the ADC chip area and power consumption as compared to the traditional flash ADCs. The Flash ADC architecture, also known as parallel ADCs, are the fastest among all other ADCs, but it is used for low resolution applications due to large number of comparators. The sub section describes comparator and proposed mux based architecture in detail:

TIQ comparator: In the TIQ comparator switching voltage of CMOS is used as a reference voltage for comparison[1]. It consists two back to back CMOS inverter and they are connected as a series combination with same channel width (Wn=Wp) ratio. CMOS inverters switching threshold is the point where input voltage is equal to output voltage (Vin =Vout) and at that point both transistor nMOS and pMOS always operate in saturation region. Comparators threshold voltage can be obtained by equating the current equations of both nMOS and pMOS transistors, by taking same channel length (Ln = Lp) and gate oxide capacitance (Cox). To make threshold of comparator output sharp and to provide full digital output voltage swing ,we used gain boosters after comparator.

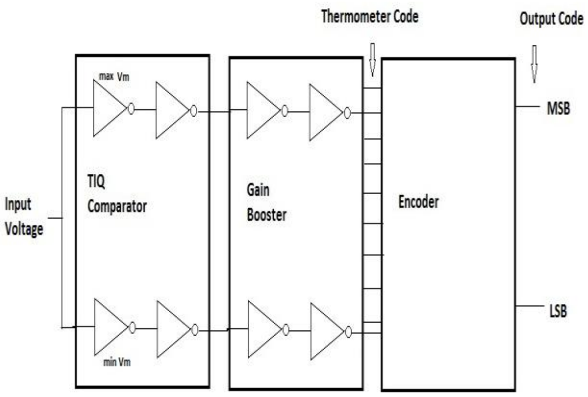

Fig. 1. Block diagram of the TIQ ADC

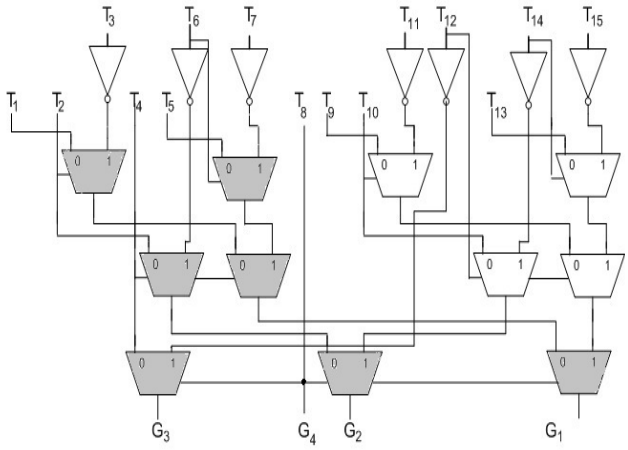

Fig. 3. Mux based Thermometer to Gray converter

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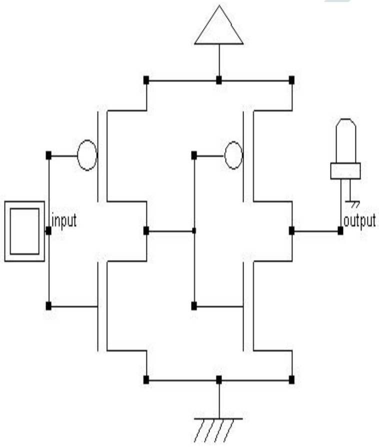


Fig. 2. TIQ comparator

COMPARATORS TRANSISTOR PARAMETERS

Parameters	Values
W_{pmax}	3.6um
W_{pmin}	0.49um
W_{nmax}	3um
W_{nmin}	1.85um
$L_{n=Lp}$	0.1um
u_n	340cm^2/Vs
u_p	240cm^2/Vs

If the input reach at a particular threshold voltage output state will change. Threshold voltage of CMOS inverter is given by the equation:

$$V_m = \frac{\sqrt{\frac{u_p.W_p}{u_n.W_n}}.(V_{dd}-|V_{Tp}|)+V_{Tn}}{1+\sqrt{\frac{u_p.W_p}{u_n.W_n}}}$$

Where,

u_n = Mobility of nMOS
u_p = Mobility of pMOS
V_{dd}= Supply voltage
V_{Tn}= Threshold voltage of nMOS
V_{Tp}= Threshold voltage of pMOS

So threshold voltages can be calculated by varying the width W_p and W_n of pMOS and nMOS transistor respectively as shown in table.

W_p	W_n	Threshold vtg
3.6	1.85	0.61
3.55	2.1	0.59
3.34	2.5	0.57
3.1	2.5	0.55
3.28	3	0.53
2.87	3	0.51
2.41	3	0.49
2.09	3	0.47
1.78	3	0.45
1.47	3	0.43
1.25	3	0.41
0.97	3	0.39
0.76	3	0.37
0.61	3	0.35
0.49	3	0.33

THRESHOLD VALUES FOR TIQ

1. Design a minimal size inverter, so that:
Vm = Vdd/2
2. Set the safe input analog range (AR), with:
ARmax =Vdd - (|VTp| + VTn)
3. Calculate the least significant bit (LSB) voltage:
LSB =AR/ (2n - 1), (for a n-bit ADC)
4. Calculate the reference voltages (Vref) from:
Vref(k) = Vmin + k * LSB, $0 < k < 2^n - 2$

ENCODERS FOR FLASH ADC

Many digital encoders for converting thermometer code to gray code have been presented in the literature as follows:

A.Wallace tree based encoder :

The wallace tree based encoder is very straight forward approach to convert Thermometer code into Gray code,which count the number of 1s. Fig. 4 shows the self re-configurable property of 4 bit wallace tree based encoder. When it is used as 3 bit encoder, only light blue colored full adders work as shown in Fig. 4.

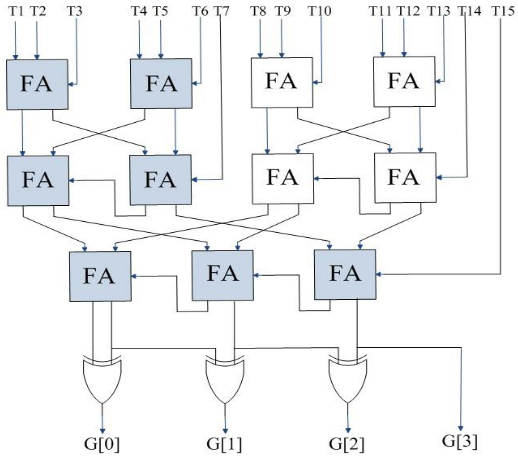
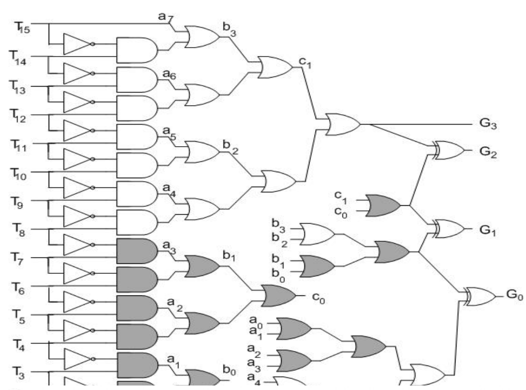


Fig 4: Wallace tree based encoder

B. Fat tree based encoder :

A more efficient approach of converting Thermometer code to Gray code is to use Fat tree based encoder. It has lesser area and delay when compared to Wallace tree based encoder. This encoder also shows self re-configurable property. Fig. 5 shows the implementation of fat tree based encoder for 15-bit thermometer code input.



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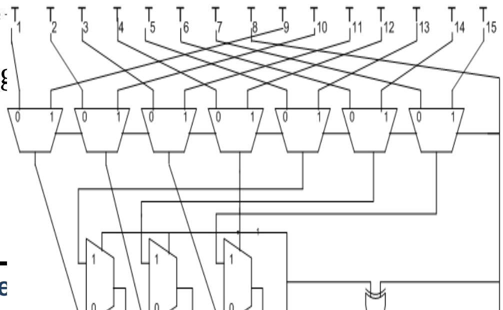


C. Existing mux based encoder :

A mux based Thermometer code to Gray code encoder is proposed. This encoder results in higher speed and smaller area as compared to wallace and Fat tree based encoders. Fig. 6 shows the implementation of MUX based encoder for 15-bit thermometer code input.

Fig 6: Existing mux based encoder

D. Proposed mux based encoder :

The proposed 15-bit Thermometer to Gray encoder is shown in Fig.3. This encoder gives better results than the existing mux based encoder in terms of power, delay, area and figure of merit. The boolean expressions of proposed 15 bit Thermometer to Gray encoder are as follows:

G4 = T8

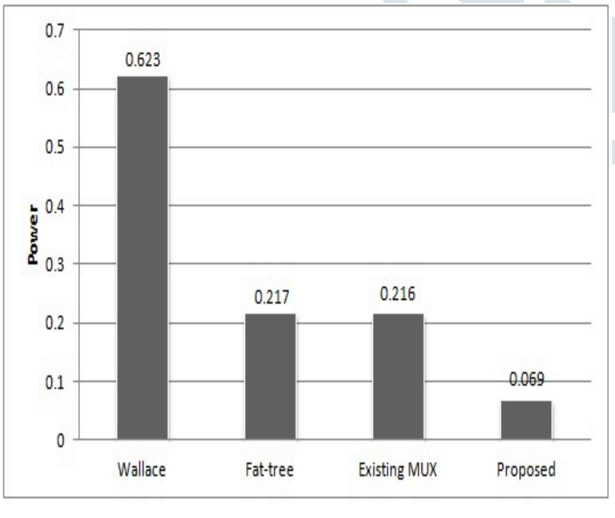
G3 = T_8:T4 + T8:T_12

G2 = T_8(T_4:T2 + T4:T_6) + T8((T_12:T10 + T12:T_14)

G1 = T_8[T_4:(T_2:T1 + T2:T_3) + T4:(T_6:T5 + T6:T_7)] + T8[T_12:(T_10:T9 + T10:T_11) + T12:(T_14:T13 + T14:T_15)]

This encoder can be configured to operate as a 7-bit Thermometer to Gray encoder by making the MSB bits T8-T15 as logic zero. In this case only the gray colored 2 : 1 muxs are working. The 15-bit Thermometer to Gray encoder can be operated as two 7-bit Thermometer to Gray encoders by making the T8 signal as logic one and latching the intermediate outputs of the 7-bit Thermometer to Gray encoder which has T1-T7 as inputs. This property is unique to the proposed mux based encoder and is not present in any of the existing encoder designs.

Simulation outputs:



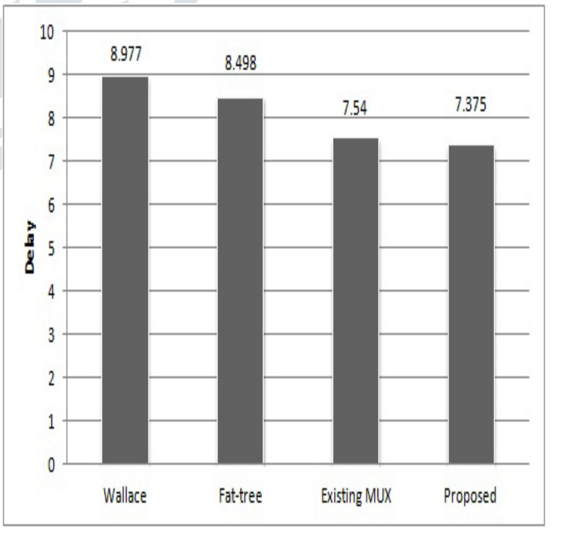


Fig 8: Power consumption of different encoders

Fig 7: Delay comparison of encoders

SIMULATION RESULT

POWER CONSUMPTION FOR DIFFERENT OPERAND LENGTHS

	7-bit(for 3- bit flash ADC)	15-bit(for 4-bit flash ADC)
Wallance Tree	0.173	0.290
Fat tree	0.105	0.151
Existing Mux Based	0.091	0.121
Proposed	0.035	0.046

	Delay (ns)	Area (m2)	Power (mW)	Figure of Merit(fJ)
Wallace Tree	8.977	13520	0.623	5592.671
Fat tree	8.498	6984	0.217	1844.07
Existing Mux Based	7.540	3640	0.216	1628.64
Proposed	7.375	3496	0.069	511.58

The table shows the power consumption of all the encoders.

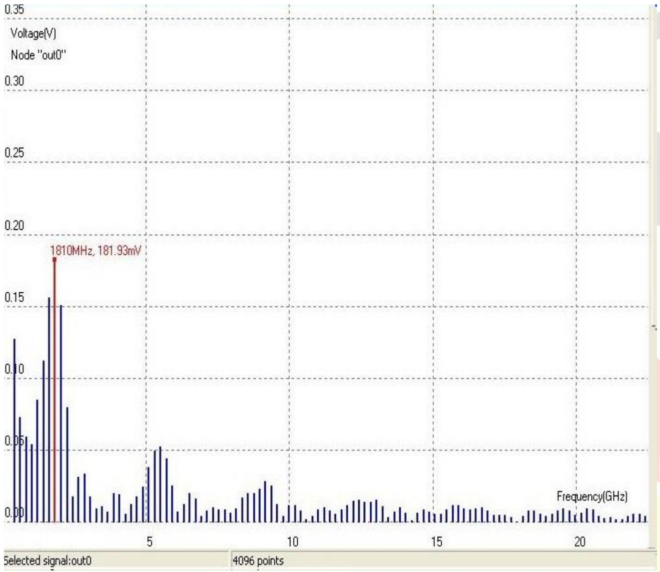


Fig. 9. FFT of output bit G1

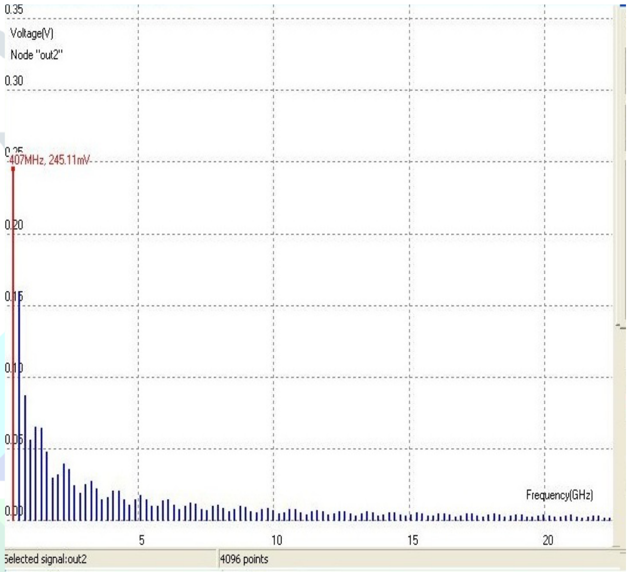


Fig. 11. FFT of output bit G3

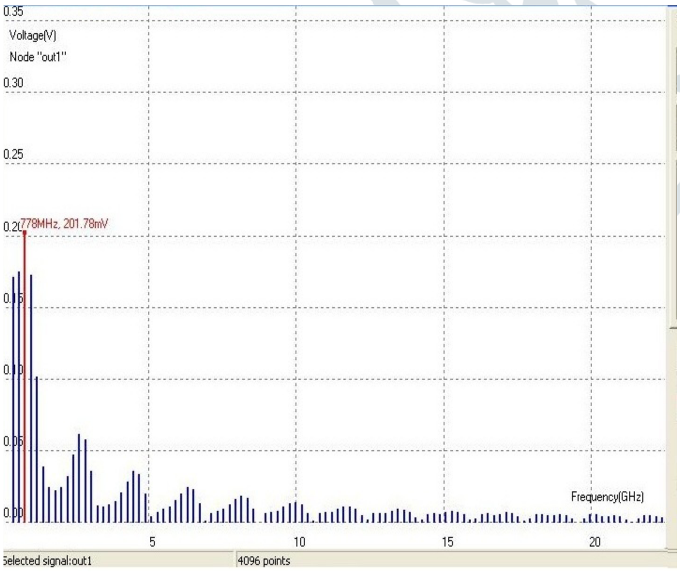


Fig. 10. FFT of output bit G2

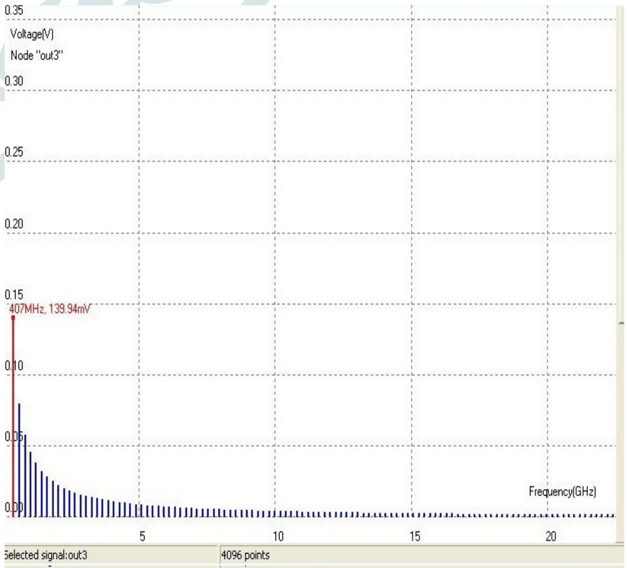


Fig. 12. FFT of output bit G4

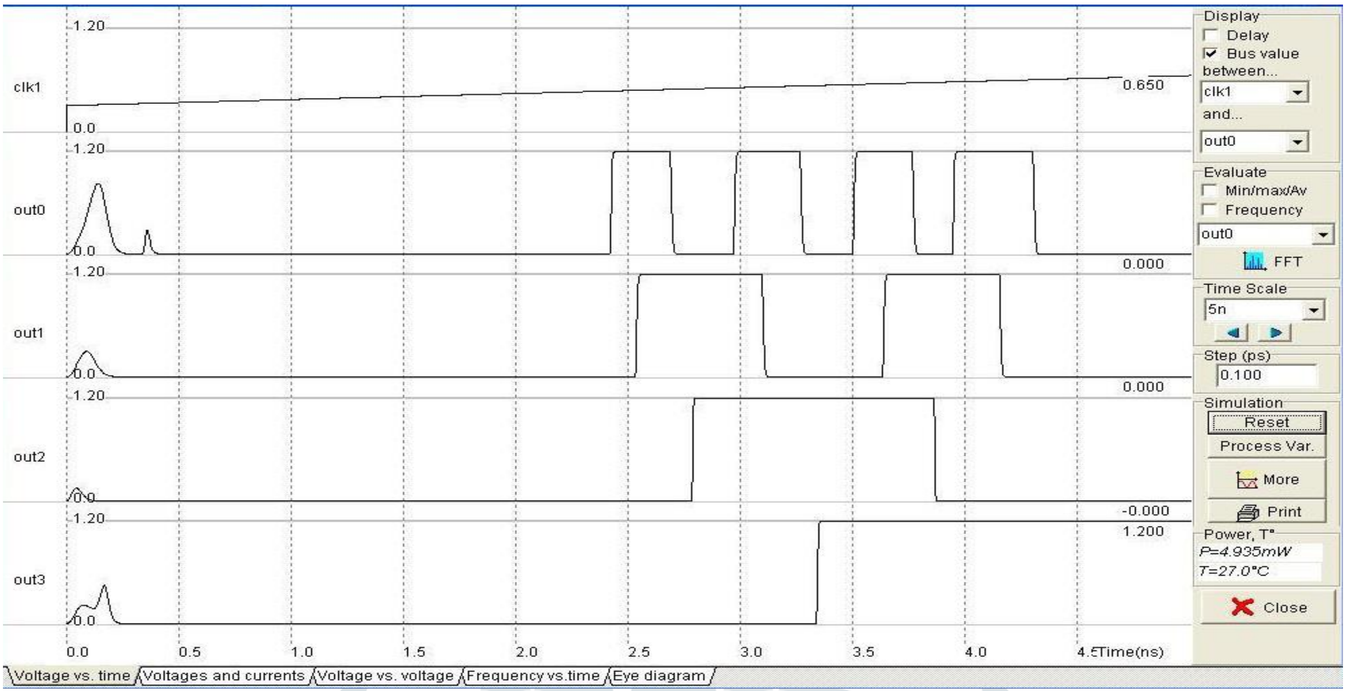


Fig. 13. Simulation result of 4 bit ADC

ADVANTAGES:

- High speed.
- Low power consumption.
- Small area for system on chip.

APPLICATIONS:

- The ADC enables high –frequency applications(typically in a few GHz range)like Radar detection, wide band radio receivers, electronic test equipment, and optical communication links.
- More often the flash ADC is embedded in a large IC containing many digital decoding functions.
- A small flash ADC circuit may be present inside a delta-sigma modulation loop.
- Flash ADCs are also used in NAND flash memory.

CONCLUSION:

A new TIQ based flash ADC is implemented which eliminates the use of resistive array, is used to design 4 bit ADC which gives Gray code as an output. A new mux based Thermometer code to Gray code converter is proposed which also reduces the power consumption.The pre simulation was implemented in Cadence v6.1 Simulation results obtained using Microwind v3.5 shows a maximal 3:2GSPS sampling rate for ADC with nominal 4:93mW power consumption. Therefore, this approach of proposed ADC is suitable for SoC applications, where reduced area and power with high speed conversion are the prime requirements.Gray codes are mainly used in glitch free fast circuit design, in communication for error correction in digital modulation techniques and in digital design for data path synchronization.Therefore the proposed ADC can be used for these applications.

FUTURE SCOPE: The proposed converter could be redesigned by reducing the technology scaling.