Date: 06/02/2019

Notice

It is hereby informed that **"Workshop on PCB Designing"** is arranged on 22nd, 23rd & 24th February 2019 by Mr. Tulsidas Salunke, Electrosal Hi Tech Pvt. Ltd. in HIT campus. The interested students are informed to register their name towards Prof. Shreevijay Ittannavar, ISTE coordinator.

Course Fee: Rs 300/- per participants.

IIIC Convener | ISTE Coordinator | ECSA Coordinator | HOD Electronics & Comm. Engg. Dept. HSIT NIDASOSHI

	S J P N Trust's **Hirasugar Institute of Technology, Nidasoshi.** *Inculcating Values, Promoting Prosperity* Approved by AICTE, Recognized by Govt. of Karnataka and Affiliated to VTU Belagavi. Accredited at "A" Grade by NAAC and Recognized Under section 2(f) of UGC	ECE Dept. IIIC, ECSA Workshop 2018-19(Even)

"PCB Designing and Testing "

In association with

Electrosal Hi Tech Pvt.Ltd.Nipani

Outcomes of the Workshop:

Students will be able to:

- Use software tool for PCB Design.
- Develop circuit schematic and PCB layout.
- Fabrication of PCB like printing,etching,drilling,component mounting and soldering.Intro
- Generate Gerber File.
- Do hobby projects.

Syllabus:

Unit 1: Introducion to Eagle PCB tool,A simple example: Schematic entry to PCB layout,Schematic Entry in detail:Creating custom components,importing standard libraries,Tools for creating components,Generating Net list from schematic: Annotation schemes,Matching schematic symbols to footprints,Board layout:Importing Net list,Foot print layout and form factor,Layers of design,Single layer,multilayer designs,Manual routing,Custom Tracks and vias,track width caalculation,auto routing,outline routing tools,generating custom routes. (6 Hours)

Unit 2:

Assignments for students to generate PCB layout for simple circuit. (5 Hours)

Unit 3:

PCB Fabrication: Quick Presenation on PCB fabrication,Printing on photo paper,etching,drilling,component mounting,soldering and testing.(7 Hours)

Unit 4:

Masking, silkscreen, Gerber file generation : Finalizing the design,Gerber file format for different layers,appending multiple boards.(6 Hours)

Unit5 :

Designing simple PCB. (Hands on session 6 Hours)

IIIC Convener

ISTE Coordinator

ECSA Coordinator

HOD
Electronics & Commn. Engg. Dept,
HSIT NIDASOSHI

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Recognized Under Section 2(f) of UGC ACT, 1956

ECE Dept.
IIIC, ISTE
Workshop
2018-19 (Even)

Registration Sheet

Sl. No.	Name of Student	Department	Sign
1.	Sangeeta Ragha	ECE	
2.	Sapna Yegappagol	ECE	
3.	Ashwini Kori	ECE	
4.	Arpita Bhajantri	ECE	
5.	Veena Pagi	ECE	
6.	Sushma Hubballi	ECE	
7.	Dishwarya Pagi	ECE	
8.	Vinit Kanth:	ECE	
9.	Anagh Dadi	ECE	
10.	Vinayak Tuppadoddi	ECE	
11.	Avinash Sunthe	ECE	
12.	Veda Nagennavar	ECE	
13.	Vaishali Muchandi	ECE	
14.	Shruti Muradunde	ECE	
15.	Shraddha Muradunde	ECE	
16.	Nityashree Pagi	ECE	
17.	Priyanka Telagade	ECE	
18.	Preeti Nadodage	ECE	
19.	Nikhita Mane	ECE	
20.	Nisarga Bagalkot	ECE	
21.	Prajakta Naradi	ECE	
22.	Sneha Bannuri	ECE	
23.	Pavitra Ranganagi	ECE	
24.	Danamma, I, Nadi	ECE	
25.	Meenakshi, B patil	ECE	
26.	Kiran D. Kelaginamani	ECE	
27.	Akshata. C. shivannavar	ECE	
28.	Pratima S. Tugalakar	ECE	
29.	Snehal. S. Gurav	ECE	
30.	Laxmi Pagi	ECE	
31.	Shivani U Kanerkar	ECE	
32.	M. D. Tanveer. S. SHAIKH	ECE	
33.	Supriya Kulkarni	ECE	
34.	Sunita Hanamadwade	ECE	
35.	Soumya. M. Metagudli	ECE	
36.	DALAWAI. LAXMI. DUNDAPA	ECE	
37.	Abhishek. S. M	ECE	
38.	Mallikarjun. S. P	ECE	
39.	Adarsh. P. Madihalli	ECE	
40.	Praveenkumar Ankad	ECE	
41.	~~Pavitra S Ranganagi~~	ECE	
42.			

IIIC Convener ISTE Coordinator ECSA Coordinator

Page No.
Date: 8/8/03/03/2019

Event: Workshop on PCB Designing & Testing.

Topic: PCB design & Testing.

Resource person: Mr. Tukaram Salunkhe
Electrocal Hi Tech Pvt. Ltd. Nipani

Audience: 4th sem & 6th sem students.

Date: 01/08/2019 to 08/08/2019. Time: 8.00 am to 6.00 pm.

Venue: 4th sem class room (D 211) & Microprocessor lab (D304 & LSC & communication Lab D305)

Sr No.	Name of students	USN.	Sign.
01	Abhishek Malgondkar	2HN17EC001	
02	Adarsh Hadihali	2HN17EC002	
03	Aishwarya Patil	2HN17EC003	
04	Akshata Shivannavar	2HN17EC004	
05	Amogh Dodd	2HN17EC005	
06	Arpita Bhajantri	2HN17EC006	
07	Ashwini Kori	2HN17EC007	
08	Avinash Suthe	2HN17EC008	
09	Danamma Neeli	2HN17EC009	
10	Kiran Kelagimanni	2HN17EC010	
11	Laxmi Patil	2HN17EC011	
12	Mallikarjun Pawadi	2HN17EC012	
13	Meenakshi Patil	2HN17EC013	
14	Nikhita Mane	2HN17EC014	
15	Nisarga Bagalkot	2HN17EC015	
16	Nityashree Patil	2HN17EC016	
17	Pallavi Panjanavi	2HN17EC017	

Page No.
Date : / /

Sl No	Name of Student	USN	Sign
19	Praveenkumar Akkad	2HN17EC020	Approved Form
20	Preeti Masodage	2HN17EC021	Preetidaf
21	Priyanka Teggade	2HN17EC022	
22	Sangeeta Ragha	2HN17EC023	
23	Sapna Yegappagol	2HN17EC024	
24	Shivani Kanerkar	2HN17EC025	Kanerkar
25	Shraddha Murudande	2HN17EC026	
26	Shruti Murudande	2HN17EC027	
27	Sneha Bansuri	2HN17EC028	Sbansuri
28	Snehal Gurav	2HN17EC029	Gurav
29	Sunita Hiremade	2HN17EC030	Sthiremadwade.
30	Supriya Kulkarni	2HN17EC031	Kulkarni
31	Surekha Hubballi	2HN17EC032	
32	Vaishali Muchandi	2HN17EC033	
33	Veda Nagesnavar	2HN17EC034	
34	Veena Patil	2HN17EC035	
35	Vinayak Tupparathi	2HN17EC037	
36	Vinit Karthi	2HN17EC038	
37	Mohamed Shaikh	2HN18EC400	
38	Pratima Tugulkar	2HN18EC401	
39	Dalawai Laxmi	2HN16EC013	L.Dalawai
40	Sangeeta Hergudli	2HN16EC034	
41	Abhishek Khadarbad	2HN16EC081	

Sr No.
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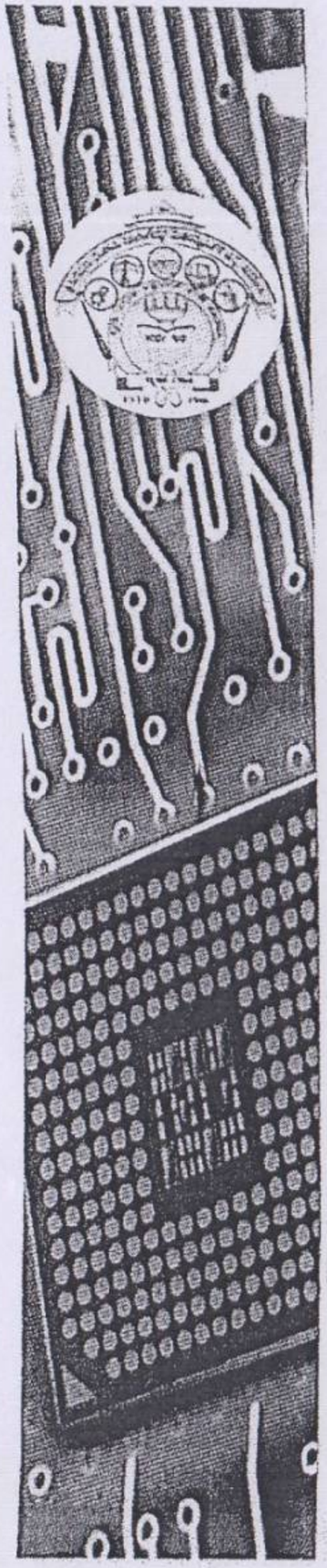

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HIRASUGAR INSTITUTE OF TECHNOLOGY

NIDASOSHI-591236

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Department of Electronics and Communication Engineering
In Association with ECSA, IIIC & ISTE Student Chapter

Three Day's Workshop On

"PCB Design & Testing"

Certificate

This is to certify that Mr./Miss Nityashru P. Patil
of 4th Sem ECE Dept. HIT Nidasoshi *has actively participated three days' workshop on "PCB Design & Testing" Conducted by Electrosal HiTech Pvt. Ltd. Nippani on 1st to 3rd March 2019 at Hirasugar Institute of Technology, Nidasoshi.*

Mr. T D Salunkhe
CEO Electrosal Pvt. Ltd. Nippani

Dr. V G Kasabegoudar
HOD

Dr. S C Kamate
Principal

QUESTIONS RESPONSES 43

Section 1 of 2

"Impact Analysis of Workshop on PCB

Form description

Email address *

Valid email address

This form is collecting email addresses. Change settings

After section 1 **Continue to next section**

Section 2 of 2

" "Impact Analysis of Workshop on PCB Design.

Description (optional)

Test on "PCB Design and Testing" Workshop
Marks: 10 Time: 20 Minutes
(Tick the Right Answers for the Multiple Choice Questions)

Description (optional)

1) What is the file extension for schematic file? *

B) .brl

C) .sch

D) .scl

2) Which tool is used to Change the track in board file? *

A) Ratsnet

B) Move

c) Delet

D) Ripup

3) Which option is need to select for change the width unit (from inch to mm) in board file. *

A) Grid

B) CAM

C) Ratsnet

D) Group

4) Which tool is used for make a Gerber file?

A) Grid

B) CAM

C) Ratsnet

D) Ripup

Add option or ADD "OTHER"

Required

9) Which chemical used for etching process. *

- A) Ferric chloride
- B) Zinc chloride
- C) Ferrous acid
- D) Sulfuric Acid.

10) ..... is used for connection between bottom layer and top layer. *

- A) Drill
- B) Route
- C) Pth
- D) Soldering

- A) Removal of heat
- B) Keeping wires outside easily.
- C) Reduction of path length
- D) All of the above

6) How Do You Verify Schematic Symbols Or Footprints? *

- 1) Cross verify with datasheets
- 2) print footprints and match with actual devices
- 3)BOTH 1 & 2
- 4)NONE

7) What Is Need for a PCB? *

- 1) Designs on bread boards or per boards are cumbersome, to have neat placement of components without j...
- 2) It helps in providing physical stability
- 3) Overall circuit is more reliable.
- 4) All.

8) What are the inputs you need to design a PCB? *

- A) We need schematic.
- B) Components Size.
- C) Input and output signals.
- D) All.

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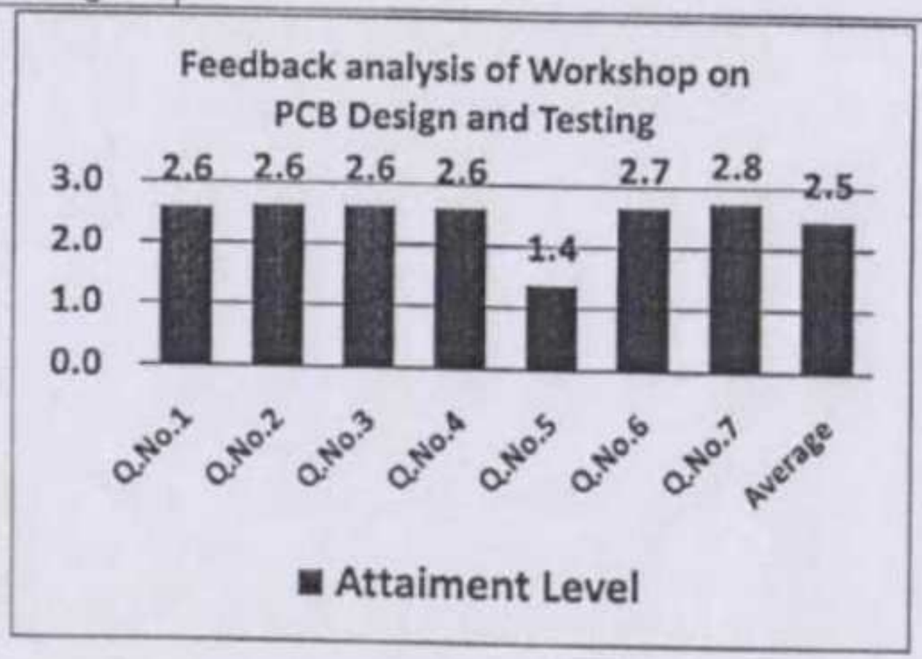
Title of Event: Workshop on PCB Design and Testing

Number of Students: 41

Q. No.	Excellent(4)		Very good(3)		Good (2)		Satisfactory(1)		Poor(0)		Total score	% of attainment = (Total score/Total Students Attended)	Average Percentage attainment	Attainment Level	Mapped Pos	Mapped PSOs
Q.No.1	15	60	9	27	7	14	5	5	3	0	106	2.6				
Q.No.2	16	64	8	24	8	16	4	4	3	0	108	2.6				
Q.No.3	13	52	14	42	5	10	4	4	3	0	108	2.6				
Q.No.4	14	56	9	27	9	18	6	6	1	0	107	2.6				
Q.No.5	14	56	0	0	0	0	0	0	0	0	56	1.4				
Q.No.6	13	52	12	36	8	16	5	5	1	0	109	2.7				
Q.No.7	16	64	12	36	4	8	5	5	2	0	113	2.8				
Average												2.5	61.6	Medium = 2	1,2,5,9, 10,12	2



Impact Analysis: From the above Table,three days workshop on PCB Design and Testing event mediumly attained to level 2 against mapped PO1, PO2, PO5, PO9, PO10, PO12 and PSO2.

NOTE: Substantial or high = 3, Medium = 2 and Low = 1

IIIC Coordinator (Prof. D.M. Kumbhar)

NBA Coordinator

HOD
Electronics & Commn. Engg. Dept
HSIT NIDASOSHI