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FIRST INTERNAL ASSESSMENT TEST

Sem: VIII EC | Sub: Real time Operating systems | Sub. Code: 10EC842

Time: 3:00pm-4:00pm | Max. Marks: 25 | Date: 07/03/2018

Note: Answer two full questions, draw sketches wherever necessary.

Q. No		Description of Question	Marks	CO	RBT Level
1	a	Define Real time System.Write & explain a pseudocode outline of a basic event driven software service.	7	C412E.1	L1,L2
		OR			
	b	With diagrams,explain all the parts in a real time service timeline with & without hardware acceleration.	7	C412E.1	L1,L2
	c	With diagram explain Distributed continuous media real time services.	6	C412E.1	L1,L2
		OR			
	d	List & explain the following Real Time: 1) Standards 2) Extensions of POSIX 1001.1b 3) Additional Real time standards.	6	C412E.1	L1,L2
2	a	With neat sketch explain Real time embedded system resource characterization & explain the design factors that decide resource margin & guidelines for resource sizing & margin maintenance.	6	C412E.2	L1,L2,L3
		OR			
	b	Explain the following with graphs & example: i) Hard real time system ii) Isochronal real time system(Soft) iii) soft real time system.	6	C412E.2	L1,L2,L3
	c	With example show that RM Priority assignment policy is optimal & prove that the only alternative is not optimal for the same example.	6	C412E.2	L1,L2,L3
		OR			
	d	Draw the resource scheduling taxonomy & explain the concept of Multiprocessor systems.	6	C412E.2	L1,L2,L3

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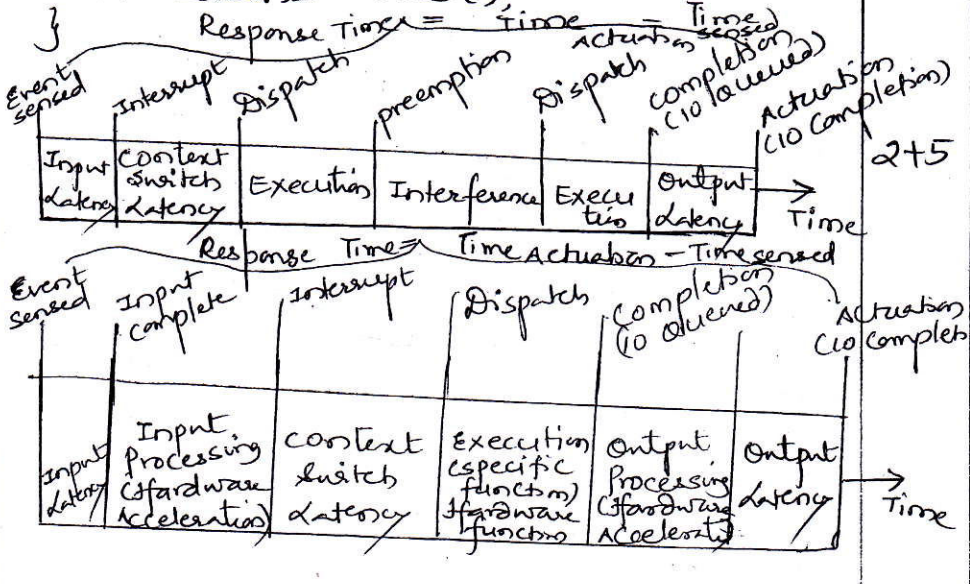
ECE Dept. | Exam. | IA Scheme Evaluation | Even Sem (2017-18)

SCHEME OF EVALUATION

Sem : VIII | Subject : RTOS | Sub Code : 10EC 842 | Date : 7/3/2018

Q. No.	Bit	Description	Marks	CO's	RBT LEVEL

1	a)	Definition & pseudocode outline of a basic event driven s/w service
		`void provide_service(void)`
		`{`
		`if(initialize_service()==ERROR)`
		`exit(FAILURE_TO_INITIALIZE);`
		`else`
		`in_service=TRUE;`
		`while(in_service)`
		`{`
		`if(waitFor(service_request_event,timeout)!=TIMEOUT)`
		`{`
		`read_input(input_buffer);`
		`output_buffer=do_service(input_buffer);`
		`write_output(output_buffer);`
		`}`
		`else post_timeout_error();`
		`post_service_aliveness(serviceIDself());`
		`}`
		`shut_down_service();`
		`}`
			2+5	C412 E.1	L2

	b)		2+5	C412 E.1	L2

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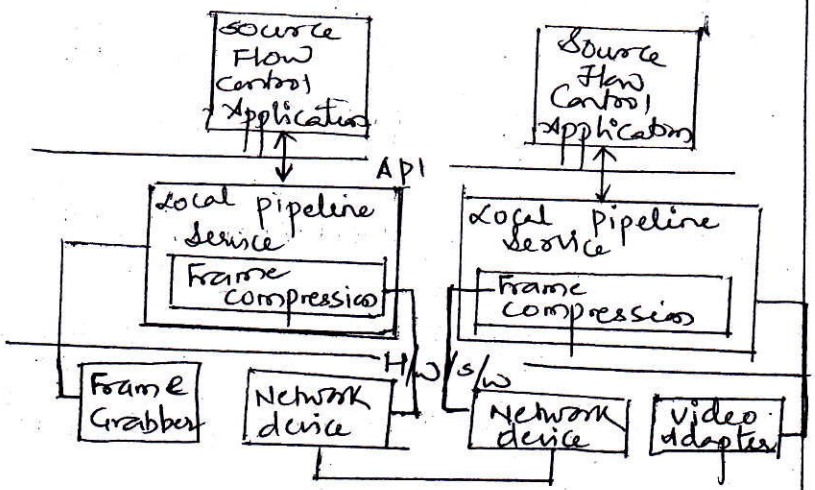
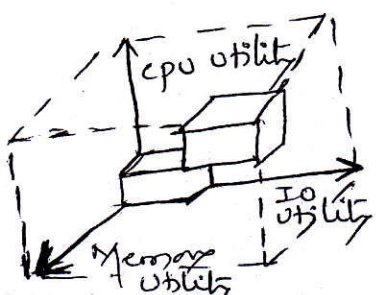
Even Sem (2017-18)

SCHEME OF EVALUATION

Sem : 8th | **Subject : RTOS** | **Sub Code : 10EC 842** | **Date : 7/3/2018**

Q. No.	Bit	Description	Marks	CO's	RBT LEVEL
1	c)		6	C412 E. 1	L2
	d)	1) IEEE Std 2003.1b-2000; IEEE Std 1003.13-1998; IEEE Std 1003.1b-1993; IEEE Std 1003.1c-1995; IEEE Std 1003.1d-1999; IEEE Std 1003.1j-2000; IEEE Std 1003.1q-2000; Extensions 1003.1b • Priority Scheduling • Real Time Signals • Clocks & Timers • Semaphores • Message passing • Shared Memory • Asynchronous & Synchronous I/O • Memory locking	6	C412 E. 4	L2
		Additional Real Time Standards: • DO-178B • JSR-1 - object Management Group RT CORBA 1.0 • IETF, RTP, RTCP • IETF RTSP • ARINC-653			
2	a)		6	C412 E. 2	L3

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SCHEME OF EVALUATION

Sem : 8th **Subject :** RTOS **Sub Code :** 10EC 842 **Date :** 7/3/2018

Q. No.	Bit	Description	Marks	CO's	RBT LEVEL
2	b)	• System cost • Reliability req'd • Availability req'd • Risk of oversubscribing resources • Impact of oversubscription Guidelines for resource sizing & margin maintenance • CPU • I/O • Memory	6	C412 E.2	L3
2	b)	1) Hard RTS: Release, Deadline, 100%, Utility, 0%, Time, After deadline Utility is -ve 2) Soft Isochronous: Release, Deadline, 100%, Utility, F(t), 0%, Time, Before Deadline Utility is <100%, After Deadline Utility is <100% 3) Release, Deadline, 100%, Utility, F(t), 0%, Time, After Deadline Utility Diminishes according to some Function F(t)	6	C412 E.2	L3

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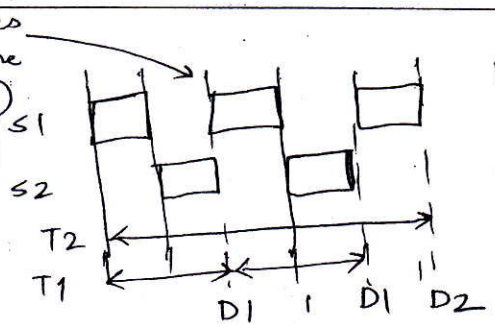
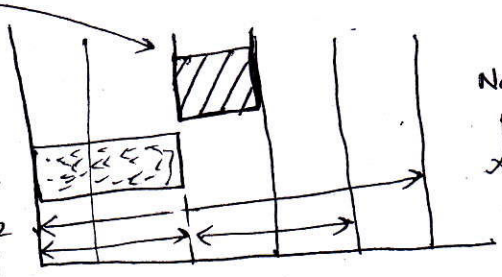
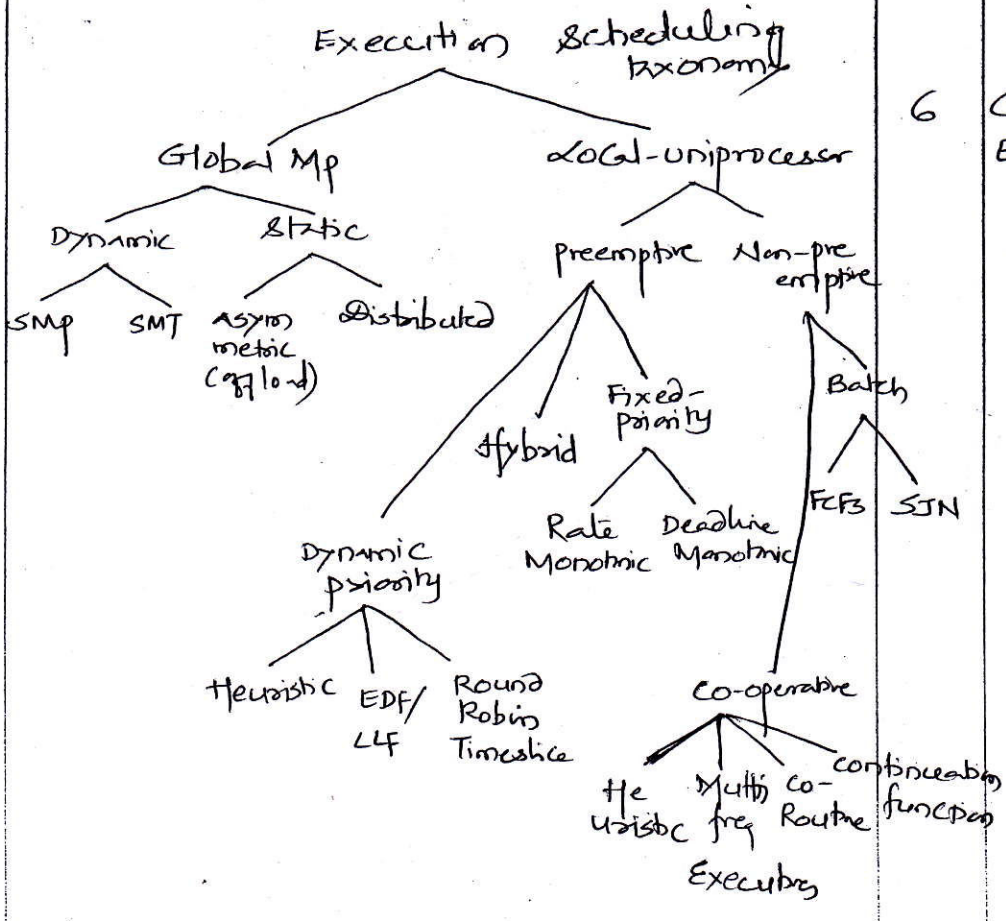
SCHEME OF EVALUATION

Sem : 8th	Subject : RTOS	Sub Code : 10EC842	Date : 7/3/18

Q. No.	Bit	Description	Marks	CO's	RBT LEVEL
2	c)	S_1 makes Deadline if $prio(S_1) > prio(S_2)$  Eg: RM priority assignment policy	6	C412 E.2	L3
		S_1 Misses Deadline if $prio(S_2) > prio(S_1)$  Non optimal priority Assignment policy			
2	d)		6	C412 E.2	L3

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SECOND INTERNAL ASSESSMENT TEST

Sem: VIII EC | Sub: Real time Operating systems | Sub. Code: 10EC842

Time: 3:00pm-4:00pm | Max. Marks: 25 | Date: 12/04/2018

Note: Answer two full questions, draw sketches wherever necessary.

Q. No		Description of Question	Marks	CO	RBT Level
1	a	Define RM LUB.Explain preemptive fixed-priority policy taking the example of two services.	7	C412.3	L2
		OR			
	b	i) What is feasibility?Explain Sufficient & N & S feasibility tests & draw the diagram of Relationship between Sufficient & N & S feasibility tests. ii) Determine the equation of utility in case of RM LUB for the case: C1 short enough to fit all three releases in T2 with diagram.	7	C412.3	L3
	c	With equations describe Scheduling Point & Completion time test.Explain Deadline Monotonic Policy & find the equation for the partial interference.	6	C412.3	L3
		OR			
	d	With diagrams explain RM Policy overload scenario & EDF Policy cascading failure overload scenario.	6	C412.3	L2
2	a	What is blocking ? Explain with neat figure the concept of Deadlock & Livelock.	6	C412.4	L2
		OR			
	b	i) Define Priority inversion. What causes unbounded priority inversion? ii) With equation explain the concept of Power management & Processor Clock modulation.	6	C412.4	L2
	c	Explain how missed deadlines can be handled in case of Soft Real Time Services.	6	C412.4	L2
		OR			
	d	What is QOS explain? Explain the concept of Mixed Hard & Soft real time services.	6	C412.4	L2

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ECE Dept | Exam | IA Scheme | 2017-18 (Even)

SCHEME OF EVALUATION IA -

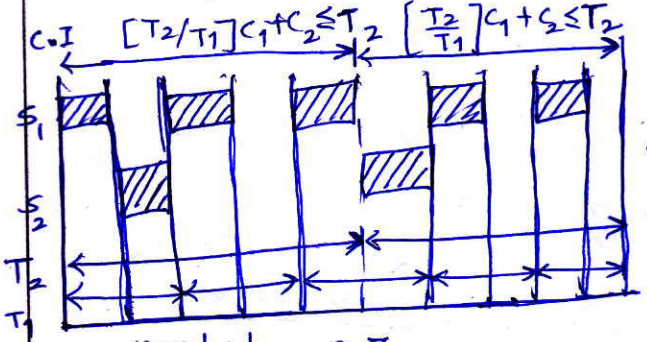
Page No : /

SEM:		SUBJECT:	SUBJECT CODE:	DATE:	
Q.No.	Bits	DESCRIPTION		Marks	CO's

1 a) RM LUB is defined as

$$U = \sum_{i=1}^{m} \left(\frac{C_i}{T_i}\right) \leq m\left(2^{\frac{1}{m}} - 1\right)$$

U → utility of the CPU resource achievable
C_i → Execution time of service i
m → Total no of services in the system sharing common CPU resources.
T_i → Release period of service i



$U = \frac{1}{2} + \frac{1}{5} = 0.7$

$U = 0.7 \leq 2(2^{1/2} - 1) \leq 0.83$

All services might be requested at the same time - critical instant

Marks: 3+4 | CO's: C412.3, L2

b) Feasibility test provides a binary result that indicates whether a set of services (threads or tasks) can be scheduled given their C_i, T_i & D_i specification. I/p is an array of service identifiers (S_i) & specifications for each, & the O/p is TRUE if the set can be safely scheduled so that none of the deadlines will be missed & FALSE if any one of the deadlines might be missed.

Sufficient: will always fail a service set that is not real time safe.
will also fail a service set that is real time occasionally as well.
Are not precise.

N&S feasibility tests: will not pass a service set that is unsafe & likewise will not fail any test that is safe.

Marks: 2+5 | CO's: C412.3, L3

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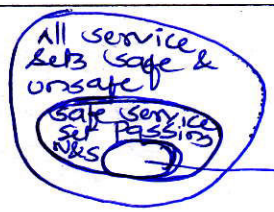
SCHEME OF EVALUATION IA -

Page No : /

SEM:	SUBJECT:	SUBJECT CODE:	DATE:

Q.No.	Bits	DESCRIPTION	Marks	CO's



safe service set passing sufficient test.

ii)

Eq2 - 1

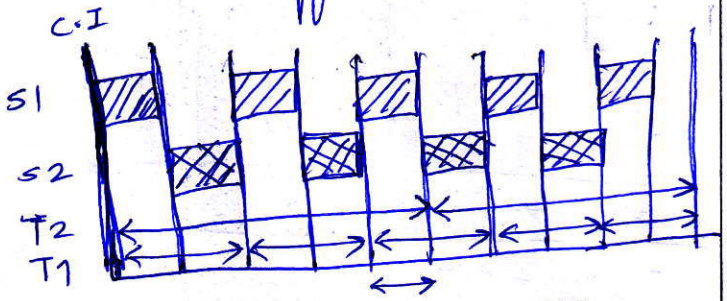
$C_1 \le T_2 - T_1\left[\frac{T_2}{T_1}\right]$

Eq2 - 2

$C_2 = T_2 - C_1\left[\frac{T_2}{T_1}\right]$

Eq - 3

$U = \frac{C_1}{T_1} + \frac{C_2}{T_2}$



$U = \frac{C_1}{T_1} + \frac{C_2}{T_2} = 1 + C_1\left[\frac{1}{T_1} - \frac{\left[\frac{T_2}{T_1}\right]}{T_2}\right]$

c) scheduling point Test:

$\forall i, 1 \le i \le n, \min \sum_{j=1}^{i} C_j\left[\frac{(l)T_k}{T_j}\right] \le (l)T_k$ — 3+3

$(k,l) \in R_i$

$R_i = \left\{(k,l) \mid 1 \le k \le i, l = 1, \ldots \left[\frac{T_i}{T_k}\right]\right\}$

CO1,2, 3 L3

DM policy: Is very similar to RM except that higher priority is assigned to the service with the shortest deadline.

- DM policy is a fixed priority policy.
- Eliminates original assumption that service period must equal service deadline & allows RM theory to be applied for scenarios even when deadline is less than period.
- Useful for dealing with significant o/p latency.
- D_i & T_i differ only by a constant value.

Sufficient feasibility tests:

$\forall i : 1 \le i \le n : \frac{C_i}{D_i} + \frac{I_i}{D_i} \le 1.0$

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SCHEME OF EVALUATION

Sem :		Subject :	Sub Code :	Date :		
Q. No.	**Bit**	**Description**		**Marks**	**CO's**	**RBT LEVEL**

$$I_i = \sum_{j=1}^{i-1} \left[\left[\left[\frac{D_i - D_j}{T_j}\right] + 1\right] C_j + \left[\left[\frac{D_i}{T_j}\right] - \left[\frac{D_i - D_j}{T_j}\right] + 1\right] \times \text{Min}\left[C_j, D_i - \left[\frac{D_j}{T_j}\right] T_j\right]\right]$$

Completion Time test:-

$$a_n(t) = \sum_{j=1}^{n} \left[\frac{t}{T_j}\right] C_j$$

1 d) 3+3 CO 2.3 L2

S_{i+1} / S_i — S_{i+1} services continue to meet deadlines. $\text{prio}(S_{i+1}) > \text{prio}(S_i)$.

S_i = over running service misses deadline

S_{i-1} services all miss their deadlines

RM policy overload scenario $\text{prio}(S_{i-1}) < \text{prio}(S_i)$

EDF policy cascading failure overload scenario

S_i = over-running

$\text{prio}(S_{i-1}) < \text{prio}(S_i)$

Terminate S_i over-run

S_i over-running

$\text{prio}(S_{i-1}) < \text{prio}(S_{i-1})$

Terminate S_{i-1} over-running

S_{i-2} = over-running

$\text{prio}(S_{i-2-1}) < \text{prio}(S_{i-2})$

2 a) 2+4 CO 4.1 L2

Blocking:- occurs any time a service can be dispatched by the CPU, but isn't b'coz it is lacking some other resource such as access to a shared memory critical section or access to a bus. when blocking has a known latency it could simply be added into response time, accounted for & therefore, would not affect RM analysis. unbounded blocking

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SCHEME OF EVALUATION

Sem : Subject : Sub Code : Date :

Q. No.	Bit	Description	Marks	CO's	RBT LEVEL
		is of bigger concern.			
2	b) i)	priority inversion is simply defined as any time that a high priority service has to wait while a lower priority service runs. Three conditions are necessary for unbounded inversion. • three or more services with unique priority in the system - High (H), Medium (M), Low (L), priority sets of services. • At least two services of diff priority share a resource with mutex protection - one or more high & one or more low involved. • one or more services not involved in the mutex has priority betw the two involved in the mutex.	3+3	C412 .4	L2
		ii) Power Management & processor clock Modulation: $P_{average} = P_{switching} + P_{short-ckt} + P_{leakage}$ $P_{switching} = (S_{prob})(C_L)(V_{supply})^2(f_{clk})$ - due to capacitor charge/discharge for switching $P_{short-ckt} = t\,(S_{prob})(V_{supply})(I_{short})$ - due to current flow when gates switch.			
2	c)	Missed deadlines can be handled in a number of ways. • Termination of the over-running service as soon as the deadline is passed. • Allowing an over-running service to continue running past a deadline	1+1 +1	C412 .4	L2

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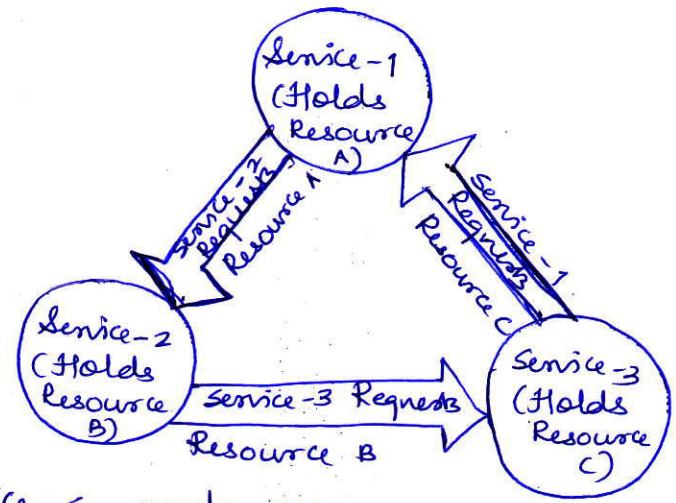
SCHEME OF EVALUATION IA-

Sem :		Subject :	Sub Code :	Date :		
Q. No.	Bit	Description	Marks	CO's	RBT LEVEL	

Deadlock & Livelock

C412.3



Service S_1 needs resources A & C,
Service S_2 needs B & C.
If S_1 acquires A, then S_2 acquires B
S_3 acquires C followed by requests by each for their other required resource a circular wait evolves.
circular wait also known as deadly embrace, causes indefinite deadlock. No progress can be made by services 1, 2 or 3 unless resources held by each are released.
Deadlock can be prevented by making sure the circular wait scenario is impossible.
when deadlock is detected & services are restarted, they could simply reenter the deadlock over & over. This variant is called livelock & also prevents progress completely despite detection & breaking of the deadlock.

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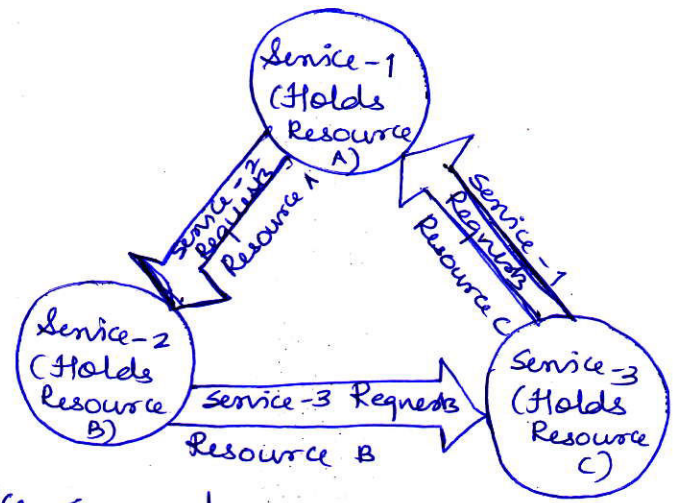
SCHEME OF EVALUATION IA-

Sem :		Subject :	Sub Code :	Date :		
Q. No.	Bit	Description	Marks	CO's	RBT LEVEL	

Deadlock & Livelock

CO1,2,3



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THIRD INTERNAL ASSESSMENT TEST

Sem:VIII | Sub: Real time Operating systems | Sub. Code: 10EC842

Time: 3:00pm-4:00pm | Max. Marks: 25 | Date: 19/05/2018

Note: Answer two full questions, draw sketches wherever necessary.

Q. No		Description of Question	Marks	CO	RBT Level
1	a	Define boot code & explain.With diagram explain device firmware interface.List the Operating system services.	7	C412.5	L2
		OR			
	b	With neat diagrams explain the concept of communicating & synchronized applications.	7	C412.5	L3
	c	List the different levels of debugging.Explain Test Access ports.	6	C412.5	L3
		OR			
	d	Describe the concept of power on self Test & Diagnostics.	6	C412.5	L3
2	a	Explain the basic concepts of Drill Down Tuning.With diagram explain hotspot drill down concept.	6	C412.6	L2
		OR			
	b	List the basic methods for building performance monitoring into Hardware & explain the concept.	6	C412.6	L2
	c	What are the basic methods for building performance monitoring into software capability into a system and explain t.he concept	6	C412.6	L2
		OR			
	d	I)Explain the following: i) Path Length ii) Efficiency iii) Calling Frequency II)Write a simple code to compute Fibonacci sequence.	6	C412.6	L2

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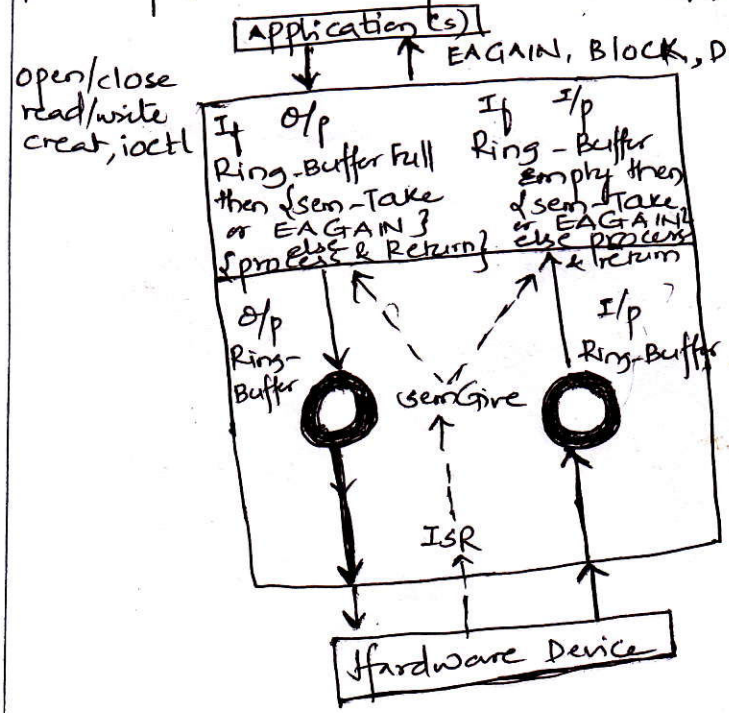
SCHEME OF EVALUATION

Sem : VIII | Subject : Real Time operating Systems | Sub Code : 10EC842 | Date : 19/05/2018

Q. No.	Bit	Description	Marks	CO's	RBT LEVEL
1	a)	code or s/w that runs out of a non-volatile device to make Hardware resources available for rest of application s/w. Explaination of Bsp:- Firmware has initialized & made available all on-board resources for a processor complex to s/w applications.	2+2 +3	C412 .5	L2



O.S services: Fundamental & Extended Services List.

Fundamental Services:

- priority preemptive scheduler for threads
- Thread control block management
- Inter-thread synchronization & comm?
- Basic I/O for system debug & bring up.
- ISR installation on interrupt vector
- Transition from boot to operational state
- Timers for delays & blocked thread timeouts
- Drivers for basic H/w devices.

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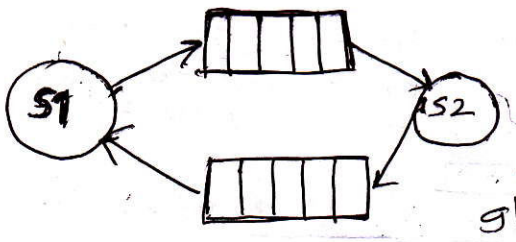
SCHEME OF EVALUATION

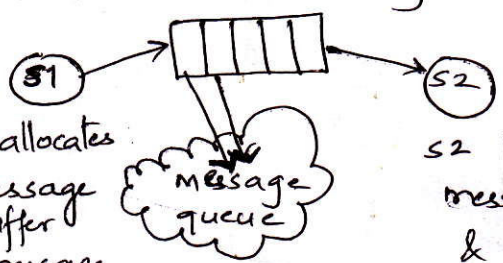
Sem :		Subject :	Sub Code :	Date :		
Q. No.	Bit	Description		Marks	CO's	RBT LEVEL

1 b)



To Synchronize & to share data or global resources. 7 C412 · 5 L3

A region of memory can be shared by two tasks & updated or read in a critical section using a mutex semaphore.



S1 allocates message buffer in message heap

S2 processes the message buffer data & frees the buffer for Re-use

c) Task or process level debugging. 2+4 C412. 5 L3
System or Kernel level debugging.
processor level debugging.

Test Access ports:-

TAP allows a JTAG to send bit patterns through the Scan chain & also ~~follows~~ allows the JTAG user to command a processor, single step it load registers & memory, download code & dump registers & memory out so that commands & data can be sent to the device under test.

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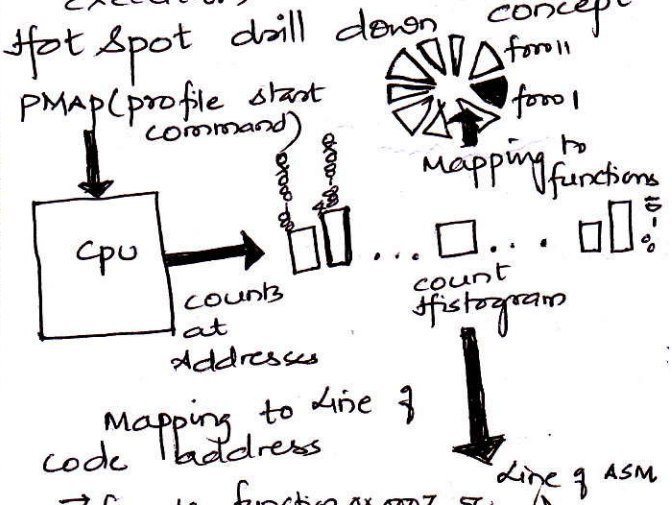
SCHEME OF EVALUATION

Sem : VIII | Subject : Real Time operating sys | Sub Code : 10EC842 | Date : 19/05/18

Q. No.	Bit	Description	Marks	CO's	RBT LEVEL
1	d)	Boot code can implement a series of diagnostic tests after a power on reset based on a nonvolatile configuration & indicate how far it has advanced in the testing since reset thro' LEDs, tones, or a record in nonvolatile memory. process is POST-method for debugging boot failures. POST codes indicates that all interfaces are okay, but that memory tests failed, then replacing memory is likely to fix the problem → o/p on a bus to memory or an external device, so probing an external bus allows you to capture POST codes & diagnose problems.	6	C412.5	L3
2	a)	Performance of firmware & s/w must be tuned to a workload. Workload is a sequence of service requests, commands, I/O's or other quantifiable transactions that exercise the software. Characteristics of code segments that most affect performance include following • Segment path length • Segment execution efficiency • Segment calling freq • Execution context. Hot spot drill down concept 	6	C412.6	L2

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SCHEME OF EVALUATION

Sem : VII | **Subject : Real Time operating system** | **Sub Code : 10EC 842** | **Date : 19/05/2018**

Q. No.	Bit	Description	Marks	CO's	RBT LEVEL
		Goal is to identify hot spots, Approach to tuning - Is to go through code from start to finish & look for efficiency issues, correct them & try running again.			
2	b)	• performance event counters. • Execution trace port. • Trace register buffer. • cycle & intervals counters for timestamping Tracing is advised after hotspots are located. Profiling supported by performance counters can not only indicate where time is spent, but also hotspots where cache is most often missed or code locations where the processor pipeline is most often stalled.	6	C412.6	L2
	c)	Building performance Monitoring into software :- **Basic Methods:-** • performance counter API • Direct code instrumentation to sample cycle & event counters for trace. • steady-state asynchronous sampling of counters through interrupts. • software event logging to memory buffer. • Function or block entry/exit tracing to a memory buffer.	6	C412.6	L2

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SCHEME OF EVALUATION

Sem : VIII | **Subject : Real Time Operating Sys** | **Sub Code : 10EC842** | **Date : 19/05/2018**

Q. No.	Bit	Description	Marks	CO's	RBT LEVEL
2	d)	path length:- Performance counters would be used to automate the acquisition of these metrics. When performance counters aren't available, you can measure path length by hand, in two different ways; I st:) By having the C compiler generate assembly code, you can then count the instructions by hand or by a word count utility. II nd) If a single step debugger is available, then you can count instructions by stepping through assembly by hand.	6	C412.6	L2

'c' code to compute Fibonacci Sequence:

```
typedef unsigned int UINT32;
#define FIB_LIMIT_FOR_32_BIT 47

    UINT32 idx=0, jdx=1;
    UINT32 seqcnt= FIB_LIMIT_FOR_32_BIT,
                   itercnt=1;
    UINT32 fib=0, fib0=0, fib1=1;
    void fib_wrapper(void)
{
  for(idx=0; idx<itercnt; idx++
    {
      fib=fib0+fib1;
```

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SCHEME OF EVALUATION

Sem : VIII	Subject : Real Time operating systems	Sub Code : 10EC 842	Date : 19/05/2018

Q. No.	Bit	Description	Marks	CO's	RBT LEVEL

```
while (idx < 10 ; seqcnt)
    {
     fibo = fib1 ; fib1 = fib ; fib = fibo + fib1 ;
     idx++ ;
     }
    }
}
```

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