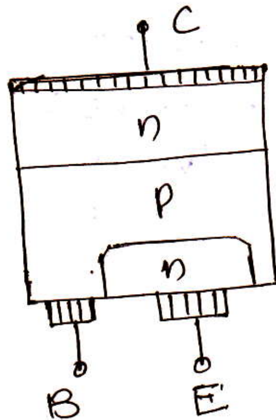
Power Transistor

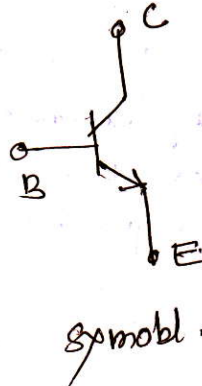
1. Power BJT :-

Power BJT's are available in both form i.e. npn & p.n.p forms. But n-pn types are relatively used for high current, high voltage applications because higher mobility of electronics. Up to 1976, BJTs were more dominating as compared to SCRs & GTO's. They were ideal switching devices for power applications. With the introduction of MOSFET in 1976, BJT's have been replaced by MOSFETs in almost all medium power applications ($\leq 500V$). And with the introduction of IGBT in 1983 & MCT's in 1988, they replaced BJTs in high power applications. But till for low power applications BJT's are used. Now a days some of the companies like motorola, Philips & Fairchild semiconductors are supplying BJTs.

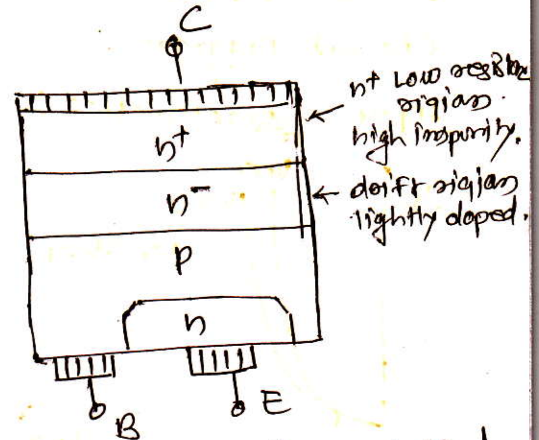
Structure of BJT



Double diffusion vertical structure of BJT



symbol.



Triple diffusion vertical structure of BJT.

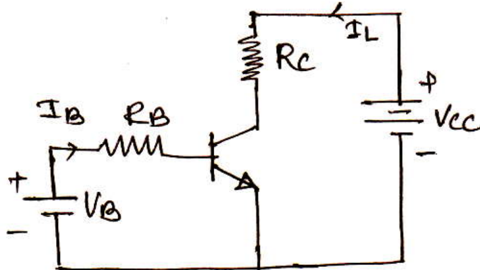
Structure of BJT is as shown in above fig. The structure is vertical oriented. This type of structure is most prefered because it has more cross-sectional area. It will provide more current handling capacity, on state resistance decreases. Also thermal of transistor decreases, it improves cooling of transistor.

The double diffusion of n layer, the structure is suitable for low voltage application. The triple n diffusion structure is suitable for high voltage application. In the triple n diffusion structure, highly doped n^+ region provide low resistance, and lightly doped n^- region called drift region. The thickness of drift region determines the breakdown voltage of transistor. Thickness of drift region increases with voltage rating & this tends to increase ON-state voltage drop. Emitter region is heavily doped, base region is lightly doped & doping concentration of collector is same as emitter.

Steady state characteristics :-

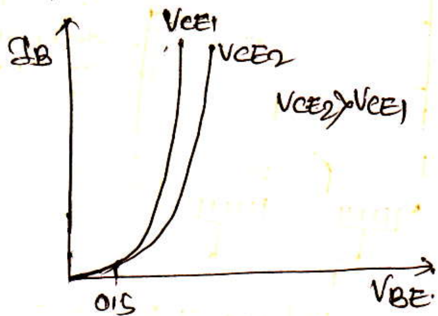
Out of C.B., C.C. & CE configurations, CE configuration is used for switching application. Typical I/p, O/p & Transfer characteristics for CE configuration is as shown in fig. below.

Experimental set up to find I/p, O/p and transfer characteristics is as shown in fig.



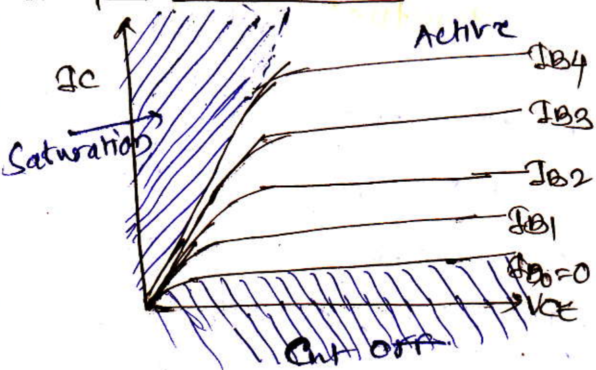
Circuit Diagram.

Input characteristics :-



Input characteristics is between I/p variables I_B versus V_{BE} for different values of V_{CE}. It is simple pn junction characteristics.

Output characteristics :-



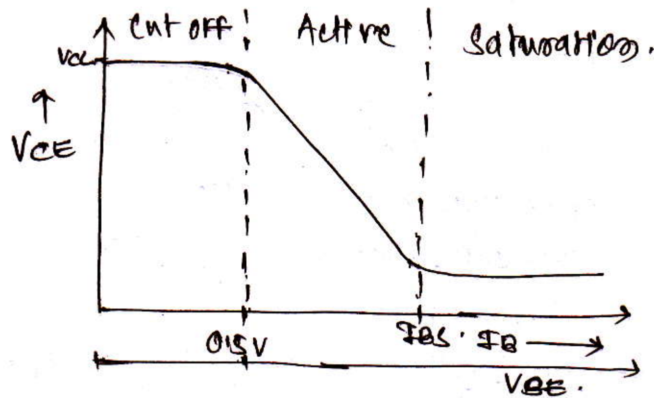
Output characteristics is between O/p variables I_C versus V_{CE} for different base currents.

When $I_B = 0$ the device is in cut off region.

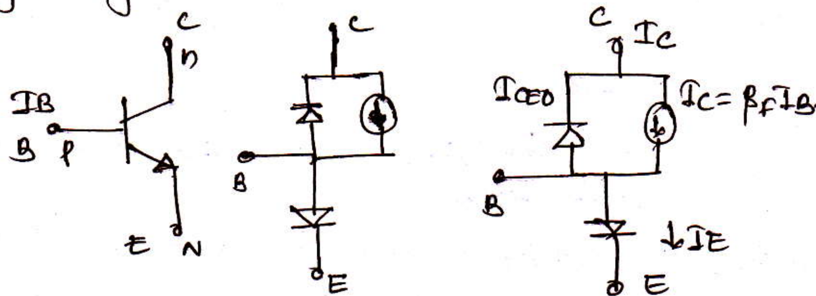
When $I_B < I_{BS}$ the device is active region, $I_C = \beta I_B$ - CB - RB, BE - FB

When $I_B > I_{BS}$ the device is in saturation. Both CB & BE Junⁿ are forward biased.

Transfer characteristics :-



Large signal model :- (NPN Transistor).



~~Emitt~~ Small signal model of npn transistor is as shown in above fig. It has two diode i.e. Base to collector & Base to emitter junction diodes. ICEO is leakage current. collector current is given by

$$I_C = \beta_F I_B .$$

β_F = current amplification factor.

$$= \frac{I_C}{I_B}.$$

But collector current has one more part i.e ICEO.

$$\therefore I_C = I_{CEO} + \beta_F I_B .$$

But $\quad I_E = I_{CEO} + \beta_F I_B + I_B$

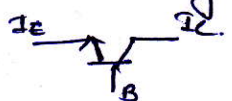
$$I_E = I_{CEO} + (\beta_F + 1) I_B .$$

$$I_E \cong (\beta_F + 1) I_B \qquad \because I_{CEO} \cong 0 .$$

$$I_E \cong (\beta_F + 1) \frac{I_C}{\beta_F}$$

$$\therefore I_E = \frac{(\beta_F + 1)}{\beta_F} I_C = \left(1 + \frac{1}{\beta_F}\right) I_C .$$

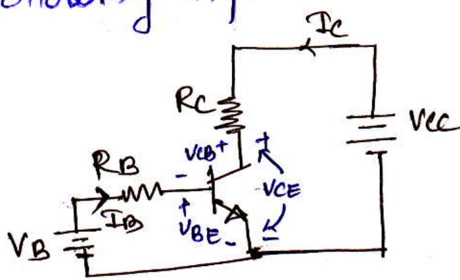
α_F = current amplification factor in CB configuration



$$\boxed{\alpha_F = \frac{I_C}{I_E} = \frac{\beta_F}{\beta_F + 1}}$$

& $\boxed{\beta_F = \frac{\alpha_F}{1 - \alpha_F}.}$

Consider transistor operated as switch as shown in following fig.



Apply KVL to base loop.

$$V_B - I_B R_B - V_{BE} = 0.$$

$$\therefore I_B = \frac{V_B - V_{BE}}{R_B} \quad --- (1)$$

Now apply KVL to collector loop.

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$\therefore V_{CE} = V_{CC} - I_C R_C$$

$$= V_{CC} - \beta_F I_B R_C \qquad \because I_C = \beta_F I_B$$

$$= V_{CC} - \beta_F R_C \left(\frac{V_B - V_{BE}}{R_B}\right) \quad -- \text{from eq}^n (1)$$

But $V_{CE} = V_{CB} + V_{BE}$.

$$\therefore V_{CB} = V_{CE} - V_{BE} \quad ---- (2)$$

From eq^n (2) whenever $V_{CE} \geq V_{BE}$, CB junction is reverse biased & transistor operates in active region.

When $V_{CE} < V_{BE}$, CB junction becomes forward biased & transistor operates in saturation region. Once transistor goes V_{CE} automatically reduces to $V_{CE(sat)}$ level. Further if the V_{BE} increases the I_B increases but I_C does not increases.

$\therefore$ Maximum collector current (I_{CM}) in active region is when $V_{CB} = 0$ i.e. $V_{BE} = V_{CE}$

$$\therefore I_{CM} = \frac{V_{CC} - V_{CE}}{R_C} = \frac{V_{CC} - V_{BE}}{R_C} \quad —— (3).$$

$\therefore$ Corresponding value of maximum base current is

$$I_{BM} = I_{CM}/\beta_F \quad —— (4)$$

If base current increased above I_{BM}, base current will increase but collector current (I_C) will slightly increases & V_{CE} decreases below V_{BE}, making CB junction forward biased with $V_{BC} = 0.4$ to 0.5 V then transistor operates into saturation.

Transistor saturation condition is defined as increase in base current will not increase collector current significantly.

In the saturation collector current I_C remains almost constant. If we know $V_{CE(sat)}$ the collector saturation current I_{CS} is given by

$$I_{CS} = \frac{V_{CC} - V_{CE(sat)}}{R_C}$$

$\therefore$ Corresponding value of Base current I_{BS} is

$$I_{BS} = \frac{I_{CS}}{\beta_F}.$$

So to operate transistor as a switch, the base current (I_B) must be greater than I_{BS} saturating current.

The ratio of I_B to I_{BS} is called as overdrive factor

$$\therefore ODF = \frac{I_B}{I_{BS}} \quad \text{--- (6)}$$

The ratio of I_{cs} to I_B is called as β_{forced}.

$$\therefore \beta_{forced} = \frac{I_{cs}}{I_B} \quad \text{--- (7)}$$

Total power loss in the two junction is P_T given by

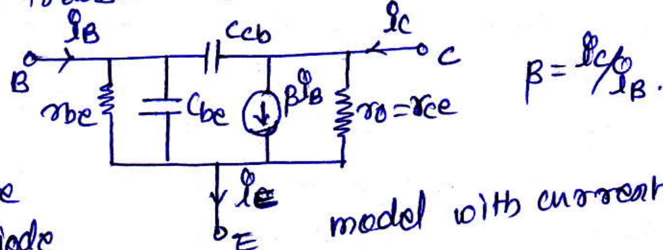
$$P_T = V_{BE} I_B + V_{CE} I_C \quad \text{--- (8)}$$

V_{BE} increases I_B increases but V_{CE} cant reduces further i.e. ODF increases V_{CE} can't reduce, because it saturates towards minimum level. As V_{BE} increases, it increases I_B & increases power loss in BE junction.

Switching characteristics :-

Transistor has 2 diodes i.e. base to emitter diode & base to collector diode. These diodes has internal capacitance a depletion capacitance & a diffusion capacitance, and in reverse biased diode has only depletion capacitance. Under steady state condition it will not have role. But in transient condition or in switching it plays important role. They affects the turn ON & turn off behaviour of transistor the transient model of transistor is as shown below.

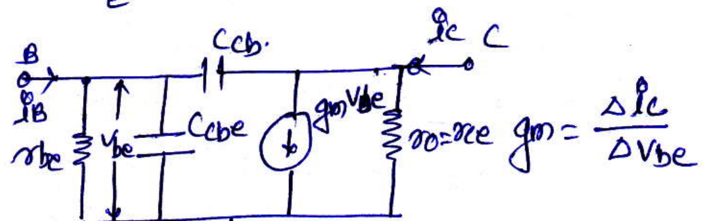
Transient Model :-



$\beta = I_C / I_B$.

model with current gain.

where
Cbe = capacitance between base to emitter junction diode
Ceb = capacitance of collector to base junction diode
rbe = resistance between base to emitter
rce = resistance between collector to base.

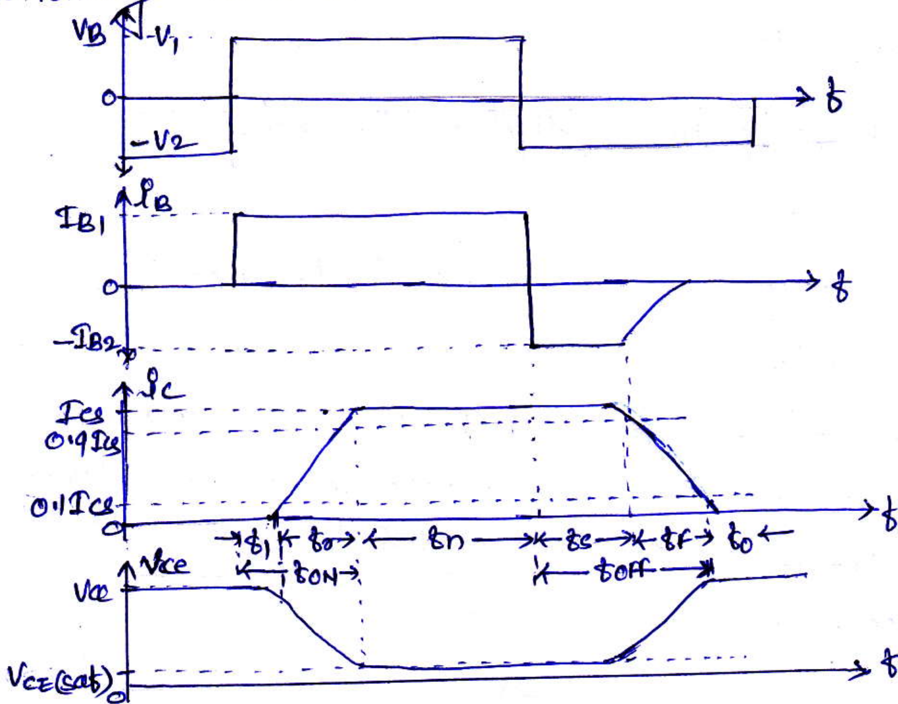


$g_m = \frac{\Delta I_c}{\Delta V_{be}}$

model with transconductance.

Ccb affects on the input capacitance significantly than output capacitance. Due to these capacitances transistor does not conduct instantly. This is shown in figure below.

Switching characteristics of BJT :-



As input base voltage rises from 0 to V_1 at the same time base current rises from 0 to I_{B1} but the collector current does not responds immediately. There is delay known as 't_d' = delay time before any collector current flows. This delay is required to charge the capacitance between base to emitter junction, to forward bias the junction, the V_{be} must be approximately 0.7 V. After this delay the collector current increases to the steady state value I_{cs}. This time is called as rise time. So on time of transistor is addition of these two time periods.

Delay time (t_d): Time required to charge input capacitance upto cut in voltage or to forward biase base to emitter diode.

Rise time (t_r): Time required to rise the collector current from 10% of collector saturation current to 90%.

Turn ON time (t_{ON}) ! $\quad t_{ON} = t_d + t_r$.

Base current is always more, its required to saturate the transistor. Once the transistor goes into saturation the excess charges are stored into base region. If the over drive factor (ODF) is more then more charges stored into base region. This extra charge is called saturating charge, & it is proportional to the excess base drive & corresponding current I_e.

Corresponding excess current I_e = Excess base current − Minimum saturating base current

$$= ODF \cdot I_{BS} - I_{BS}$$

$$I_e = (ODF - 1) I_{BS}.$$

saturating charge is given by

$Q_S = \tau_S I_C$ where τ_S = storage time constant of transistor.

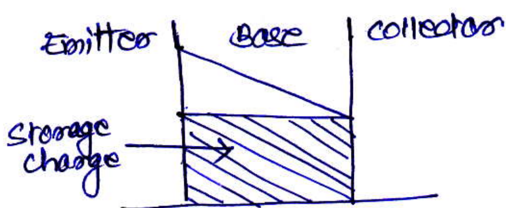
$= \tau_S I_{BS} (ODF-1)$

Now when input voltage reversed i.e. from V_1 to $-V_2$ & therefore at the same time base current is reversed. But the collector current doesnot changes immediately. It requires some time called storage time t_s. This time is required to remove saturating charge stored at base region. Storage charge will provide V_{BE} positive 0.7 V. Due to -ve I_B the excess charge stored at base will be removed. Once extra charge is removed, the base to emitter junction is reverse biased & base current starts to fall to zero. At the same time collector current also starts to fall to zero, & this time is called fall time 't_f'.

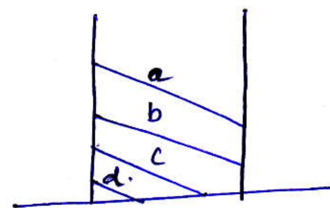
<u>Storage time (t_s)</u>: It is the time required to remove excess charge stored in base region & reverse base current decreasing.

<u>Fall time (t_F)</u>: It is time required to fall the collector saturating current from 90% of saturation current to the 10% of saturating current.

<u>Turn off time (t_{off})</u>: $t_{off} = t_s + t_F$.



ⓐ charge storage in base



ⓑ charge profile during turn off.

charge storage in saturated bipolar transistors.

Power MOSFETs

It is voltage controlled, 3 terminal, majority carrier device. It requires very small input current, switching speed is very high & its switching time is very small of the order of nanoseconds. It has increasing application in low power high frequency applications. It do not have the problem of second breakdown, but it requires special care in handling of electrostatic ~~charge~~ discharge. It is very difficult to protect them under short-circuit fault conditions.

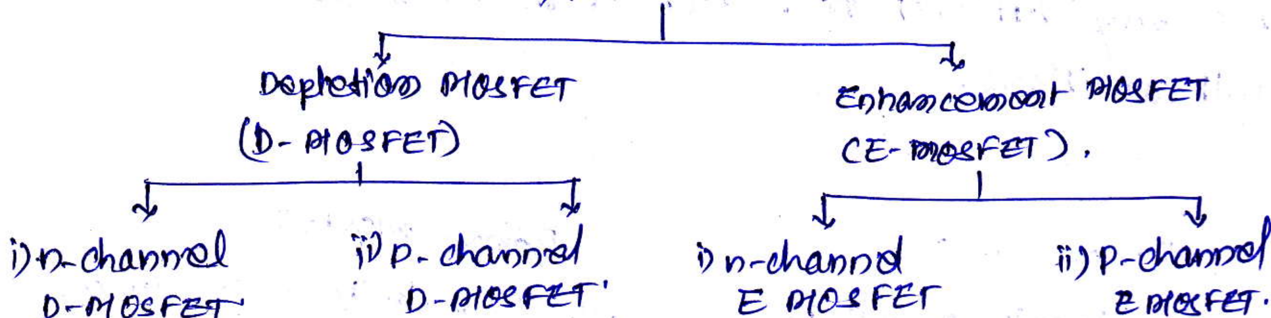
Comparision between Power BJT & Power MOSFET

Power BJT	Power MOSFET
1. It is minority as well as majority carrier device.	1. It is majority carrier device.
2. It is current controlled device	2. It is voltage controlled device.
3. It has negative temp. coefficient.	3. It has positive temp. coefficient.
4. Operating freqⁿ is less	4. Operating freqⁿ is High
5. Second breakdown can take place	5. No possibility of second breakdown.
6. Peak current capability is less than MOSFET	6. Peak current capability is more than BJT.
7. BJTs are less sensitive to voltage spikes	7. MOSFETs are more sensitive to voltage spikes.
8. On state voltage drop is less than MOSFET & hence on state power loss is less than MOSFET	8. The on state voltage drop is more than BJT & hence on state power loss is more than BJT.
9. Conduction losses are less than MOSFET	9. Conduction losses are more than BJT.
10. Switching losses are more than MOSFET	10. Switching losses are less than BJT.
11. More energy efficient at low frequency.	11. More energy efficient at high frequency.
12. I/p impedance is less as that of MOSFET	12. I/p impedance is more than BJT.
13. Parall operation is complex.	13. Parallel operation is simple.

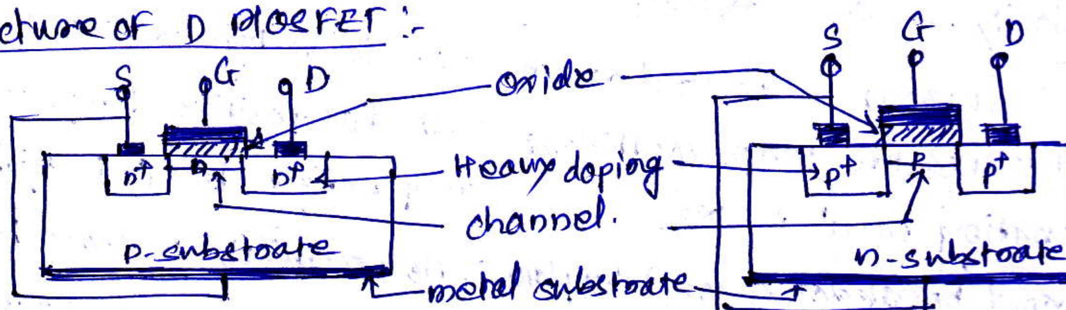
(14) I/p capacitance is less	(14) I/p capacitance is more.
(15) I/p current in mA is more.	(15) I/p current is in nanoamp. is very less.
(16) No electrostatic discharge problem.	(16) There is electrostatic discharge problem.

Commercially available power MOSFETS are as IRF 540, IRF 150, IRF 250, IRF 510, IRF 840, 244, 248 etc.

Structure of Power MOSFET :-

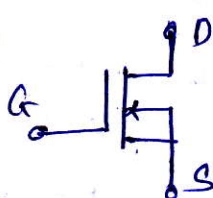


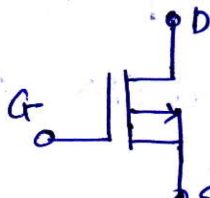
Structure of D MOSFET :-



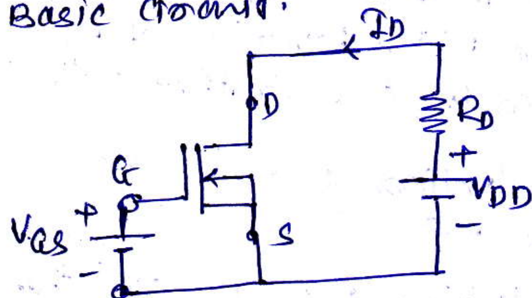
n-channel D MOSFET   p channel D-MOSFET

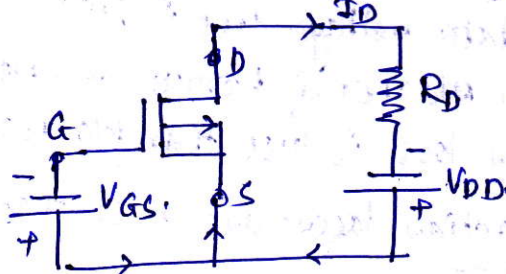
Symbol.





Basic circuit.

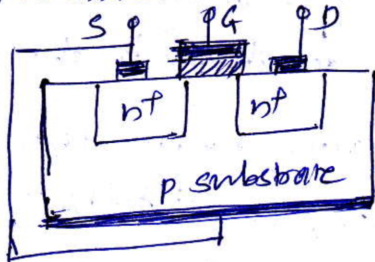




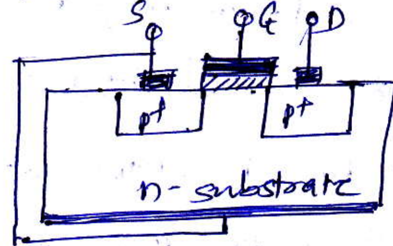
Depletion mode mode MOSFET's are normally on MOSFETs at $V_g = 0$ drain current exists. If -ve voltage is applied at gate to sources of n-channel MOSFET causes some electrons in n channel are repelled & depletion region is created below oxide layer, results channel narrower, offering more value of R_{DS}. The value of V_{GS} is made enough, the channel becomes completely depleted (off) i.e offering high value of R_{DS} & $I_D = 0$, That value of V_{GS} is call pinch off voltage (V_P). For p channel D-MOSFET polarities of applied voltage are reversed.

Structure of E-MOSFET

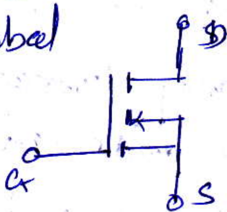
N channel E MOSFET

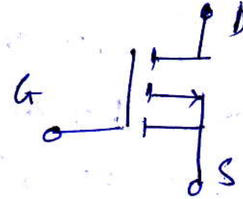


P channel MOSFET

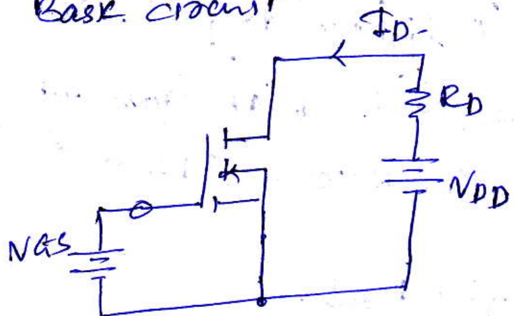


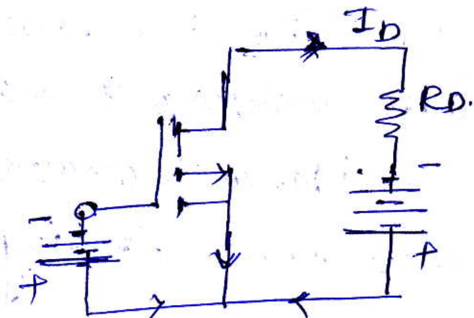
Symbol





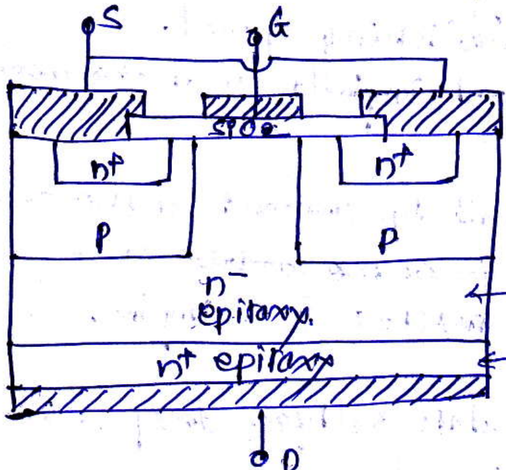
Basic circuit



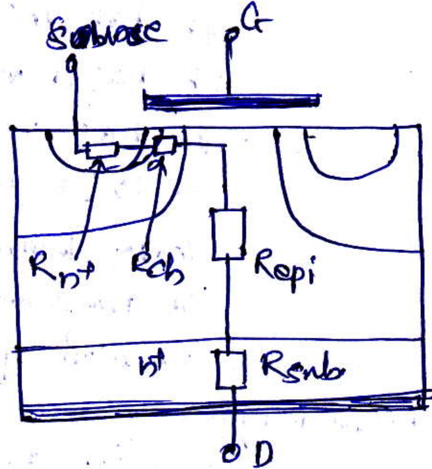


E MOSFETS are normally off MOSFET, to make them on; V_{GS} must be +ve for n channel E MOSFET & V_{GS} must be -ve for n-channel E MOSFET. When +ve voltage at gate to source of n-channel MOSFET is applied electrons from p-substrate are attracted under the gate region. When V_{GS} is equal or greater than threshold voltage, efficient number of electrons are accumulated which forms a virtual channel & current flow starts from drain to source. The polarities of V_{GS} & V_{DS} are reversed in case of p-channel E-MOSFET.

V-MOSFET structure:-



Cross section of V-MOSFET



On state resistance of V MOSFET

Buffer layer – separates drain metal & depletion region.
even out voltage stress at drain
on state resistance decreases & hence forward voltage drop.

As depletion MOSFETs are remains ON at $V_{GS}=0$, hence they are not used for power application. E MOSFETs are OFF at $V_{GS}=0$, hence they are used in power application. The cross section of vertical MOSFET (V-MOSFET) as shown in above fig.

It has n^+ layer called buffer layer. Buffer layer separates metal drain & depletion layer. It distributes voltage stress evenly at drain. It also decrease on state resistance & hence on state voltage drop decreases. Structure has n^- epitaxy layer called drift layer & is responsible for power handling capacity. But its on state resistance is more as it is lightly dopped. On state resistance increases with increases in drift layer but increases power handling capacity. On state resistance is given by

$$R_{DON} = R_{n^+} + R_{ch} + R_{epi} + R_{sub}.$$

When sufficient positive gate voltage is applied w.r.t. source, as the effect electrons from p-layer, n^+ layer attracts under the gate oxide, this forms channel, which allows the current to flow from drain to source.

Advantages of MOSFET :-

- It requires very low gate energy
- It has less switching loss.
- It has a very fast switching speed.
- It has very high input impedance of the order of $10^9\Omega$ to $10^{11}\Omega$.
- Gate draws very small i/p current of the order of nanoamperes. ~~Ia is of the order of 10~~
- Parallel operation of MOSFET is simple.

Disadvantages :-

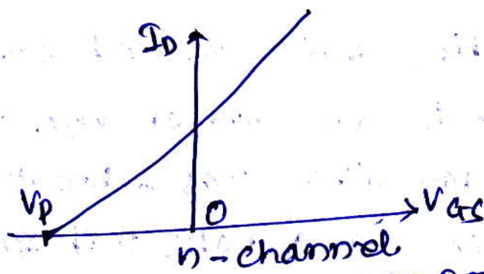
- High forward on state voltage drop & hence more on state voltage drop.
- They are more sensitive voltage spikes.
- They have electrostatic discharge problem.

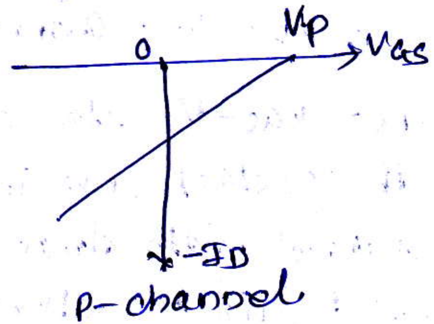
Steady-state Characteristics :-

MOSFET is voltage controlled device. It has very high I/p impedance. The gate draws very small leakage current of the order of nano-amp. The current gain is I_D/I_G, is typically of the order of 10^9. But transconductance is important parameter not current gain. The transconductance is the ratio of drain current to gate to source voltage. It is given by gm.

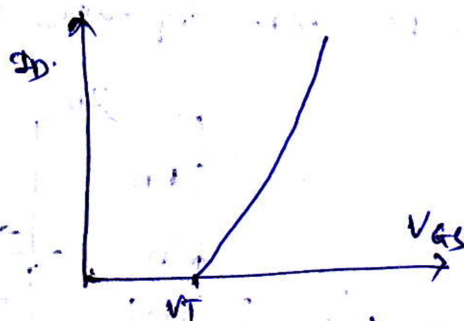
$$g_m = \text{transconductance} = \frac{\Delta I_D}{\Delta V_{GS}} \Big/ V_{DS} = \text{constant}.$$

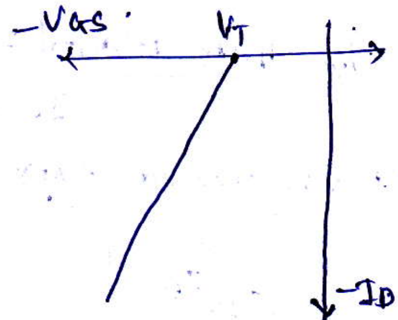
Transfer Characteristics :-





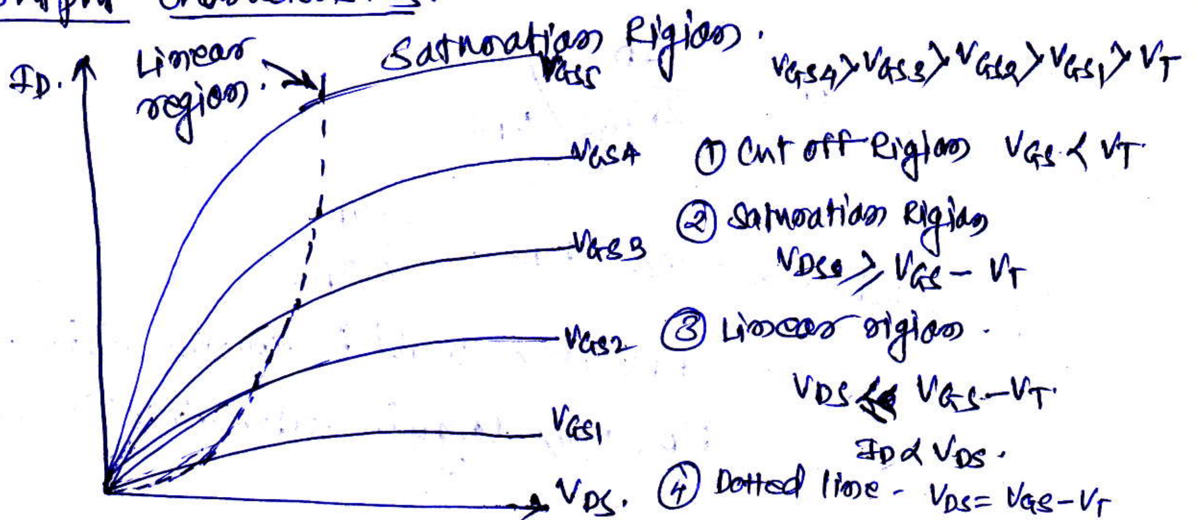
(a) Depletion type - MOSFET





(b) Enhancement type MOSFET

Output Characteristics :-



1) Cut off region :- In this region $V_{GS} < V_T$. Channel is not formed, & hence no I_D.

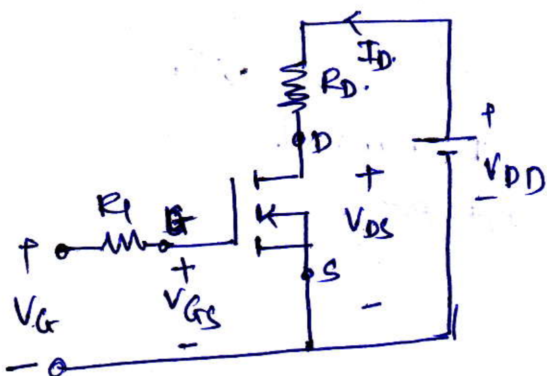
2) Linear region :- In this region $V_{GS} > V_T$ & where $V_{DS} \leq V_{GS} - V_T$. In this region drain current I_D varies in proportional to the drain to source voltage. Power MOSFET are operated in linear region for switching action.

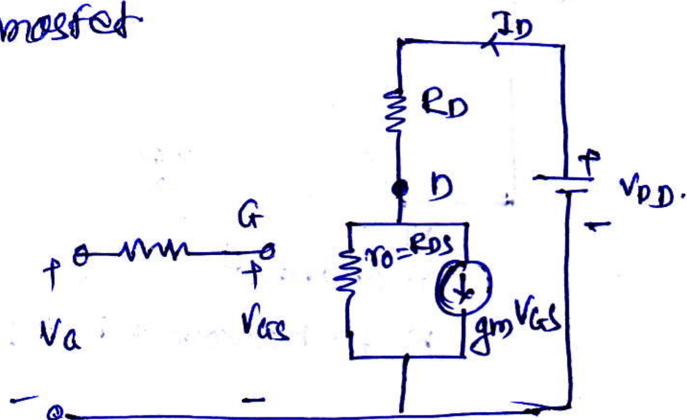
3) Saturation region :- (Pinch off region).

In this region $V_{GS} > V_T$ & where $V_{DS} \geq V_{GS} - V_T$. Channel saturates (or pinch off's at) at $V_{DS} = V_{GS} - V_T$. In saturation drain current remains almost constant for increase in any value of V_{DS}. In this channel width almost const for given V_{GS} & hence channel is said to saturates. It should note that saturation in transistor & in MOSFET is different.

Steady state Model :-

It is same for both depletion type and Enhancement type mosfet





$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \Big/ V_{DS}$$

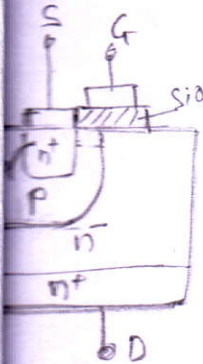
$$\text{O/p resistance} = r_0 = R_{DS} = \frac{\Delta V_{DS}}{\Delta I_D}.$$

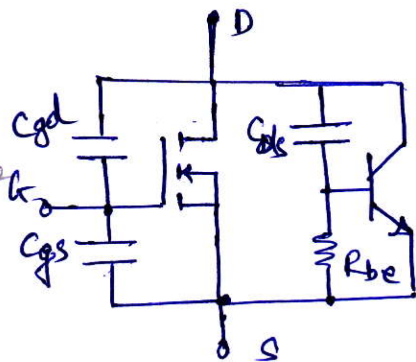
R_{DS} very small in linear region i.e $m\Omega$

R_{DS} very large in saturation region i.e. $M\Omega$.

Switching Characteristics :-

Parasitic Model of E MOSFET :-





E MOSFET has diffⁿ parasitic capacitance

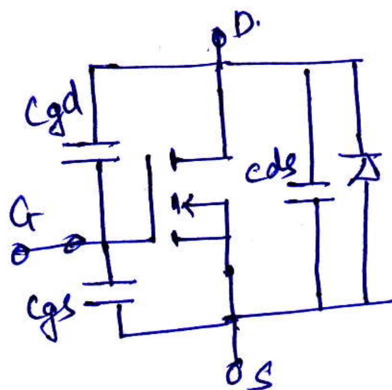
Cgd = cap- betⁿ gate to drain

Cgs = cap- betⁿ gate to source

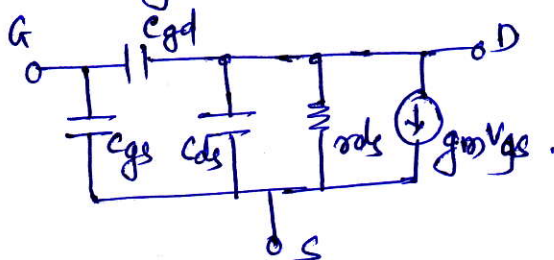
When no gate voltage MOSFET is like two back to back diode or simply a transistor & hence is shown parallel to MOSFET

Cds = drain to source capacitance.

Rbe = Resistance betⁿ base to emitter of transistor. But it is internally shorted by putting metal. Hence Rbe is very small. ∴ The equivalent model shows, As rbe shorted, base to emitter diode is shorted & hence only one diode.



Switching Model of MOSFET :-



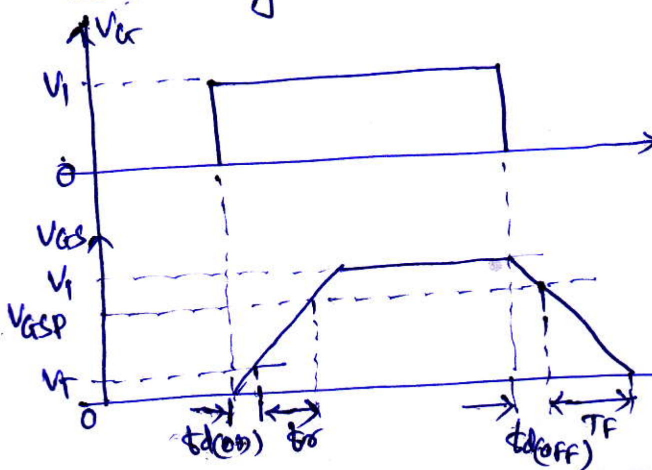
① The turn on delay td(on) :- It is the time required to charge the I/p capacitance to threshold voltage level.

② The rise time tr - It is the gate-charging time from threshold level to pinch off voltage level Vgsp. In which MOSFET is linear region. V₁ = is the over drive gate voltage falls MOSFET into saturation region or pinch off region.

③ The turn off time td(off) :- It is the time required for the I/p capacitance to discharge from the overdrive voltage V₁ to pinch off level voltage Vgsp.

④ The fall time tf :- It is the time required for I/p capacitance to discharge from the pinch off level voltage Vgsp to threshold voltage V_T.

Switching Waveforms

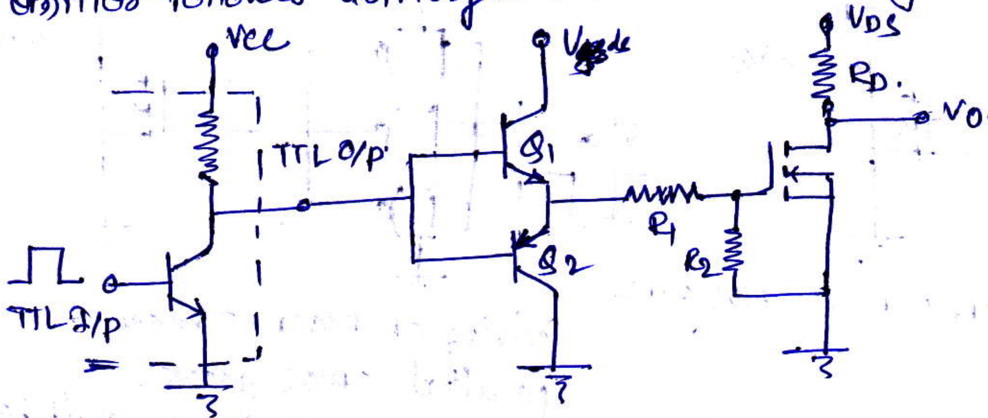


Gate Drive Circuits :-

MOSFET does not requires power to drive gate, but it is required to transfer charge to the gate terminal to turn ON. & from the terminal to turn off the MOSFET. At the I/p of gate, it has capacitances C_{gd} & C_{gs}. It is necessary to charge the capacitances & to turn ON & discharge the capacitance to Turn OFF. Hence we can say gate is electrically isolated from drain & source i.e it has high I/p impedance & low leakage current from gate to source. There are different MOSFET driving circuits are as follows.

1. Driving of MOSFET from TTL :-

We can drive the MOSFET by using TTL logic. But performance of MOSFET will not be optimum, because transistor requires some time to go into saturation. so to improve switching performance, rise time & fall time must be less. For this use buffer circuit. which will provide fast current sourcing & sinking to the gate of MOSFET. Such a simple complimentory emitter follower driving circuit shown in fig. below.



Q_1 & Q_2 have high gain.

$$I_{charge} = \frac{C_{gs} \cdot V_{DS}}{t_r} \quad \& \quad I_{discharge} = \frac{C_{oss} V_{DS}}{t_f}$$

$$C_{gs} = C_{iss} - C_{oss}$$

where

C_{gs} = gate to source capacitance in pF

C_{iss} = I/p capacitance in pF

C_{oss} = reverse transfer capacitance in pF

t_r = I/p pulse rise time in ns.

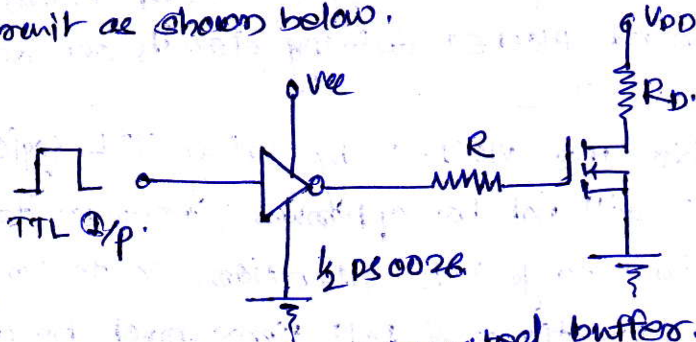
t_f = I fall time in nsec.

V_{ds} = drain to source ~~power~~ voltage in V.
V_{gs} = gate to source voltage in V.
Power dissipation across buffer transistor is given by

$$P = V_{CE}\, I_C\, t_r\, f$$

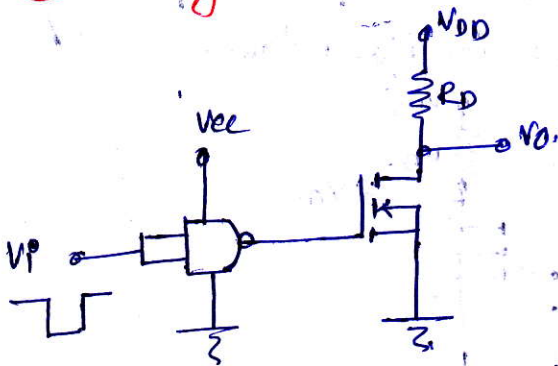
where V_{CE} = buffer transistor saturation voltage in V.
I_C = " " collector current in A
f = switching frequency in KHz

Now a days it is not necessary to design these discrete circuit, because the buffer IC's are available to drive the MOSFET eg. DS0026. Such circuit as shown below.

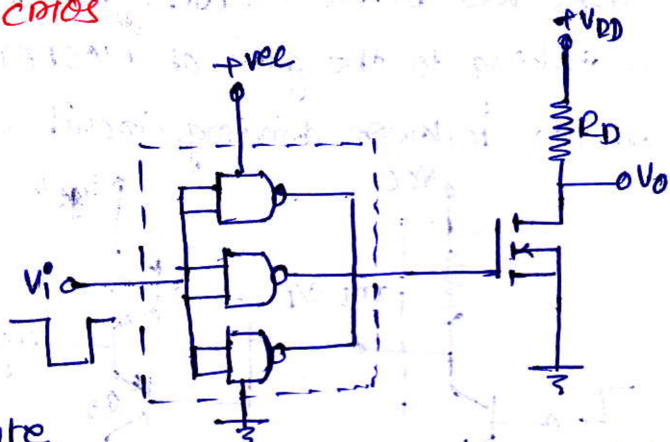


High current integrated buffer.

② Driving the MOSFET from CMOS



Driving of MOSFET from CMOS gate

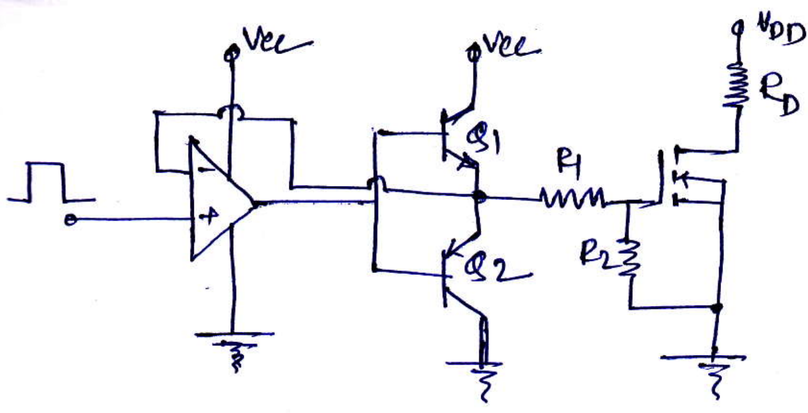


Driving of MOSFET from paralled CMOS gates.

single CMOS gate can drive MOSFET. But to improve switching time ~~more~~ less than one gate can be made by parallelling more than one gate. It will increase driving current to drive I/p capacitance.

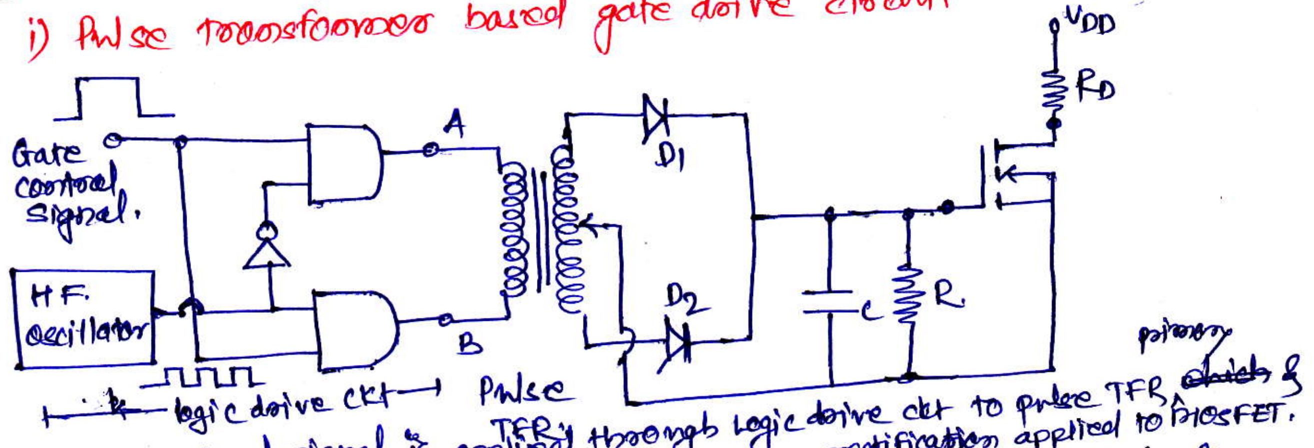
③ Driving MOSFET from Linear Circuits :-

We can use op-amp for driving for driving the power MOSFET. Op-amp has more current delivering capacity. But one drawback of op-amp is its slow rate i.e switching freq^n less than @ 25 KHz. In order to improve switching freq^n op-amp o/p is given to complimentary emitter follower stage. Typical op-amp driving circuit as shown below.



④ Isolation of gate & base drive circuits :-

i) Pulse transformer based gate drive circuit



Gate control signal is applied through logic drive ckt to pulse TFR primary & o/p taken from secondary, after rectification applied to MOSFET.

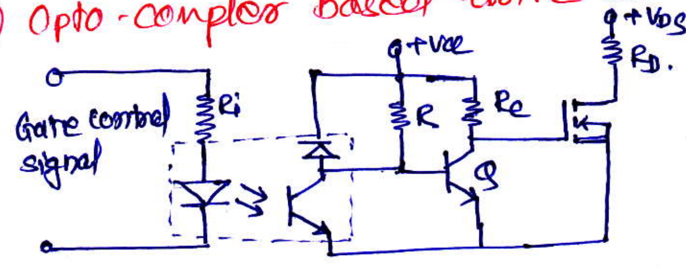
Advantages

1. Isolation between power circuit & driving circuit is obtained by pulse TFR
2. It can drive MOSFETS are at different voltage levels. i.e. MOSFET may be at ground level or at any other voltage level.
3. The size of TFR reduces with switching freq^n.
4. It will not require separate power supply.

Disadvantages

1. If driving current required is more then it use is limited
2. Switching performance depends on diodes. In case of high freq^n schottky diodes may used.

② Opto-coupler based drive circuit :-

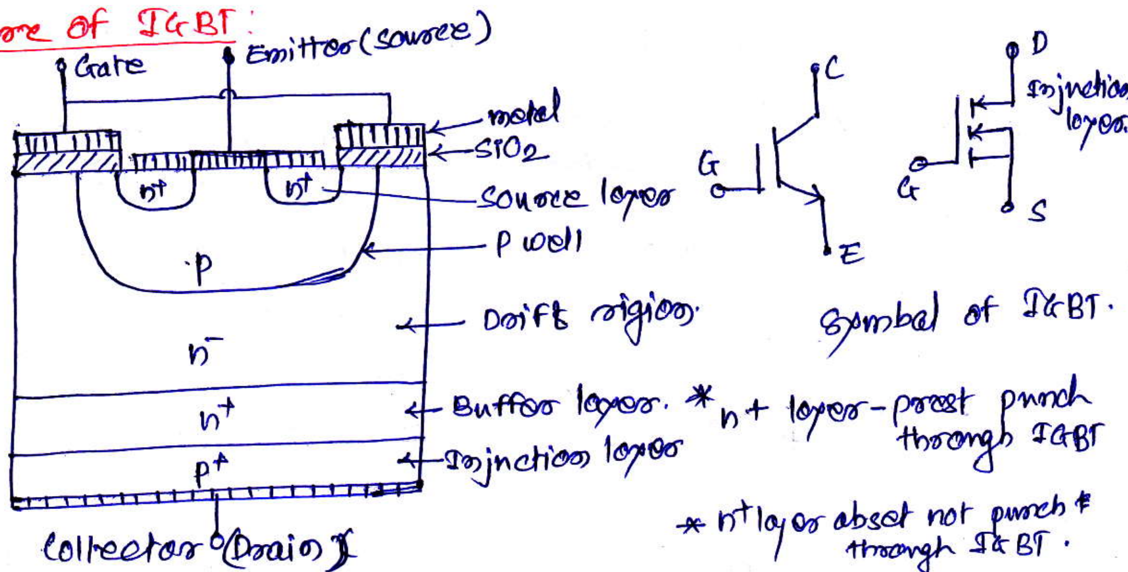


Optocoupler combines an infrared LED & photo transistor. Gate control signal is applied to ILED & o/p is taken from photo transistor. O/p current of phototransistor is not sufficient drive the MOSFET, so additional transistor is need for amplification. This is very simple ckt which provides optical coupling. This method of isolation requires addition amplication.

IGBT

An Insulated gate bipolar transistor (IGBT) was invented in 1988 by B. Jayant Baliga (Indian electrical engineer, B.Tech from IIT Madras &, MS & PHD from RPI (Rensselaer Polytechnic Institute) New York). It combines the advantages of BJTs and MOSFETs. MOSFET has advantages that its input impedance high, voltage controlled device, more operating frequency & no second break-down problem. Whereas the transistor has excellent on state characteristics i.e. low on state resistance. An IGBT has all these advantages combined together. It's operating speed is high but less than MOSFET. But it handles more power as compared to both transistor & MOSFET. IGBT can be driven by using same gate driving circuit for MOSFET.

Structure of IGBT:



Cross section of n-channel vertical structure of IGBT

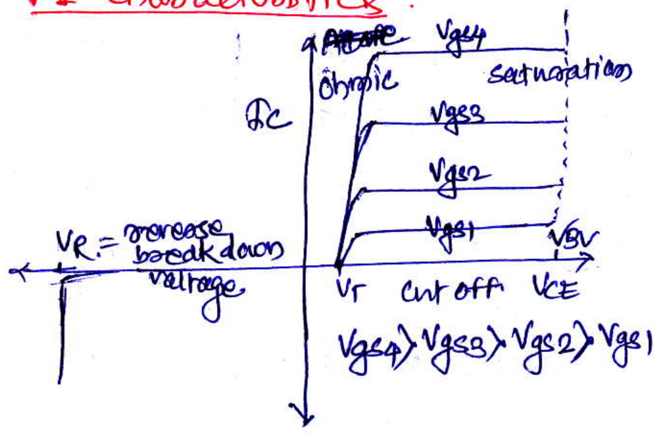
IGBT also has vertical structure as it has advantage of less on state resistance, increased cross-sectional area & more power handling capacity. Above fig. shows the structure of IGBT, it is same as power MOSFET with extra p^+ layer called injection layer. This injection layer forms collector / Drain of IGBT.

The n^+ buffer layer is not important in the operation of IGBT. But depending upon n^+ layer there are two types of IGBT.

1. Punch Through IGBT (PT IGBT) - It has buffer layer. It handles more power in forward direction but less power in reverse direction. hence it is called as Asymmetric IGBT.

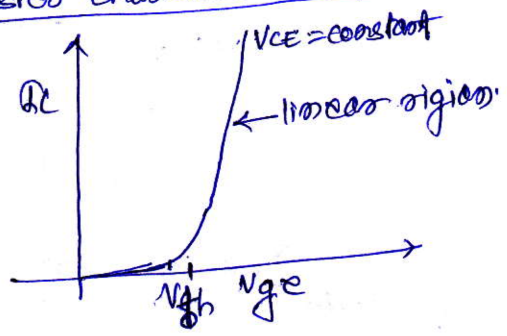
2. Non Punch Through IGBT (NPT IGBT) :- It is without n^+ buffer layer. It handles power in both forward & reverse direction, hence it is called as symmetric IGBT.

VI characteristics :-



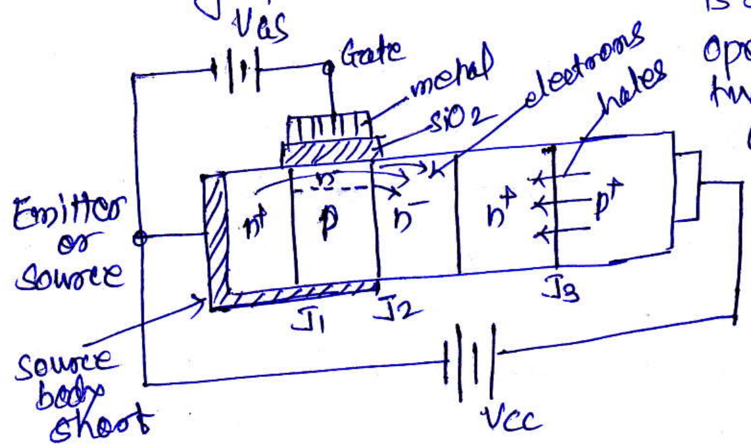
Output characteristics is as shown in fig. This is like same as MOSFET. When $V_{gs} < V_T$ IGBT in cut off region. When $V_{gs} > V_T$ IGBT falls into linear region or ohmic region, where current Ic increases with VCE. Rate of increase of current is more as that of MOSFET, slope is more steeper. Still increase in V_{ge} device fall into saturation as channel saturates. Still increase in V_{ge}, when $V_{ge} = V_{BV}$, is forward breakdown voltage, it goes into avalanche breakdown. At this point current through device is very & it may damage the device.

Transfer characteristics :-



Transfer characteristics is as shown in fig., it is same as MOSFET. When $V_{gs} = V_{th}$ i.e threshold voltage, an inversion layer forms under gate region & current starts increasing.

Operating principle :



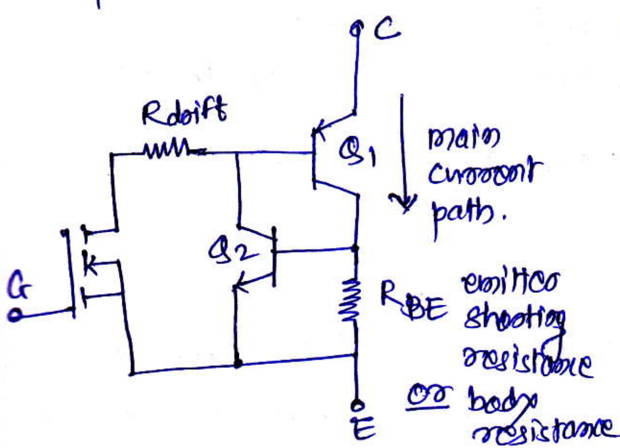
The operating principle of IGBT is same as that of MOSFET. The operation can be divided into two parts :- ① Creation of inversion layer

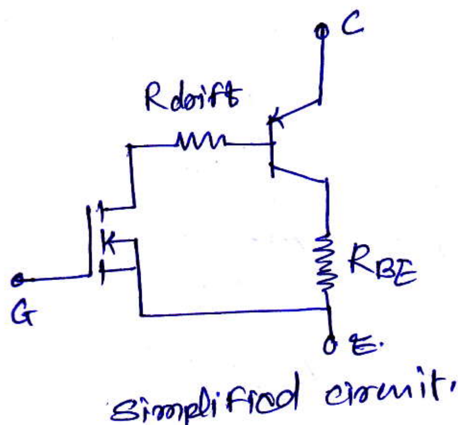
② Conductive modulation

Due to the application of $V_{gs} > V_{th}$, n type inversion layer formed in p region body. Thus channel is formed for conduction of current $n^+ n\, n^-$. Conductivity modulation of drift layer reduces on state resistance & hence on state power loss is less. Due to application of

forward voltage between collector to emitter, the junction J_3 forward biases. Due to creation of inversion layer electrons from source are injected into n^- drift layer via n^+, n, n^- channel. As junction J_3 is forward biased it injects holes in the n^+ buffer layer. The electrons from n^- drift layer creates a space charge, which attracts holes. Thus double injection takes place & flow of electron takes place.

Equivalent Circuit :-

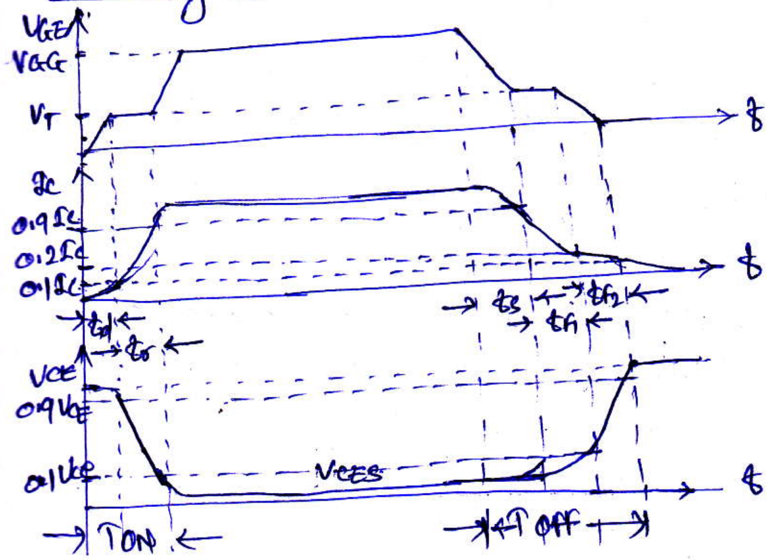




simplified circuit.

An equivalent model of IGBT consists of PNP & NPN transistor pair, which represents four layers of parasitic thyristor structure with MOSFET shunting npn transistor. This gives the either high current mode or zero current mode device. Emitter of Q_1 termed as collector of IGBT, emitter of Q_2 termed as emitter of IGBT. The main current is carried out by Q_1 PNP transistor. Input side of IGBT look like MOSFET, hence MOSFET is added on in equivalent circuit. As drift layer is lightly dopped, resistance of IGBT depends upon length of drift layer.

Switching characteristics of IGBT:-



If we observe the chart the turn ON time is less & turn off time is more. The turn ON time is same as MOSFET or even less than it. But during turn off there are two distinct time intervals t_{f1} & t_{f2}. This tail current limits the use of IGBT for fast switching. The turn off time is caused by the discharge time constant of gate capacitance and R_{GE}.

t_d = Turn ON delay time : Time required for the gate current to charge gate emitter capacitance up to threshold voltage level (V_T) i.e bring device in conduction. During this time V_{CE} drops to 0.9 V_{CE} & I_C increase to 0.1 I_C. I_C is steady state value of current I_{CS}.

t_r = Rise time : Time required for I_C to reach steady state value from. During this time V_{CE} drops from 0.9 V_{CE} to 0.1 V_{CE}.

t_{on} = Turn ON time = $t_d + t_r$.

t_s = storage time - Time required to fall the V_{GE} from steady state V_{GG} to V_T. During this time I_C fall to 0.9 I_C from steady state value.

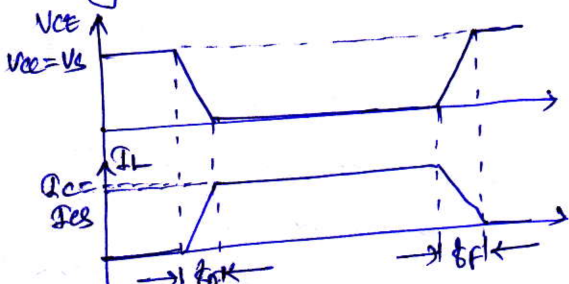
t_{f1} = Fall time t_1 - Time required to fall I_C from 0.9 I_C to 0.2 I_C.

t_{f2} = Fall time t_2 - Time required to fall I_C from 0.2 I_C to 0.1 I_C.

t_{off} = Turn off time : $t_{off} = t_s + t_{f1} + t_{f2}$

di/dt and dv/dt Limitations :-

If we assume the delay time and storage time of transistor negligible, & the waveforms of transistor switch is as shown in figure below.



Voltage & current waveforms

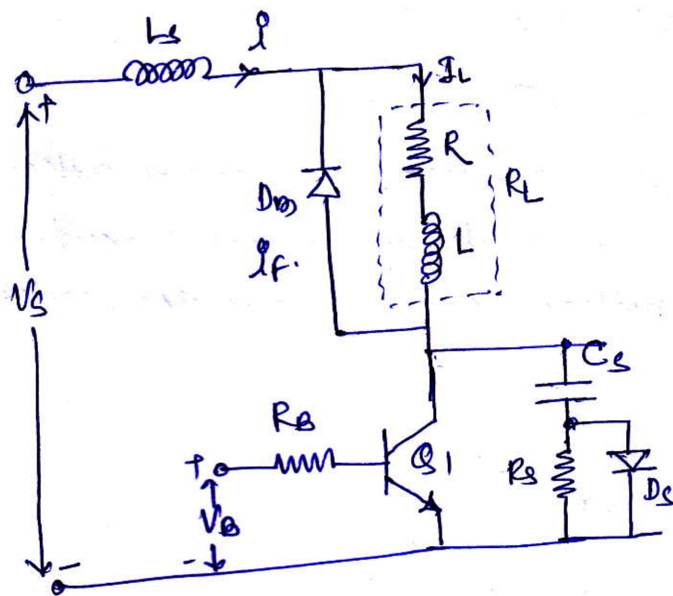
During turn on, the collector current rises & di/dt is

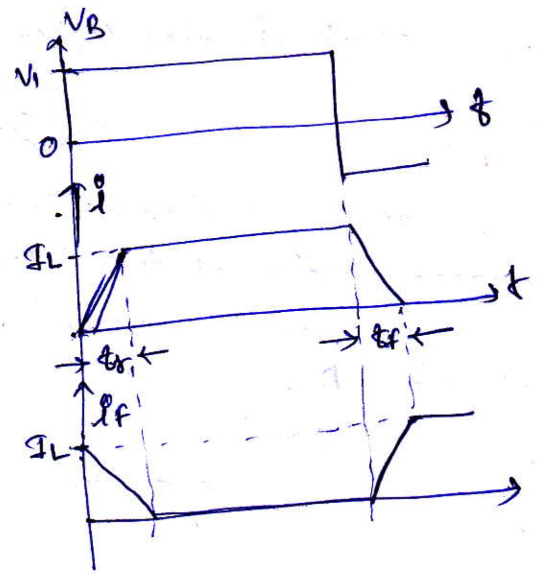
$$di/dt = I_{CS}/t_r. \quad \text{—(1)}$$

During turn off, the collector to emitter voltage V_{CE} rises & dv/dt is

$$dv/dt = V_s/t_f. \quad \text{—(2)}$$

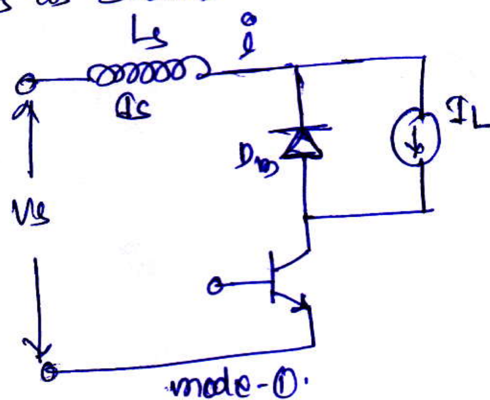
Condition for di/dt and dv/dt will be set by transistor, which is given by manufactures. At this rate of change of voltage and current increases above given limit it may damage the device. & so to protect the device against high di/dt & dv/dt protection circuit is need to limit this di/dt & dv/dt. A typical transistor switch with di/dt & dv/dt protection is as shown in figure below. The RC network across the transistor is known as snubber circuit or snubber, it will protect transistor against high dv/dt. The inductor L_s in series with transistor is used for di/dt protection, & it is some time called as a series snubber.





Protection circuits.

When transistor Q_1 turned on, the collector current rises & current through diode Dm decrease. The equivalent circuit during this as shown below as mode 1. & turn on di/dt is given as



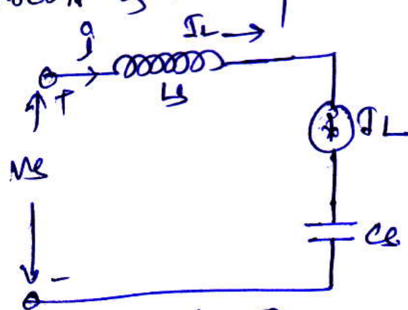
$$\frac{di}{dt} = \frac{V_s}{L_s} \quad \text{—— ③}$$

Equating eqn ① & ③

$$\frac{di}{dt} = \frac{V_s}{L_s} = \frac{I_L}{t_r}$$

$$\therefore L_s = \frac{V_s t_r}{I_L} \quad \text{—— ④}$$

During turn off, the capacitor Cs charges by the load current & the equivalent circuit is shown in mode-2. The capacitor voltage appears across transistor & the dv/dt is



$$\frac{dv}{dt} = \frac{I_L}{C_s} \quad \text{—— ⑤}$$

Equating eqn ⑤ & eqn ②

$$\frac{dv}{dt} = \frac{I_L}{C_s} = \frac{V_s}{t_f}$$

$$\therefore C_s = \frac{I_L t_f}{V_s} \quad \text{—— ⑥}$$

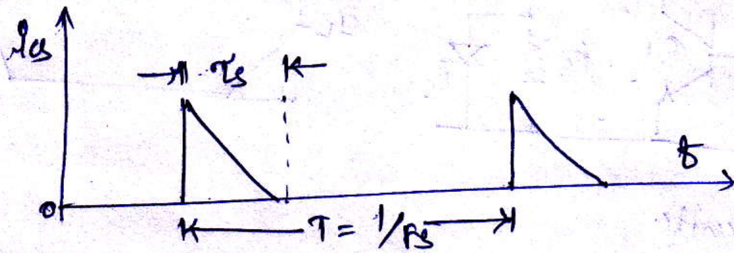
(mode ③ circuit: IL, Dm, Vs, Cs, vs, Rs)

Once the capacitor charged upto Vs, the freewheeling diode turns on & reverse current flows through Ls, there is damped resonance circuit. To avoid continuous oscillations, the circuit must be critically damped. For critically damped series

RLC circuit damping factor $\delta = 1$ & it gives.

$$R_s = 2\sqrt{\frac{L_s}{C_s}} \quad \text{—— (7)}$$

Capacitor discharges through transistor, it increases current rating of transistor. The discharge current through transistor can be avoided by putting R_s across capacitor, instead of diode D_s.



For discharge current, the time constant $R_sC_s = \tau_s$, it must be 1/3 of switch period T.

$$\therefore R_sC_s = \frac{T}{3} = \frac{1}{3f_s}.$$

$$\therefore R_s = \frac{1}{3f_sC_s} \quad \text{—— (8)}.$$