Department of Electronics & Communication Engg.

Course : DAA-15EC751 **Sem.: 7th (2018-19 ODD)**

Course Coordinator:

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DSP Algorithms & Architecture

MODULE-5

Interfacing and Applications of DSP Processor

Introduction

In the case of parallel peripheral interface, the data word will be transferred with all the bits together. In addition to parallel peripheral interface, there is a need for interfacing serial peripherals. DSP has provision of interfacing serial devices too.

Synchronous Serial Interface: There are certain I/O devices which handle transfer of one bit at a time. Such devices are referred to as serial I/O devices or peripherals. Communication with serial peripherals can be synchronous, with processor clock as reference or it can be asynchronous.

Synchronous serial interface (SSI) makes communication a fast serial communication and asynchronous mode of communication is slow serial communication. However, in comparison with parallel peripheral interface, the SSI is slow. The time taken depends on the number of bits in the data word.

CODEC Interface Circuit:

CODEC, a coder-decoder is an example for synchronous serial I/O. It has analog input-output, ADC and DAC. The signals in SSI generated by the DSP are DX: Data Transmit to CODEC, DR: Data Receive from CODEC, CLKX: Transmit data with this clock reference, CLKR: Receive data with this clock reference, FSX: Frame sync signal for transmit, FSR: Frame sync signal for receive, First bit, during transmission or reception, is in sync with these signals.

RRDY: indicator for receiving all bits of data and

XRDY: indicator for transmitting all bits of data. Similarly, on the CODEC side, signals are FS*: Frame sync signal, DIN: Data Receive from DSP,

DOUT: Data Transmit to DSP and SCLK: Tx / Rx data with this clock reference.
As only one signal each is available on CODEC for clock and frame synchronization, the related DSP side signals are connected together to clock and frame sync signals on CODEC. Fig. 8.2 and fig. 8.3 show the timings for receive and transmit in SSI, respectively.

Receiver Timing for SSI

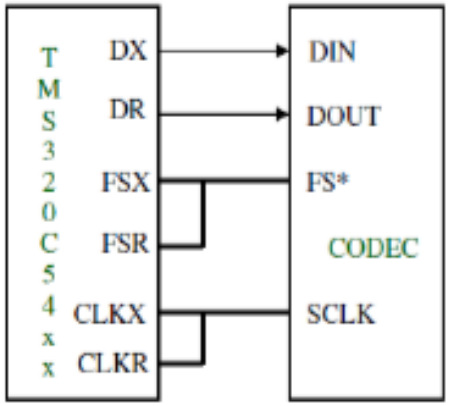

Fig. 8.1: SSI between DSP & CODEC

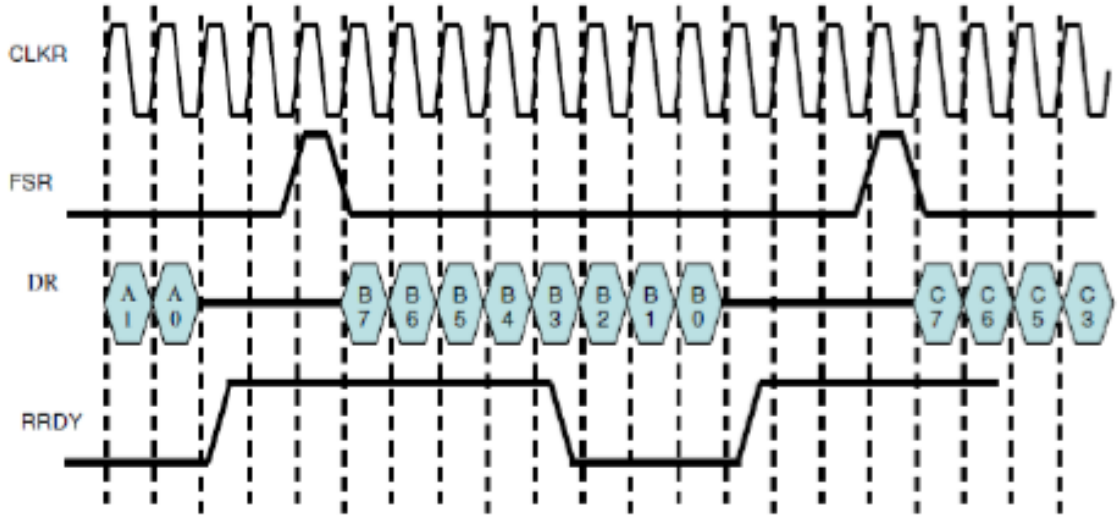

Fig. 8.2: Receive Timing for SSI

Transmit Timing for SSI

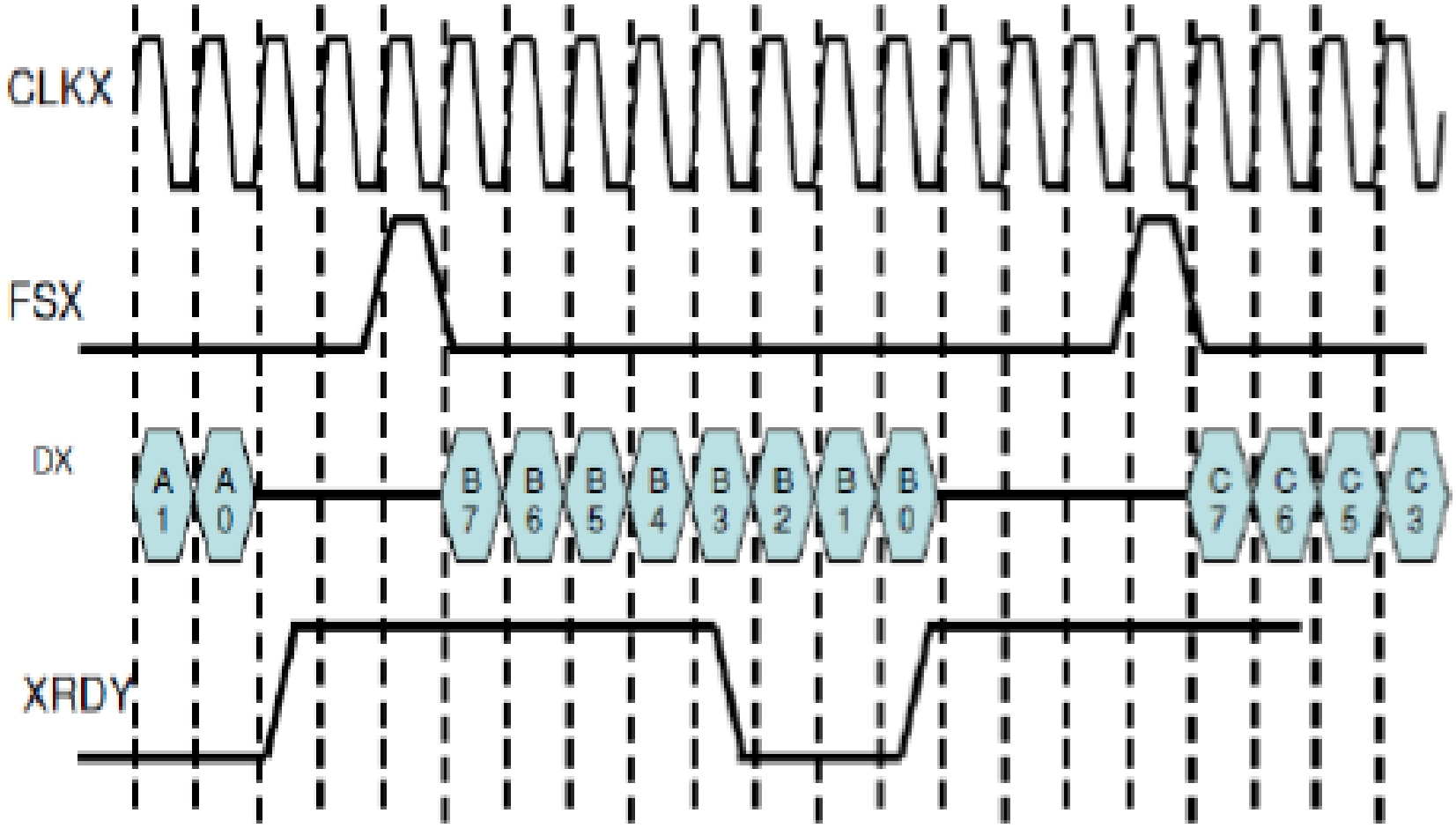

Fig 8.3: Transmit Timing for SSI

CODEC PCM3002

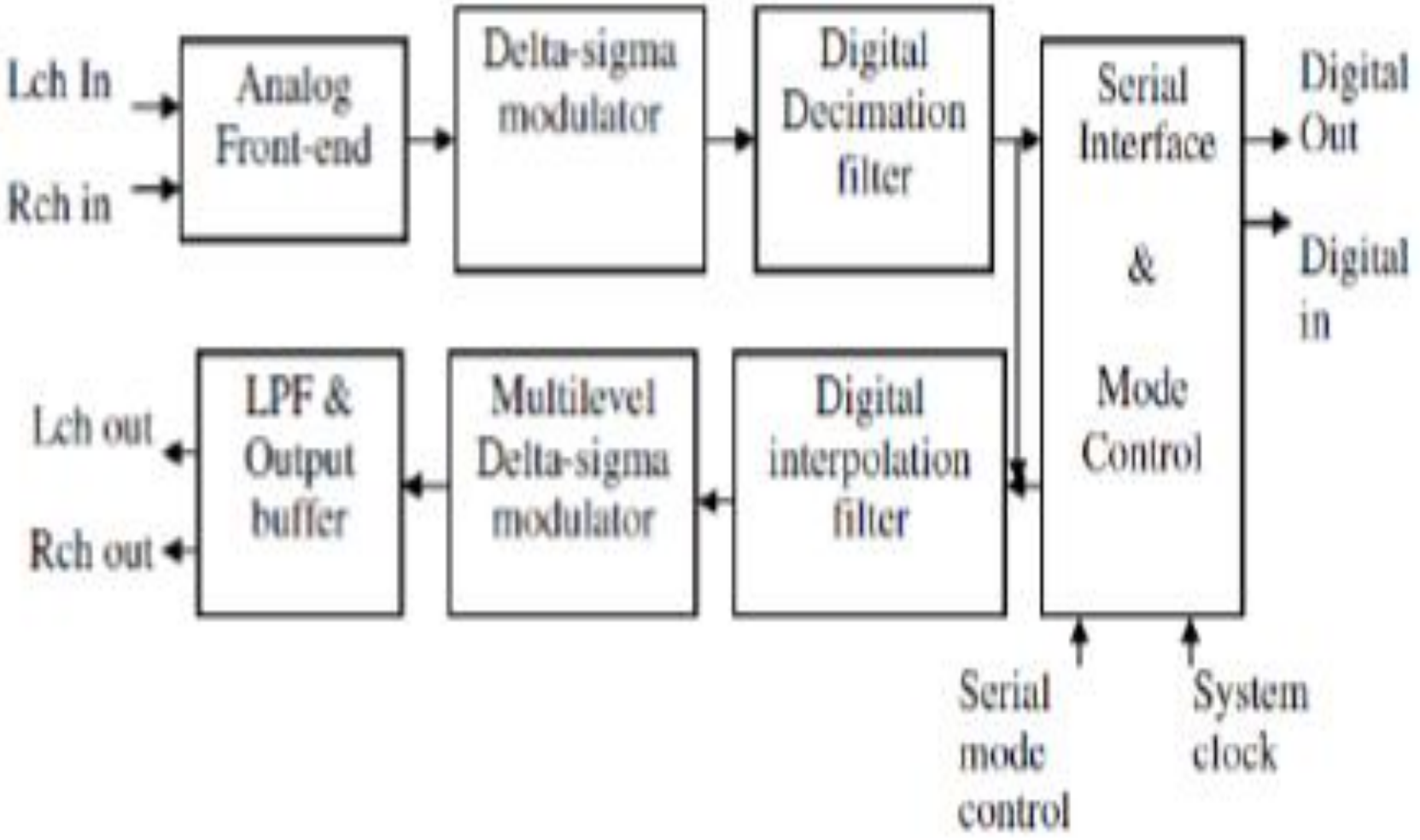

Fig. 8.4: Block diagram for CODEC PCM3002

PCM3002 Interface to DSP in DSK

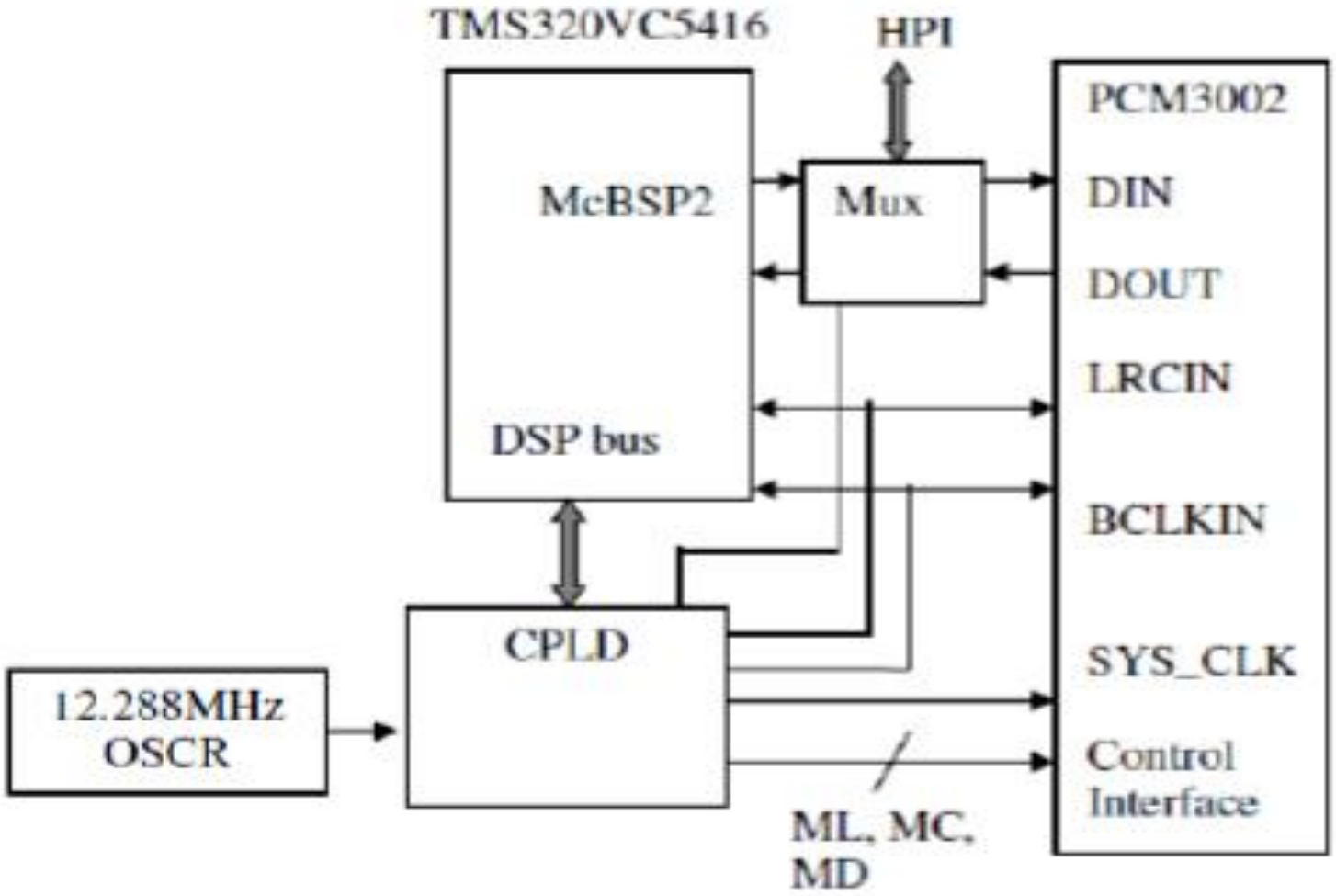

Fig. 8.5: PCM3003 Interface to DSP in DSK

Bio-Telemetry Receiver

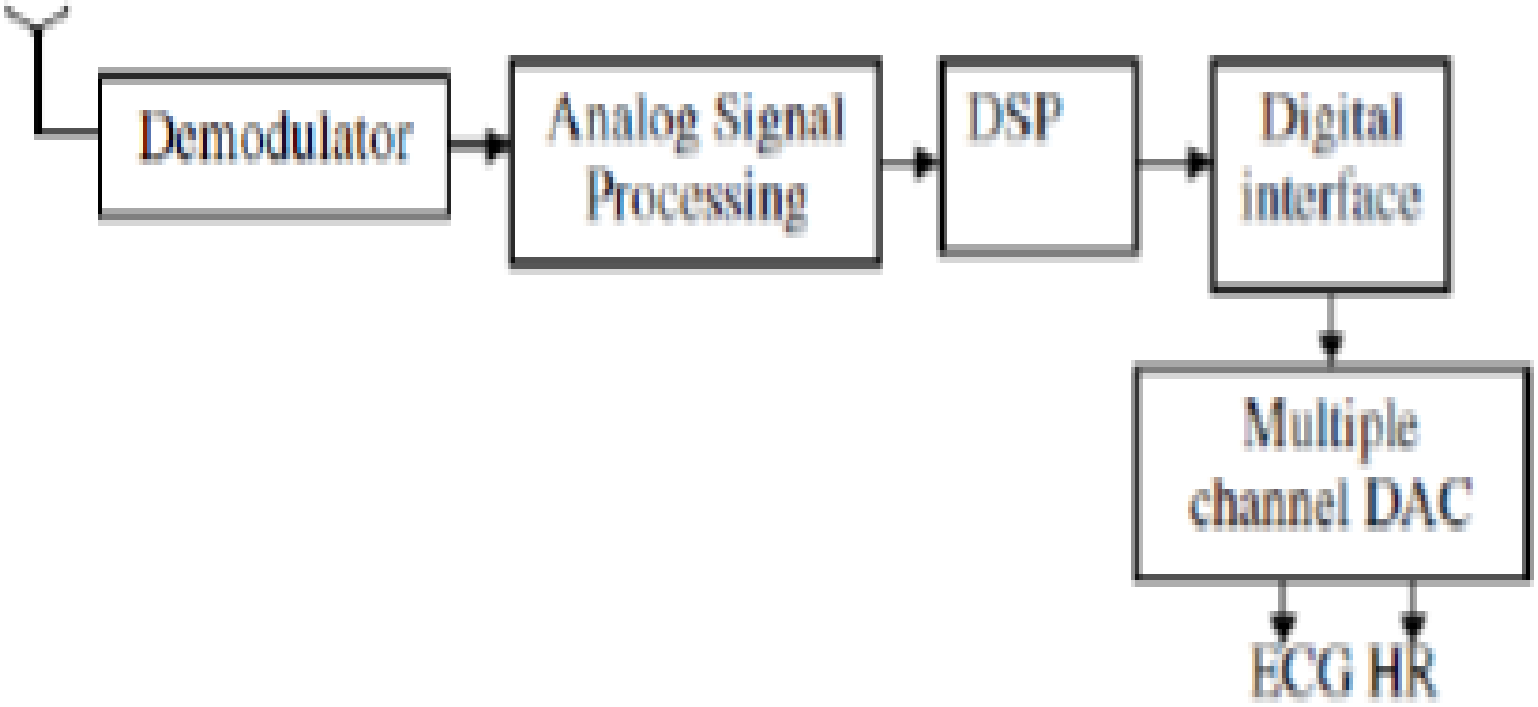

Fig. 8.8: Bio-telemetry Receiver

DSP Based Bio-Telemetry Receiver

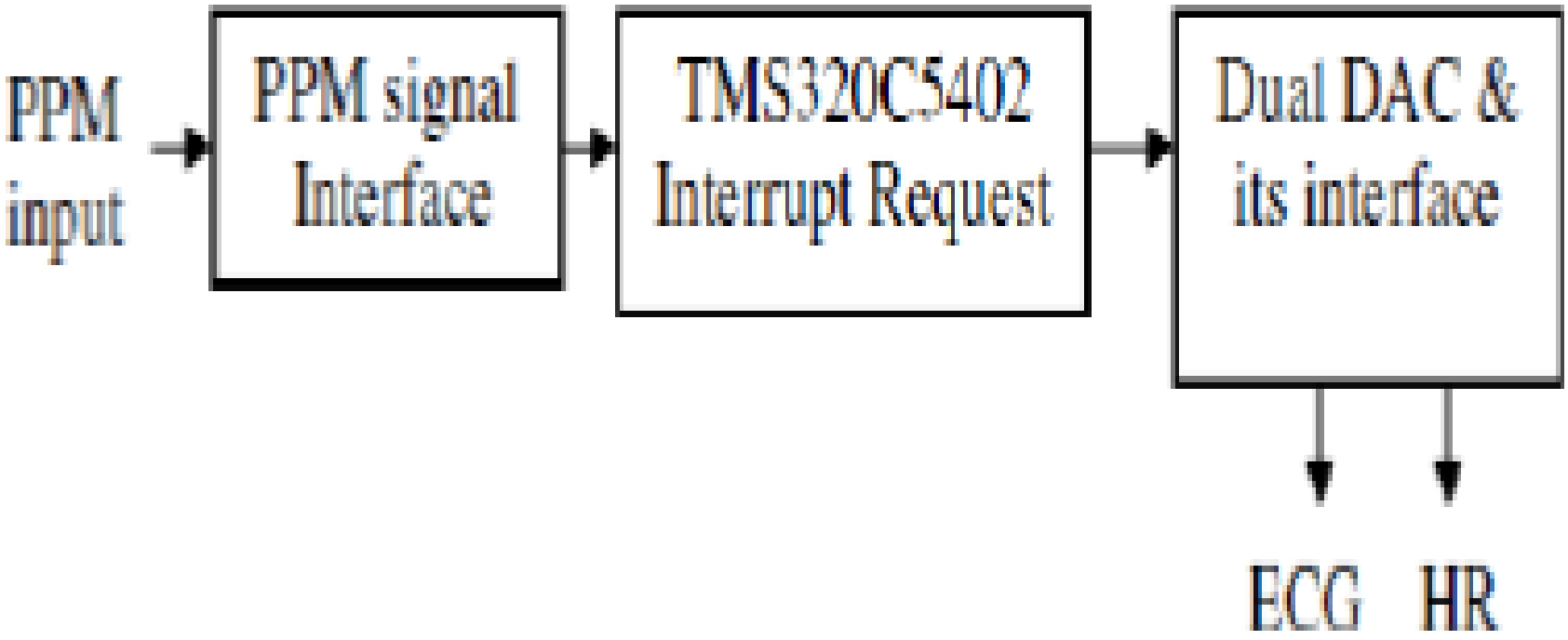

Fig. 8.11: DSP based biotelemetry Receiver Implementation

Signals in Determination of HR

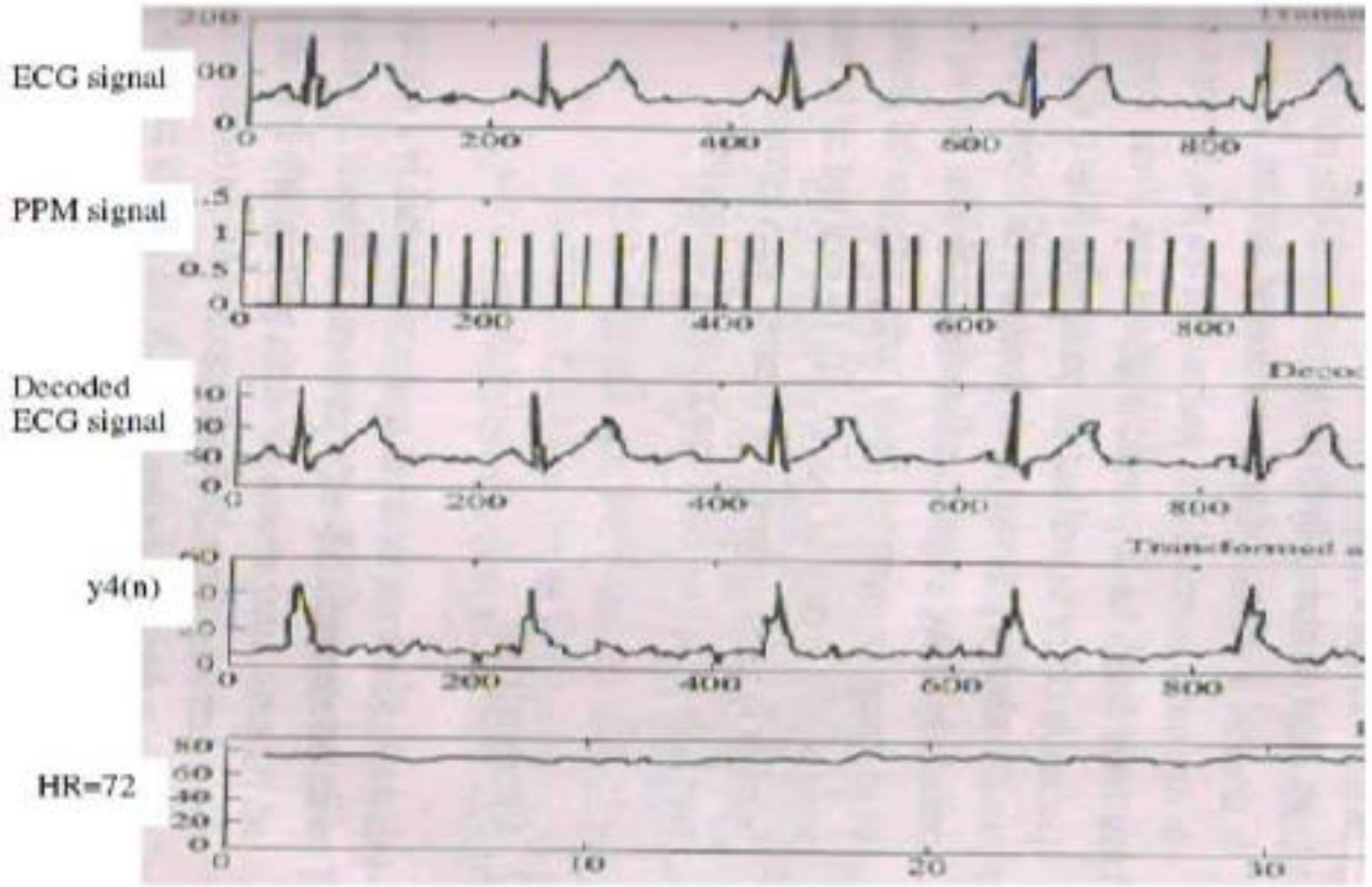

Fig. 8.12: Signals in determination of HR

Speech Production Mechanism

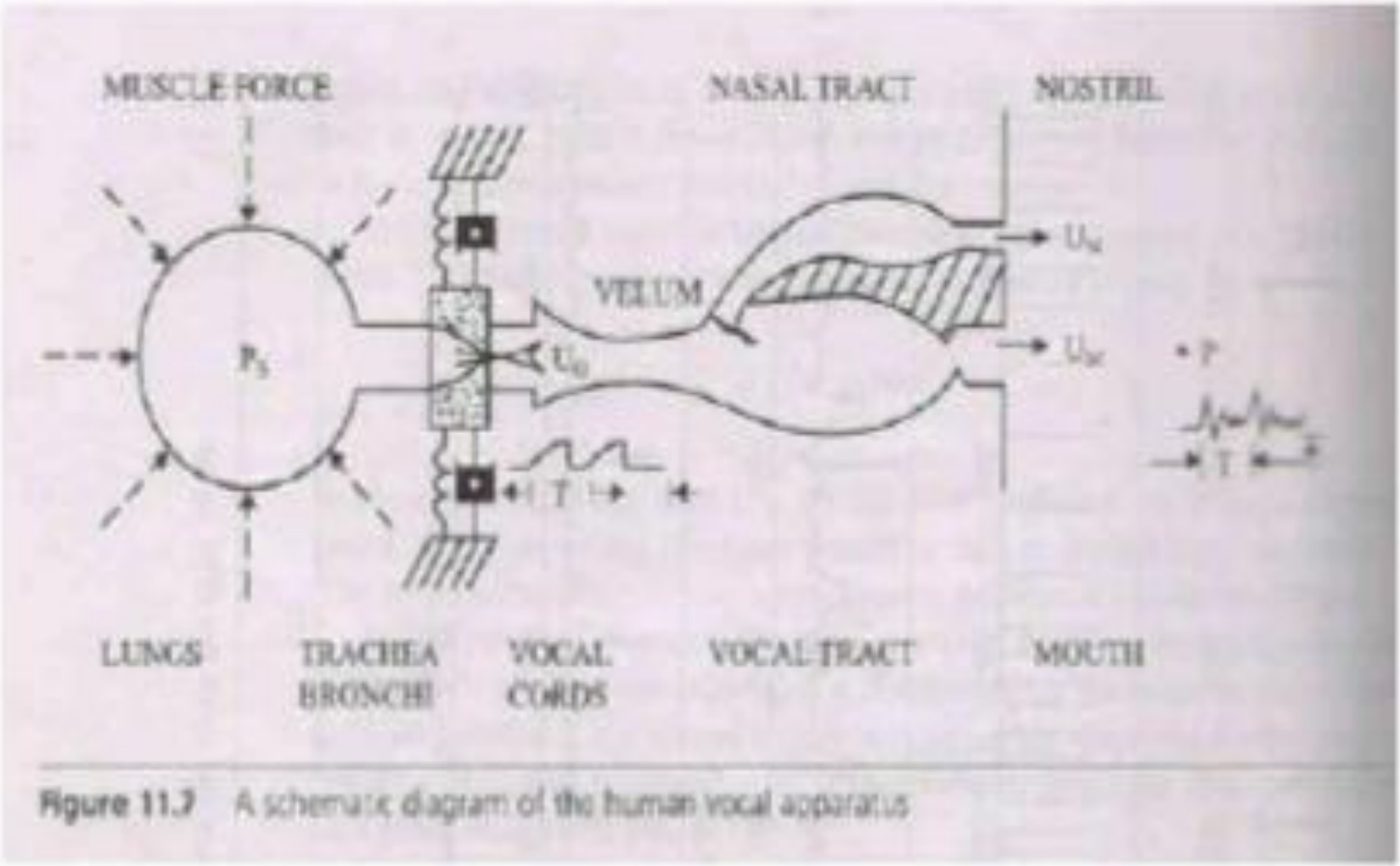

Fig. 8.13: Speech Production Mechanism

Autocorrelation Pitch Detector

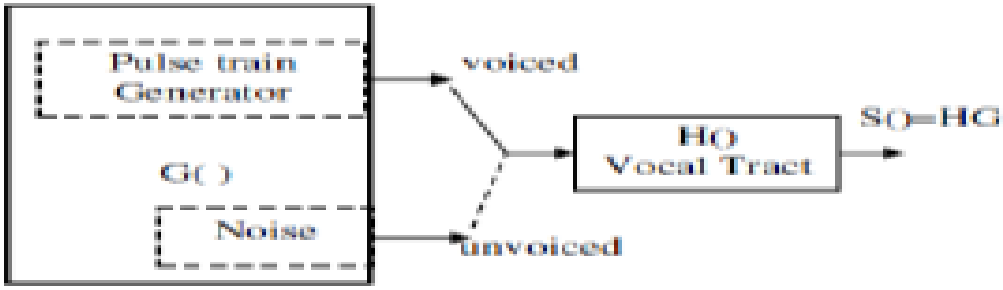

Fig. 8.14: Speech Production Model

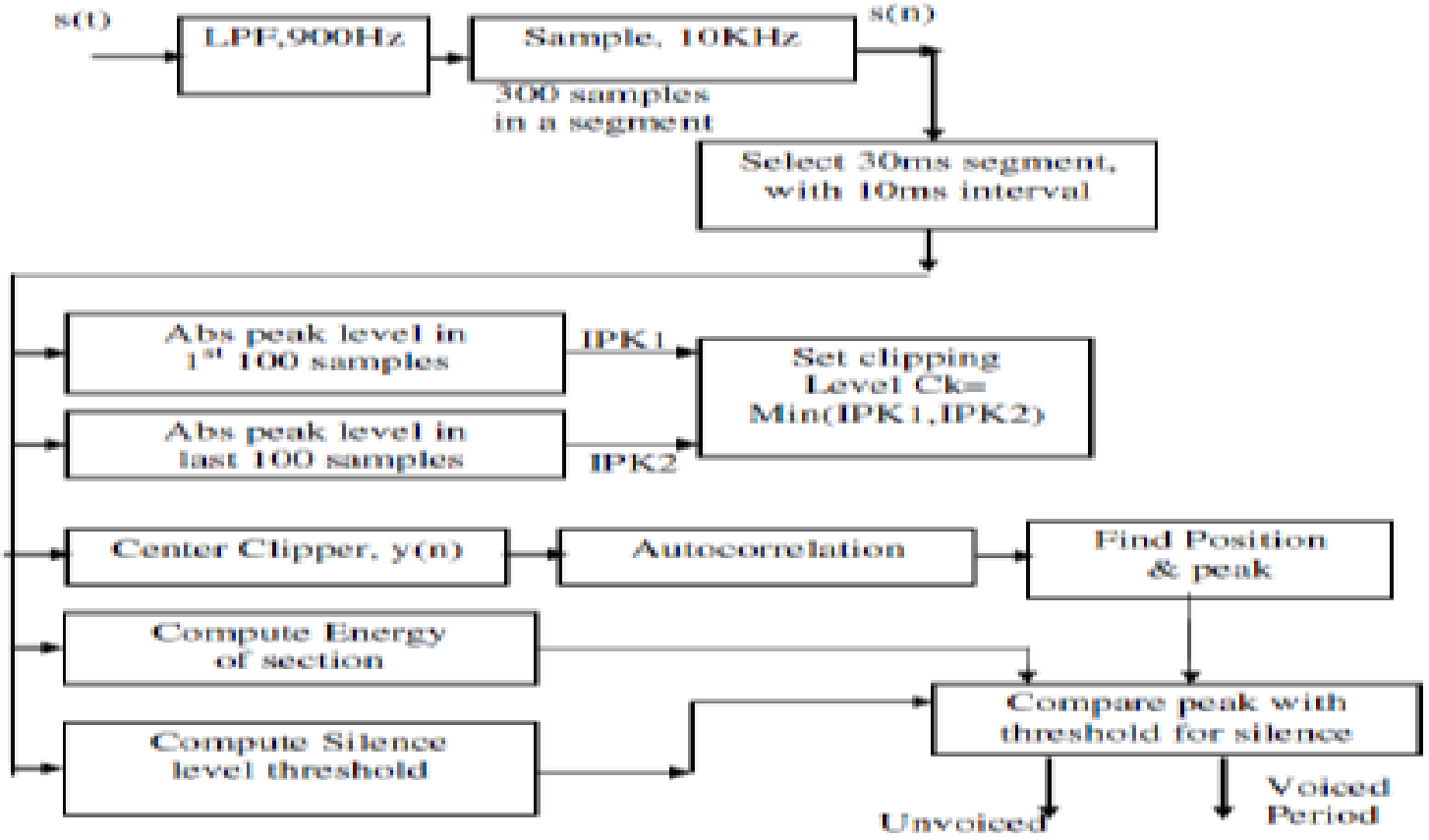

Fig. 8.15: Block Diagram of Clipping Autocorrelation Pitch Detector

JPEG Encoder & Decoder

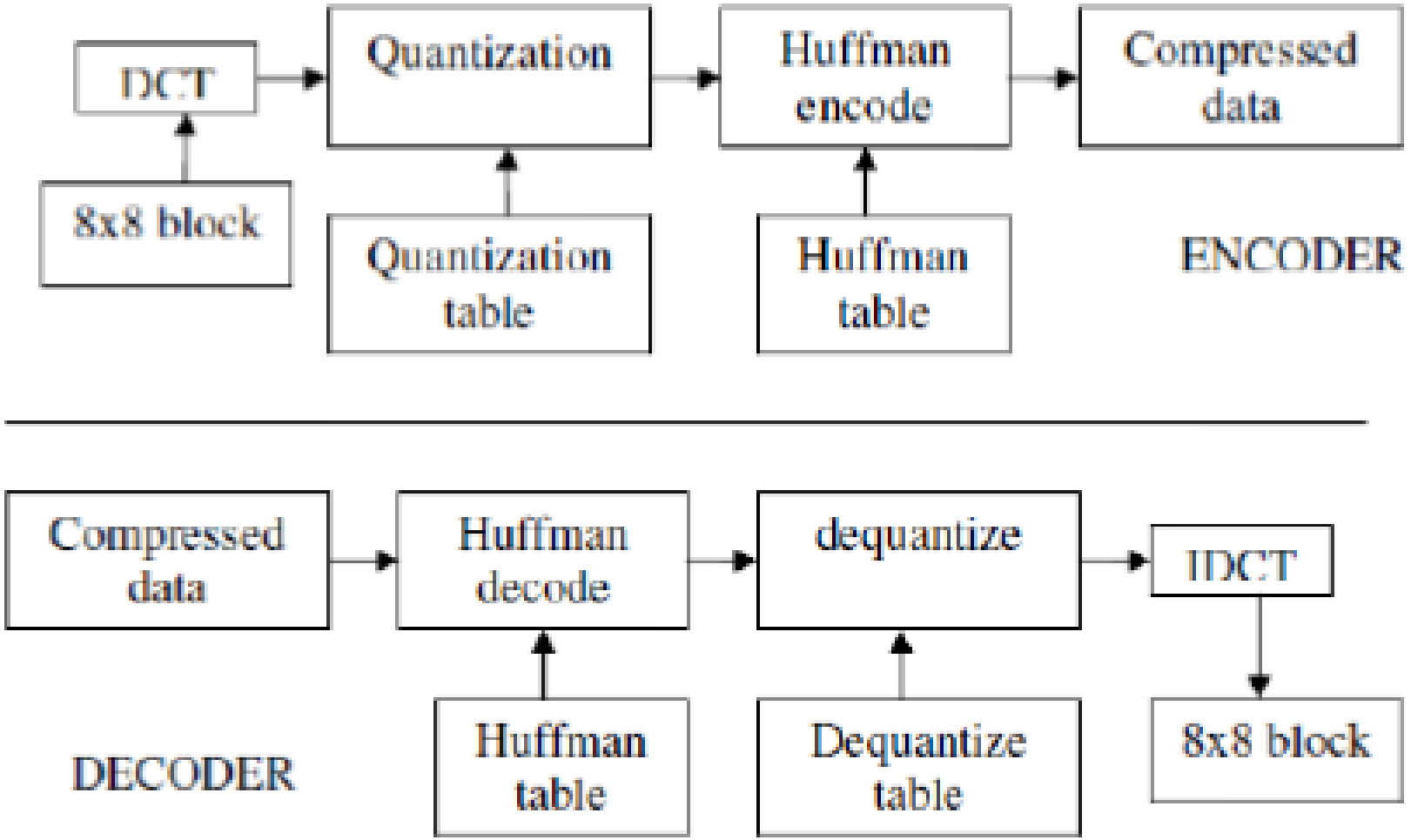

Fig. 8.21: JPEG Encoder & Decoder

Queries ...?