Department of Electronics & Communication Engg.

Course : DAA-15EC751 **Sem.: 7th (2018-19 ODD)**

Course Coordinator:

Prof. Nyamatulla M Patel

DSP Algorithms & Architecture

MODULE-3

Programmable Digital Signal Processors

Summary of the Architectural Features of three fixed-Points DSPs

Architectural Feature	TMS320C25	DSP 56000	ADSP2100
Data representation format	16-bit fixed	24-bit fixed point	16-bit fixed point
Hardware multiplier	16 x 16	24 x 24	16 x 16
ALU	32 bits	56 bits	40 bits
Internal buses	16-bit program bus 16-bit data bus	24-bit program bus 2 x 24-bit data buses 24-bit global	24-bit program bus 16-bit data bus 16-bit result

Summary of the Architectural Features of three fixed-Points DSPs

		databus	bus
External buses	16-bit program/data bus	24-bit program/data bus	24-bit program bus 16-bit data bus
On-chip Memory	544 words RAM 4K words ROM	512 words PROM 2 x 256 words data RAM 2 x 256 words data ROM	-
Off-chip memory	64 K words program 64k words data	64K words program 2 x 64K words data	16K words program 16K words data
Cache memory	-	-	16 words program
Instruction cycle time	100 nsec	97.5 nsec.	125 nsecc.
Special addressing modes	Bit reversed	Modulo Bit reversed	Modulo Bit reversed
Data address generators	1	2	2
Interfacing features	Synchronous serial I/O DMA	Synchronous and Asynchronous serial I/O DMA	DMA

Functional architecture for TMS320C54xx processors

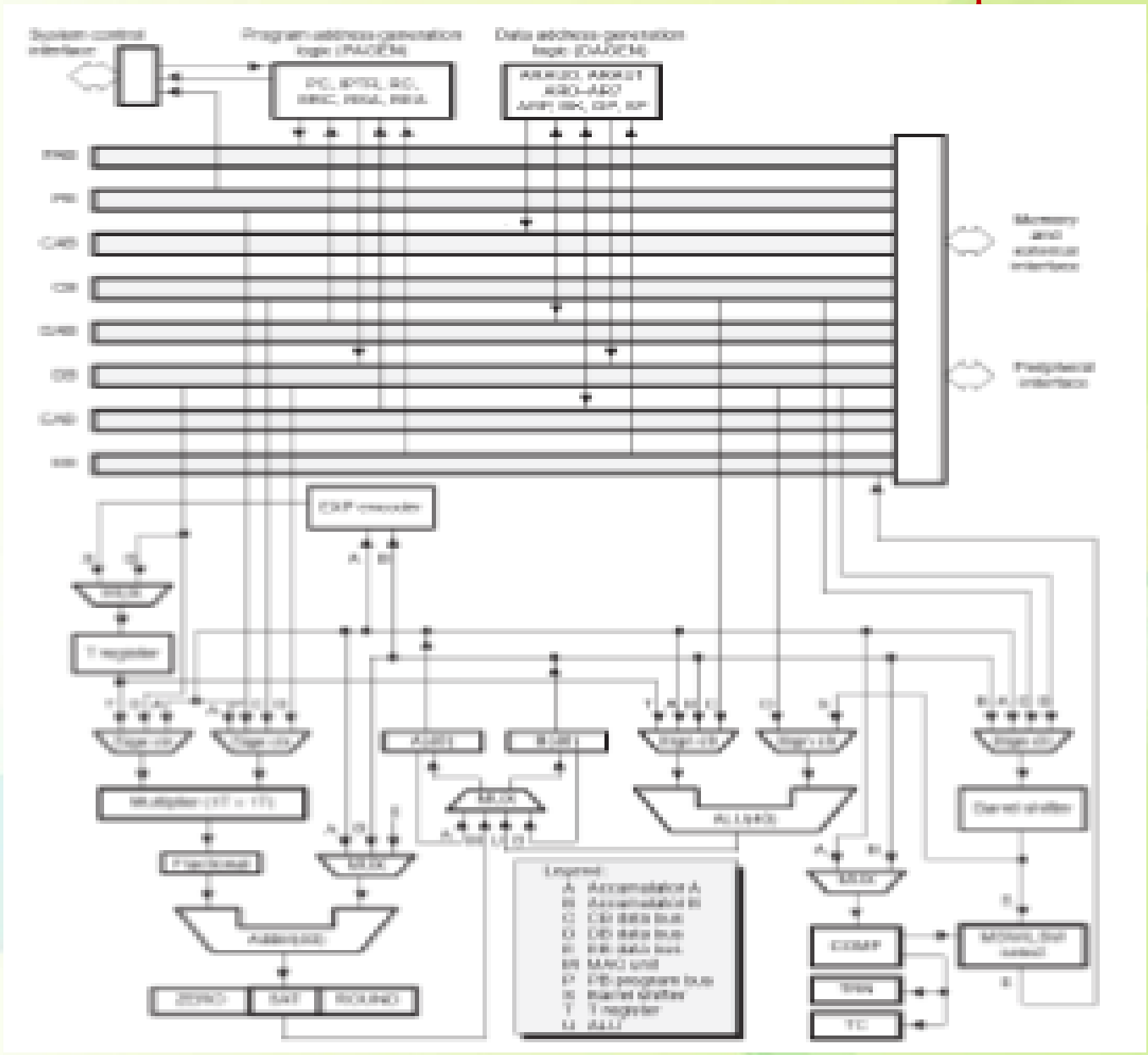


Figure 3.1.Functional architecture for TMS320C54xx processors.

Functional diagram of the central processing unit of the TMS320C54xx processors.

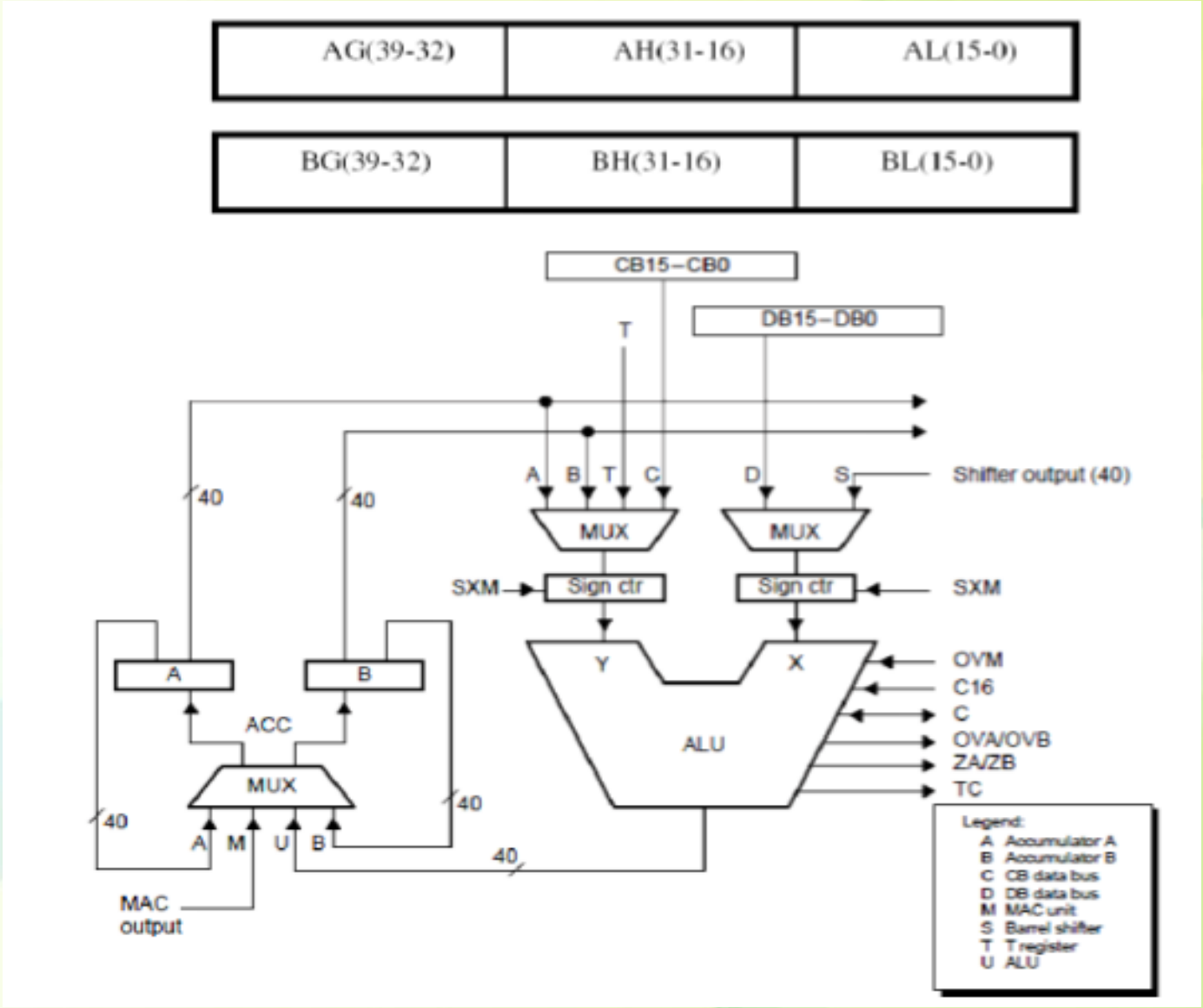


Figure 3.2.Functional diagram of the central processing unit of the TMS320C54xx processors.

Functional diagram of the barrel shifter

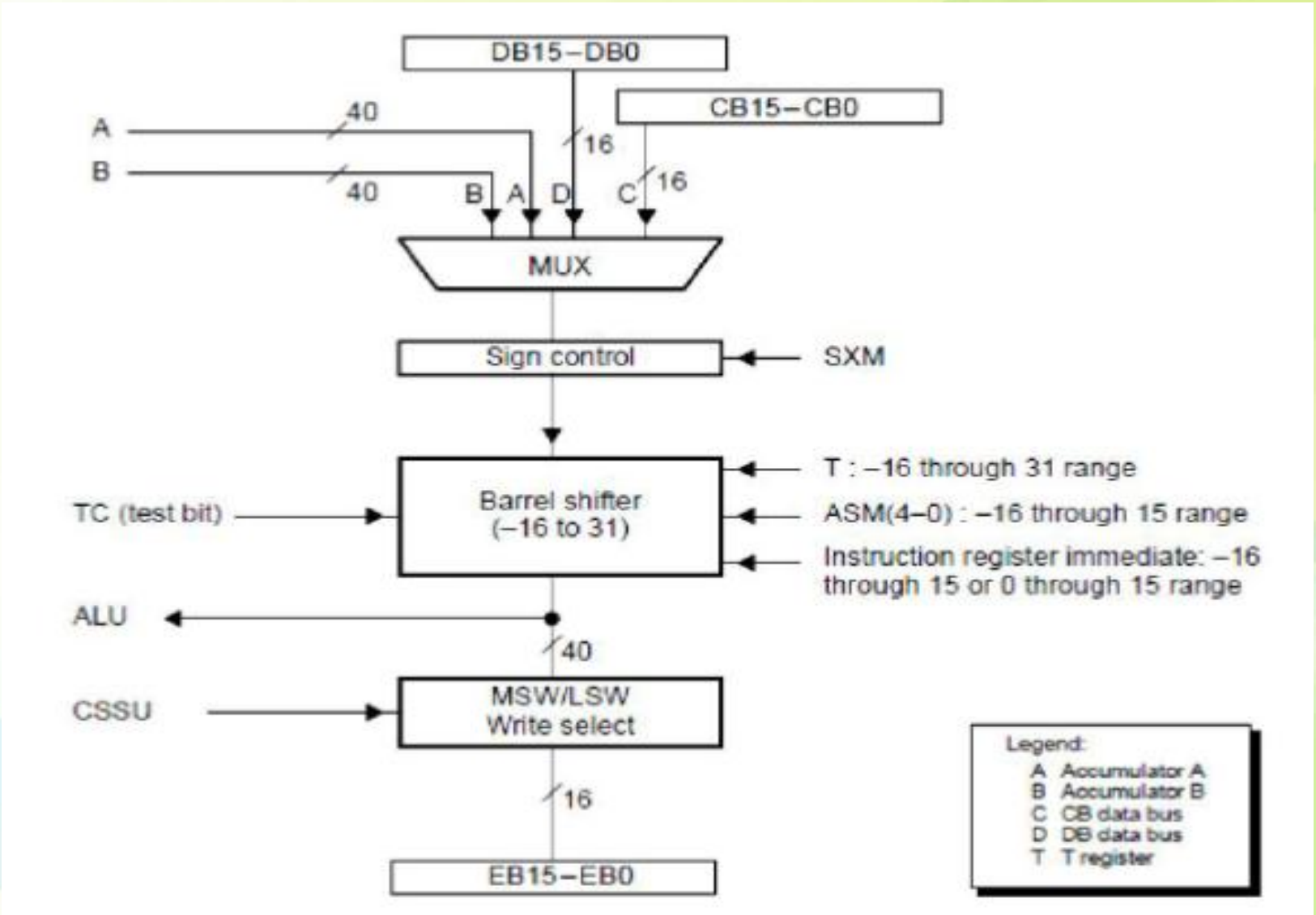


Figure 3.3.Functional diagram of the barrel shifter

Functional diagram of the multiplier/adder unit of TMS320C54xx processors.

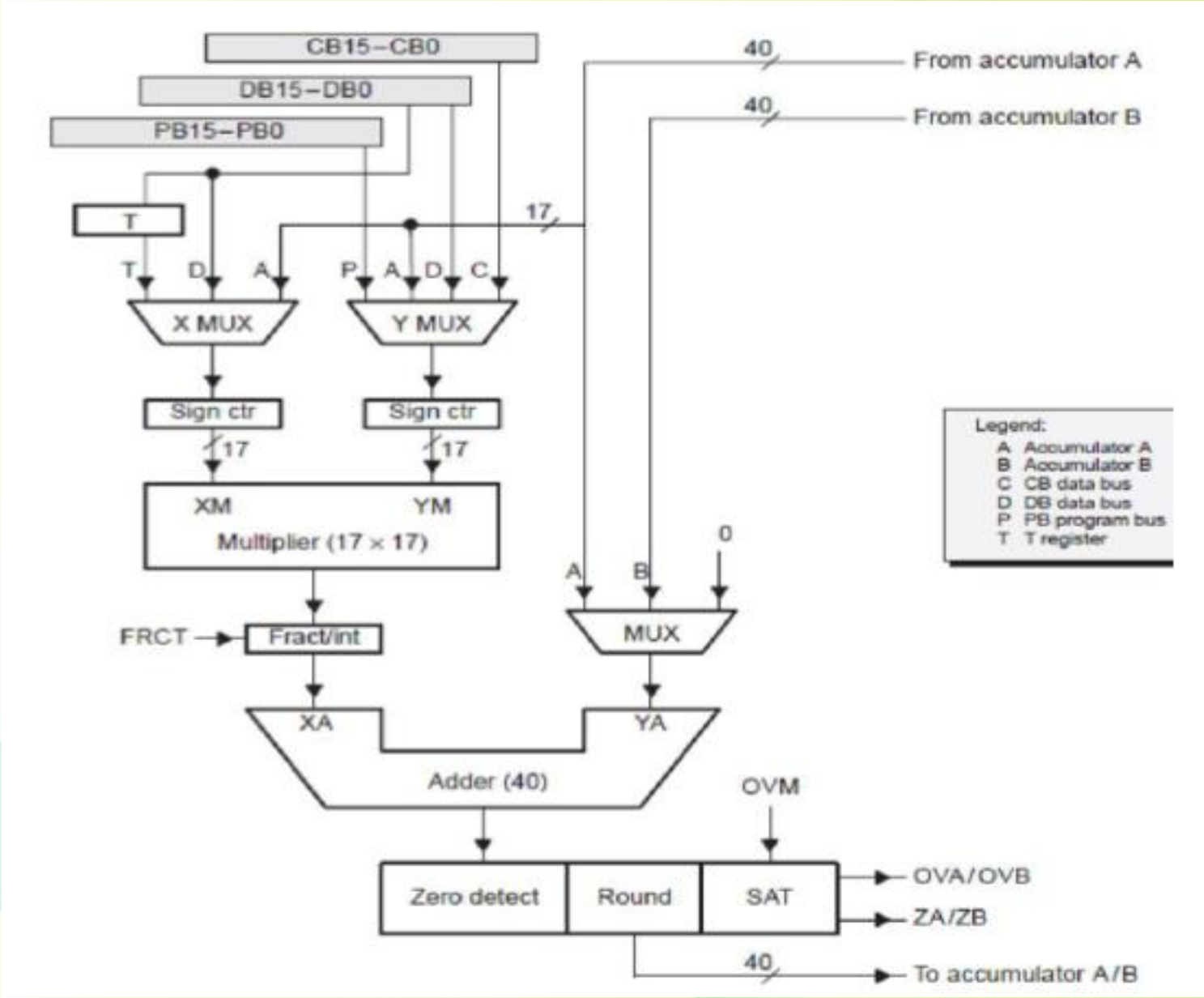


Figure 3.4. Functional diagram of the multiplier/adder unit of TMS320C54xx processors.

Block diagram of the direct addressing mode for TMS320C54xx Processors.

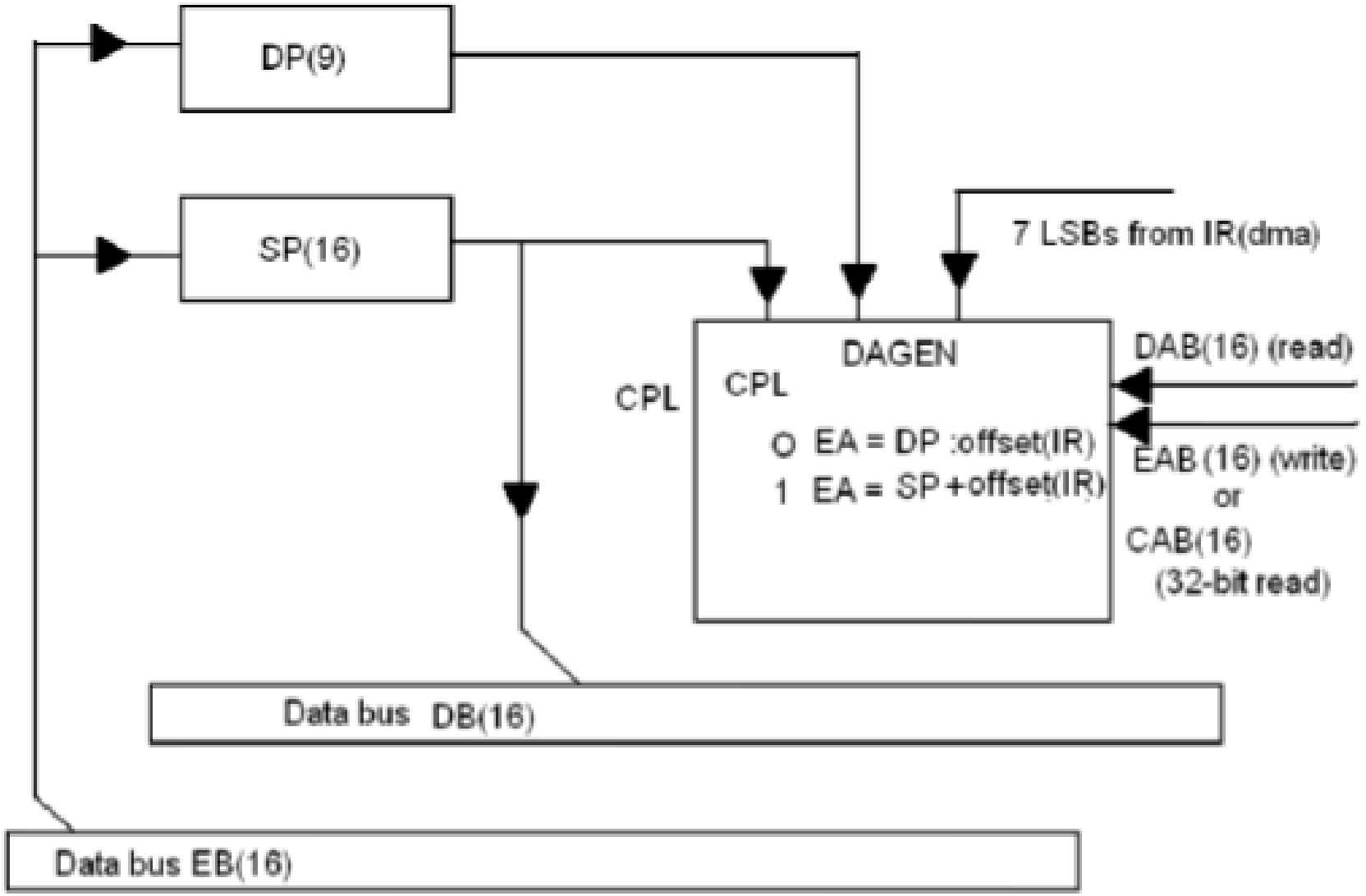


Figure 3.7 Block diagram of the direct addressing mode for TMS320C54xx Processors.

Indirect Addressing Mode

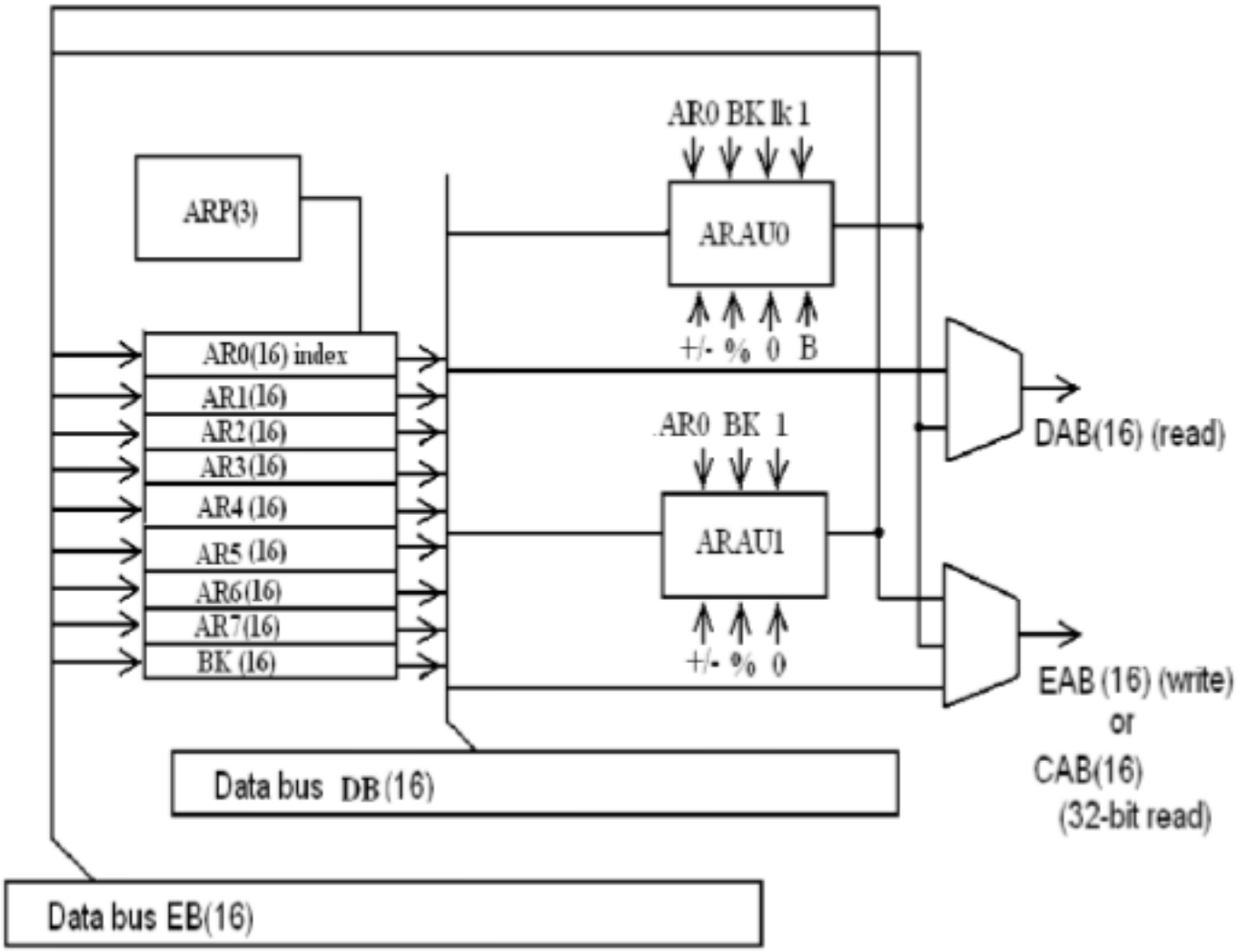


Figure 3.8 Block diagram of the indirect addressing mode for TMS320C54xx Processors.

Circular Addressing Mode

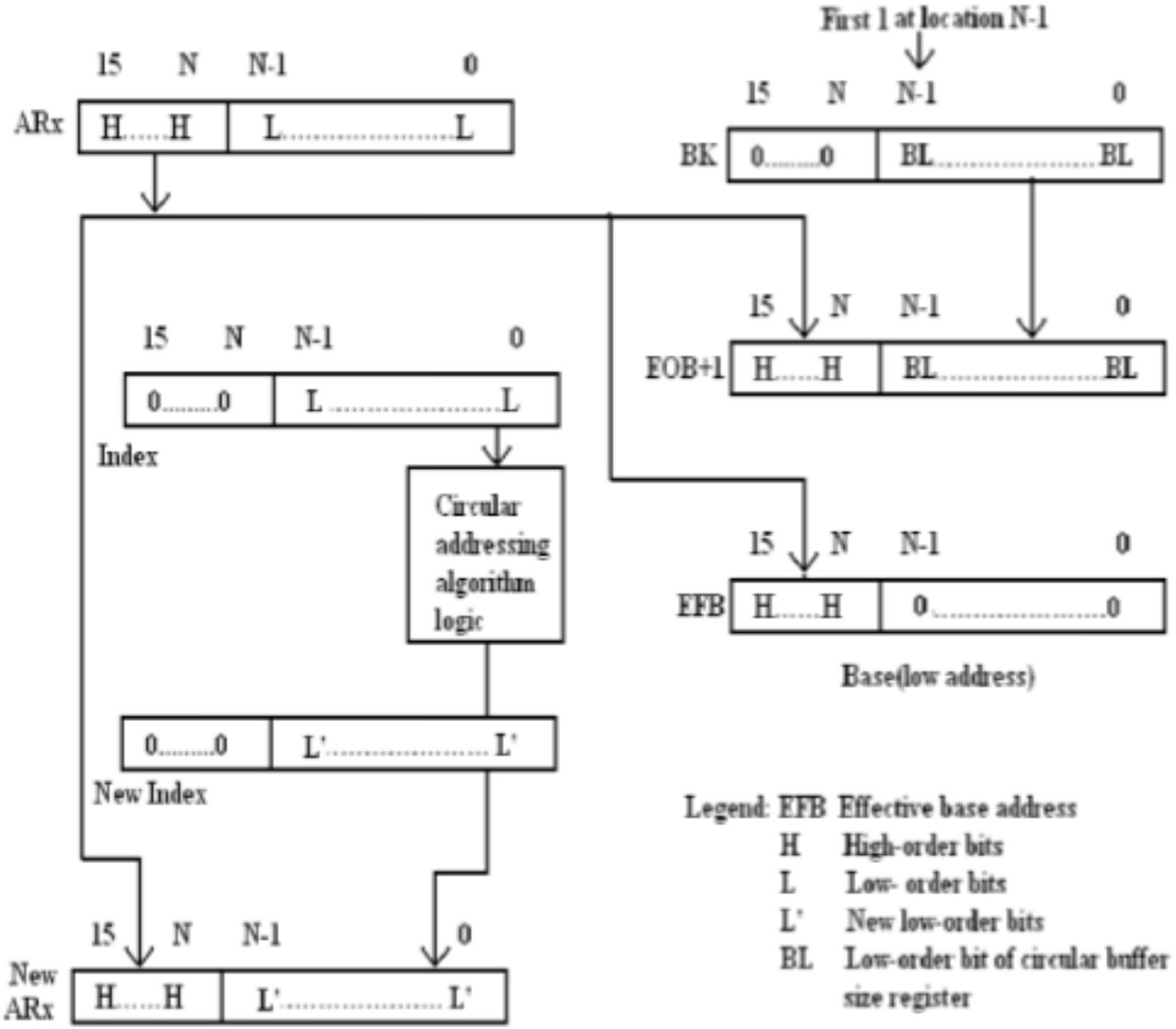


Figure 3.9 Block diagram of the circular addressing mode for TMS320C54xx Processors.

Circular Addressing Mode Contd…

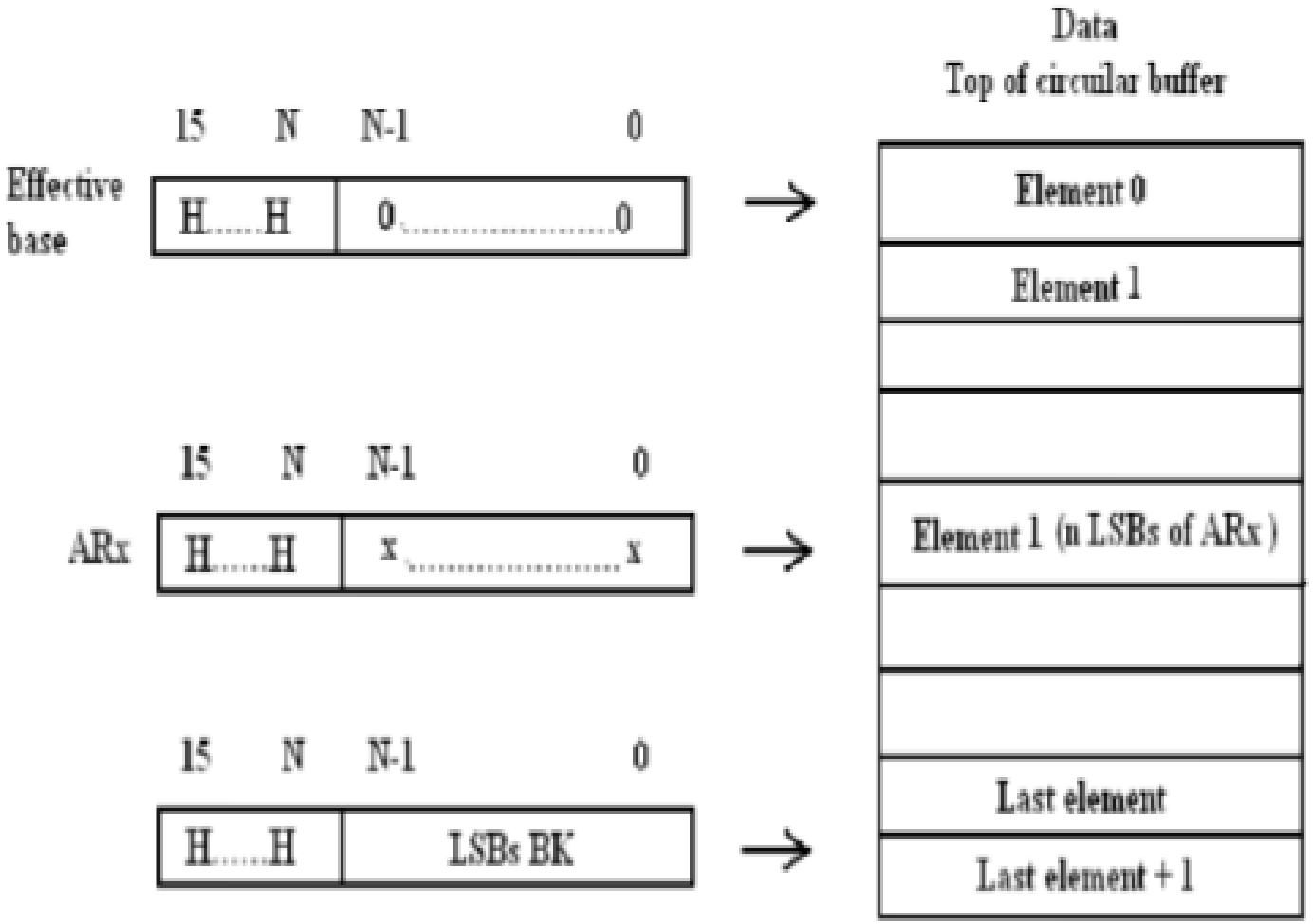
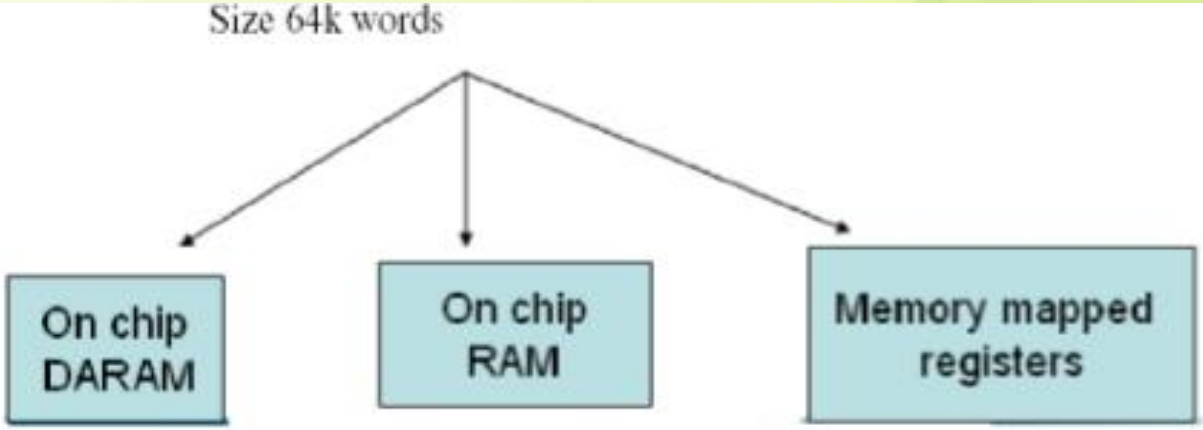
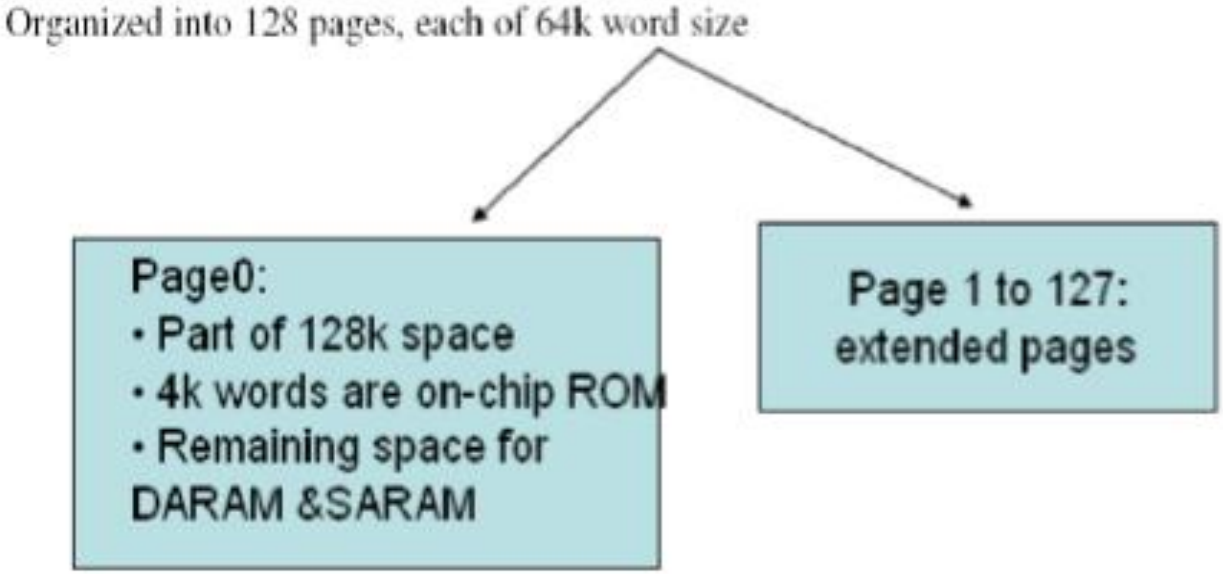


Figure 3.10 circular addressing mode implementation for TMS320C54xx Processors.

Memory Space of TMS320C54xx Processors



Program memory: To store program instructions &tables used in the execution of programs.



Queries ...?