Department of Electronics & Communication Engg.

Course : DAA-15EC751 **Sem.: 7th (2018-19 ODD)**

Course Coordinator:

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DSP Algorithms & Architecture

MODULE-2

Architectures for Programmable Digital Signal Processing Devices

Basic Architectural Features

A programmable DSP device should provide instructions similar to a conventional microprocessor. The instruction set of a typical DSP device should include the following,

a. Arithmetic operations such as ADD, SUBTRACT, MULTIPLY etc

b. Logical operations such as AND, OR, NOT, XOR etc

c. Multiply and Accumulate (MAC) operation

d. Signal scaling operation

In addition to the above provisions, the architecture should also include,

a. On chip registers to store immediate results

b. On chip memories to store signal samples (RAM)

c. On chip memories to store filter coefficients (ROM)

Braun Multiplier for a 4X4 Multiplication

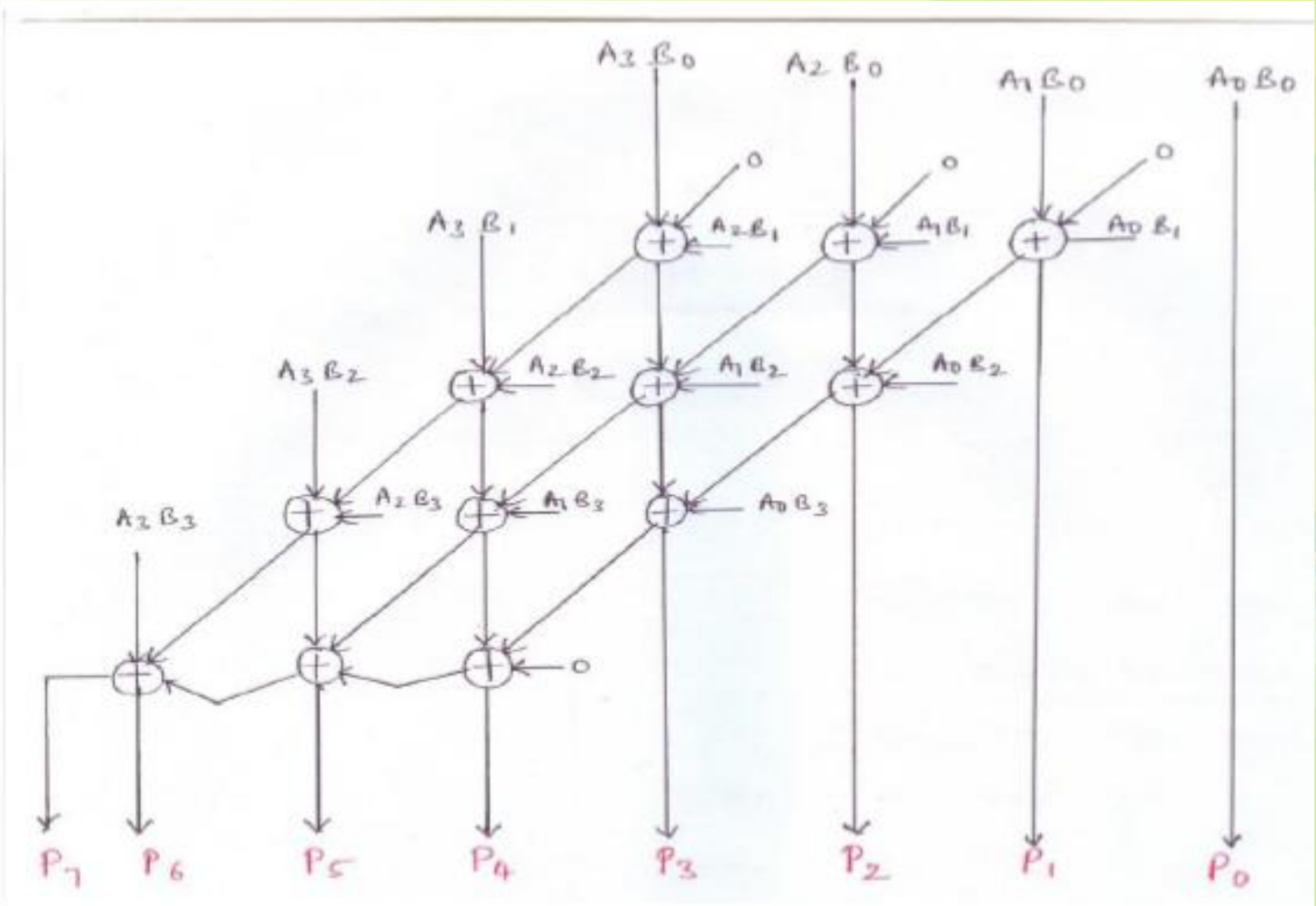


Fig 2.1 Braun Multiplier for a 4X4 Multiplication

A Multiplier with Input and Output Latches

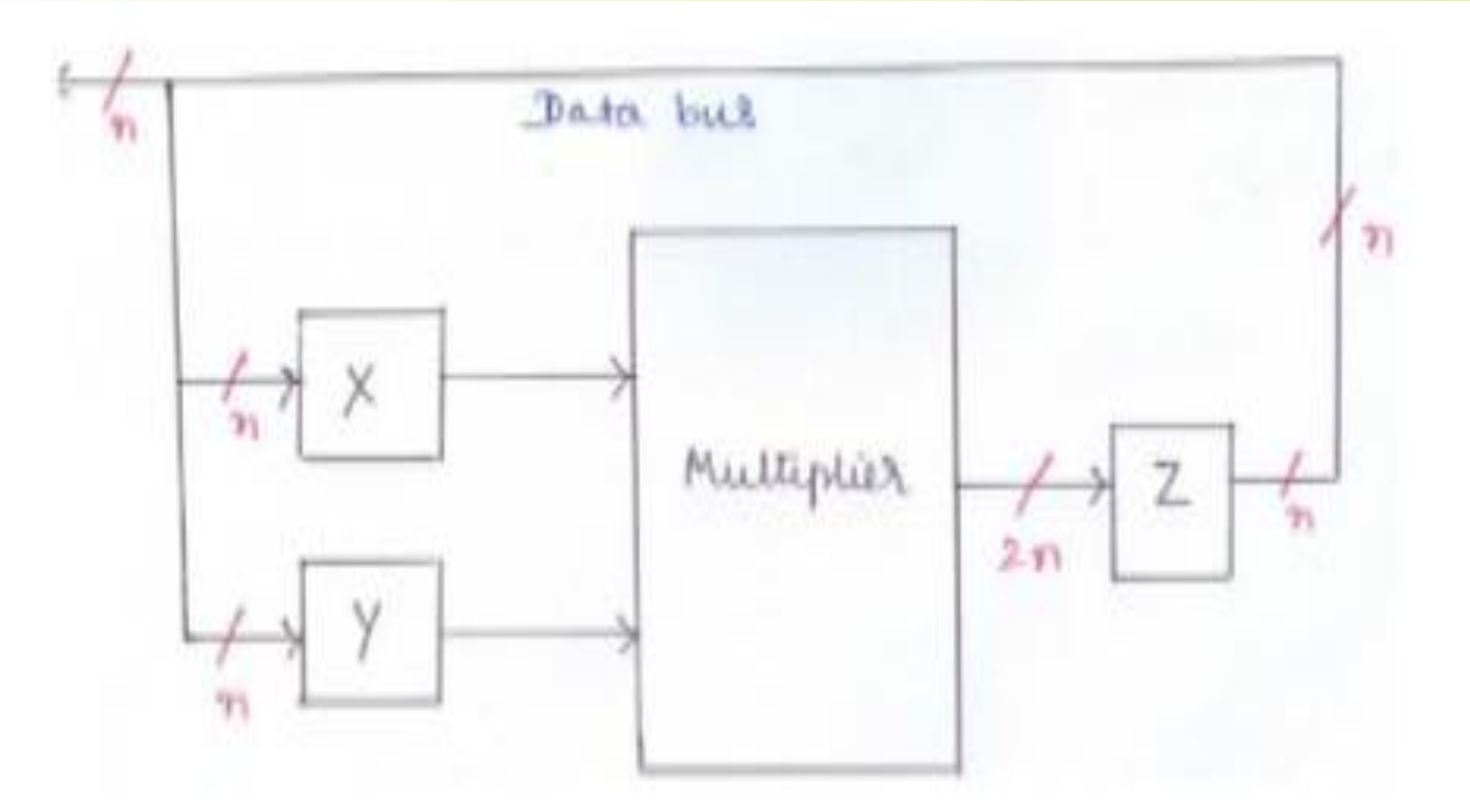


Fig 2.2: A Multiplier with Input and Output Latches

A Barrel Shifter

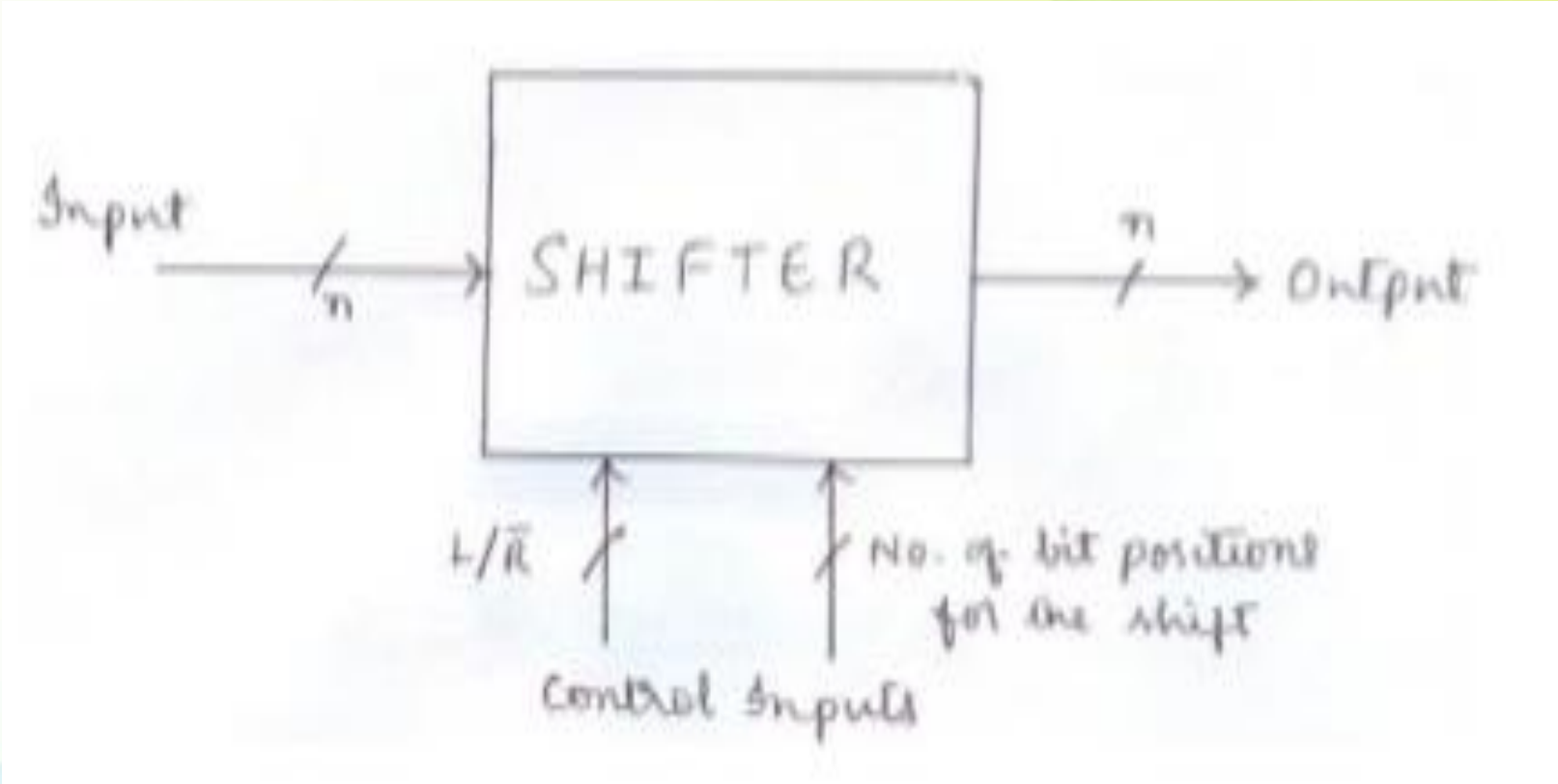
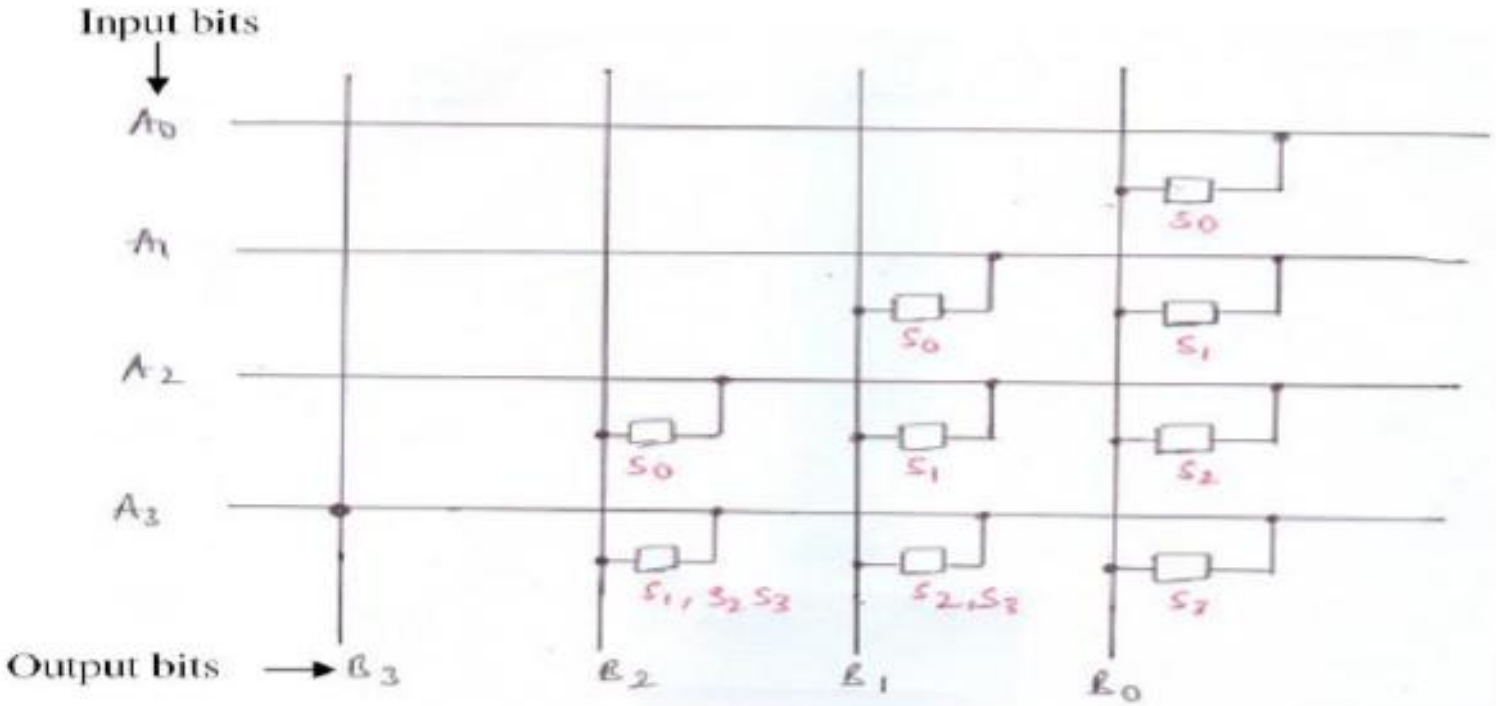


Fig 2.3 A Barrel Shifter

Implementation of a 4 bit Shift Right Barrel Shifter



INPUT				SHIFT (SWITCH)	OUTPUT (B_3 B_2 B_1 B_0)			
A_3	A_2	A_1	A_0	0 (S_0)	A_3	A_2	A_1	A_0
A_3	A_2	A_1	A_0	1 (S_1)	A_3	A_3	A_2	A_1
A_3	A_2	A_1	A_0	2 (S_2)	A_3	A_3	A_3	A_2
A_3	A_2	A_1	A_0	3 (S_3)	A_3	A_3	A_3	A_3

Fig 2.4 Implementation of a 4 bit Shift Right Barrel Shifter

A MAC Unit

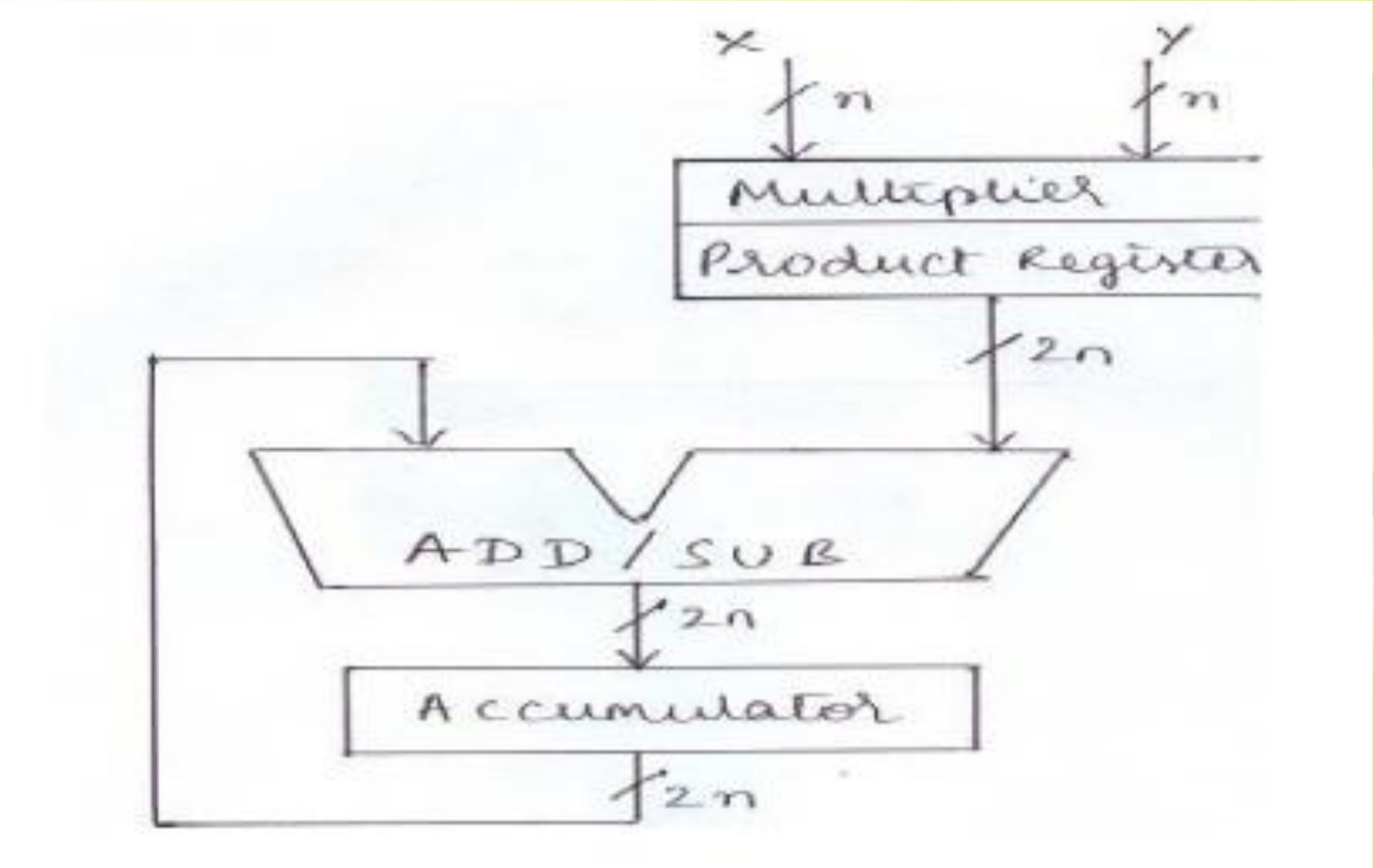


Fig 2.5 A MAC Unit

Saturation Logic

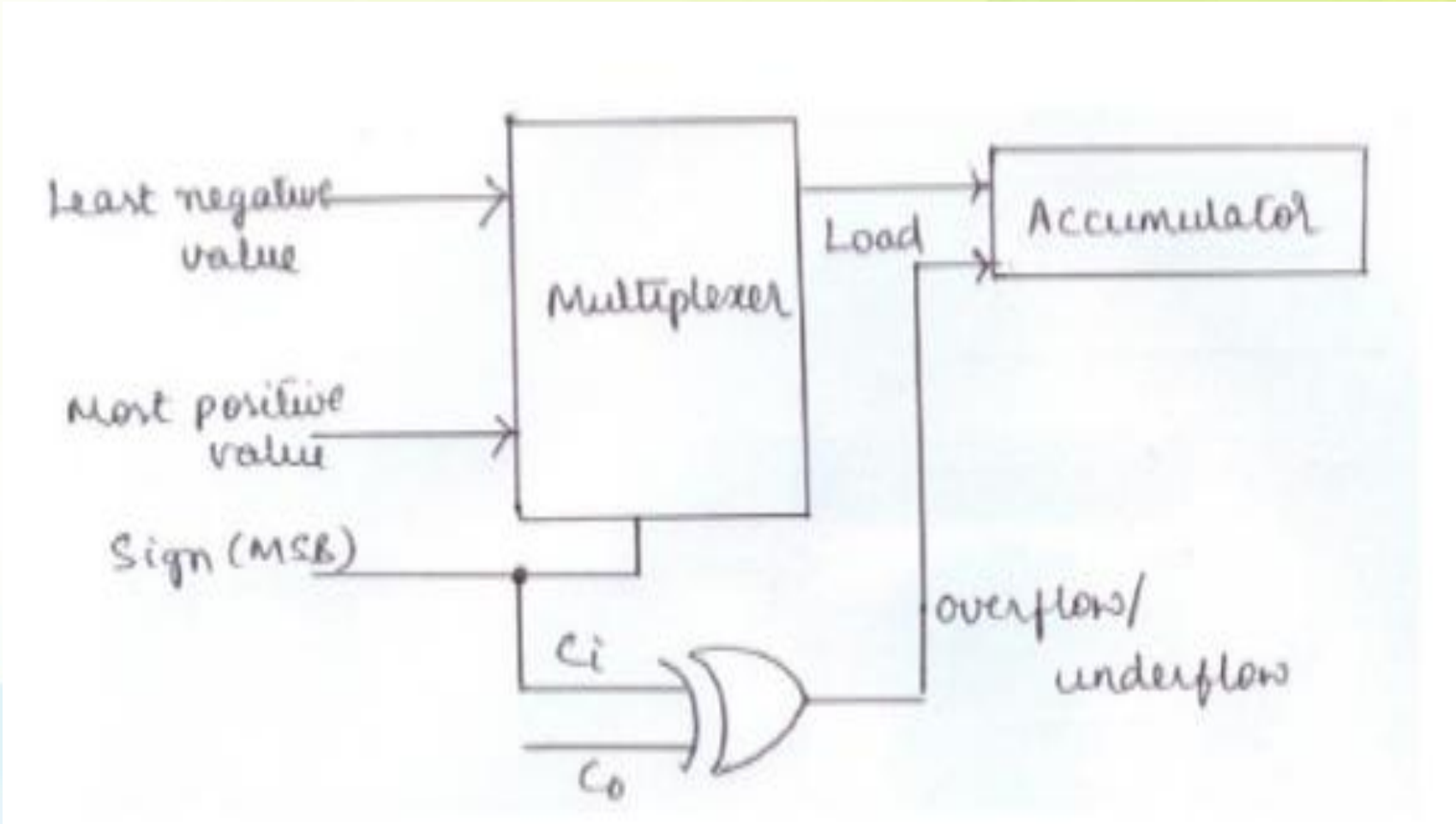


Fig 2.7: Schematic Diagram of the Saturation Logic

Arithmetic Logic Unit of a DSP

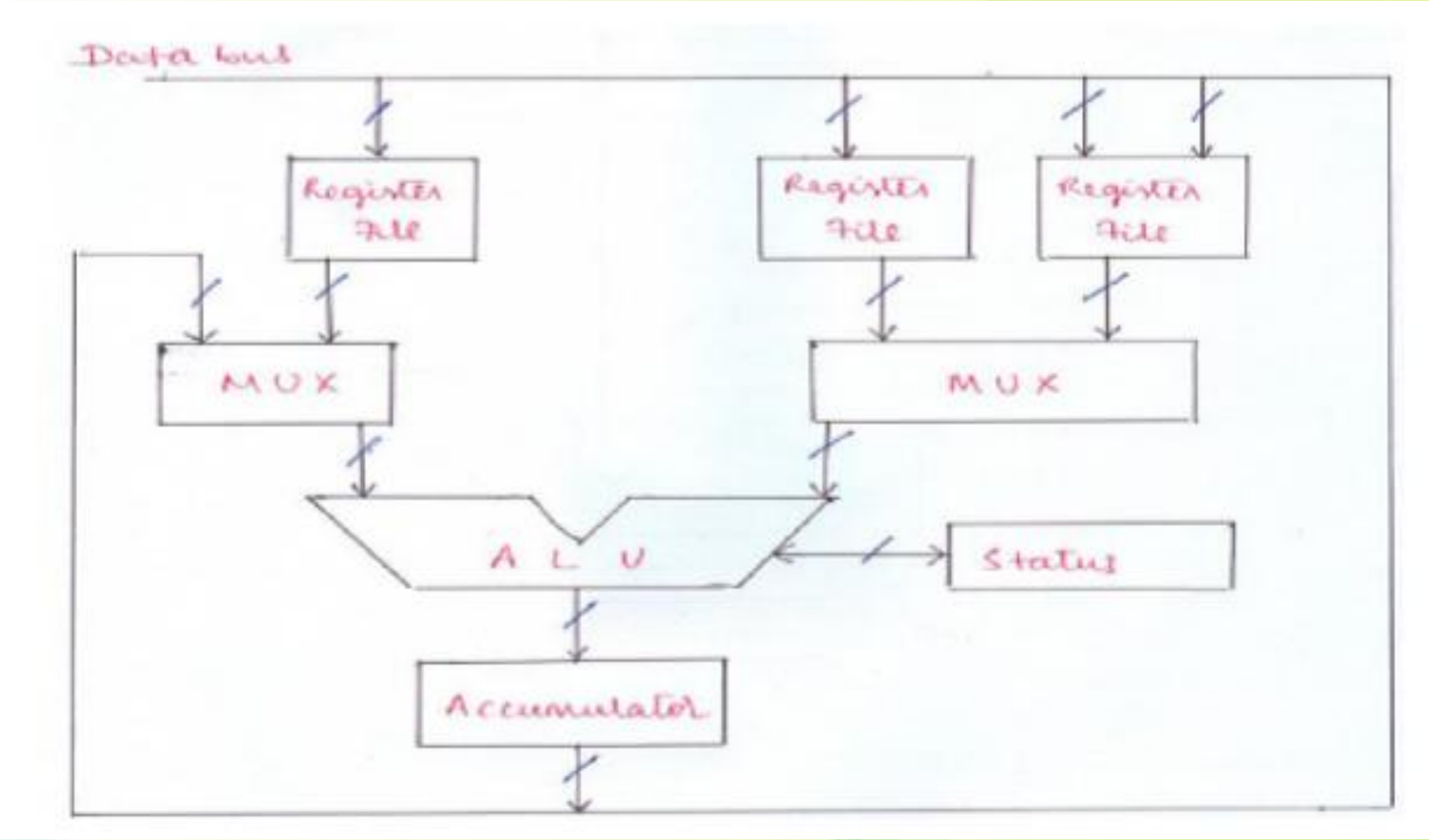


Fig 2.8 Arithmetic Logic Unit of a DSP

Harvard Architecture with Dual Data Memory

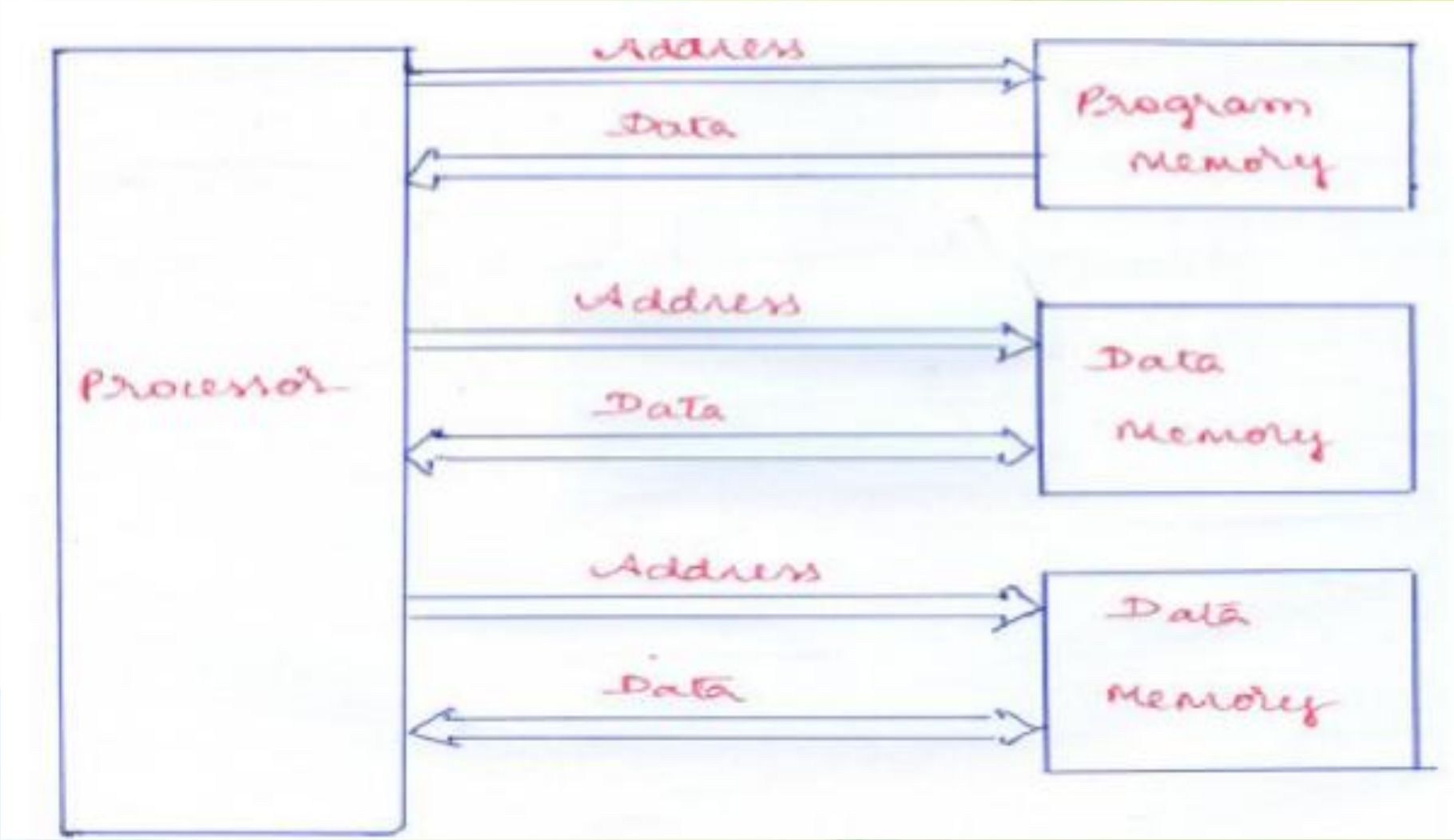


Fig 2.11 Harvard Architecture with Dual Data Memory

Address generation unit

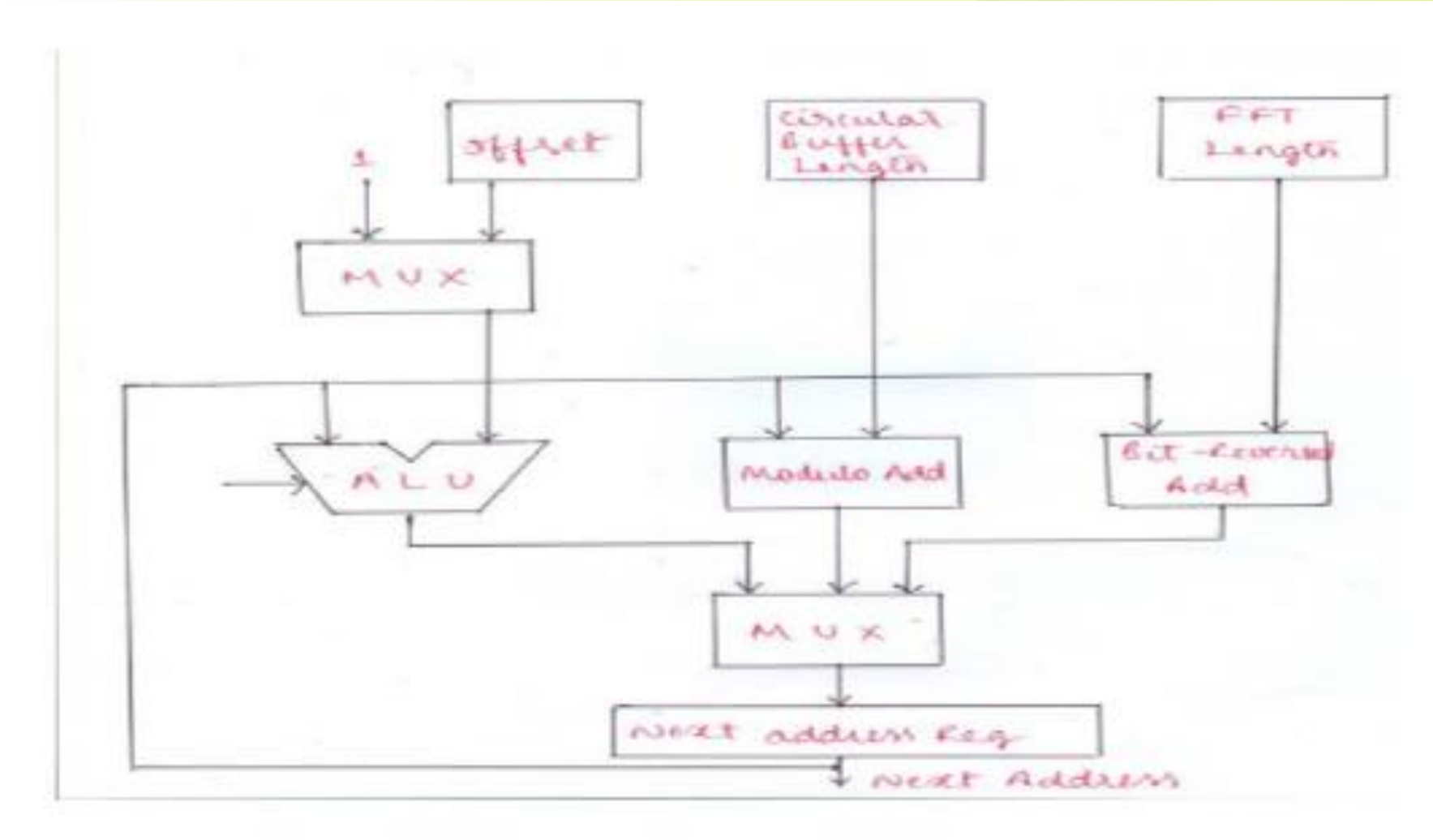


Fig 2.13 Address generation unit

Program Sequencer

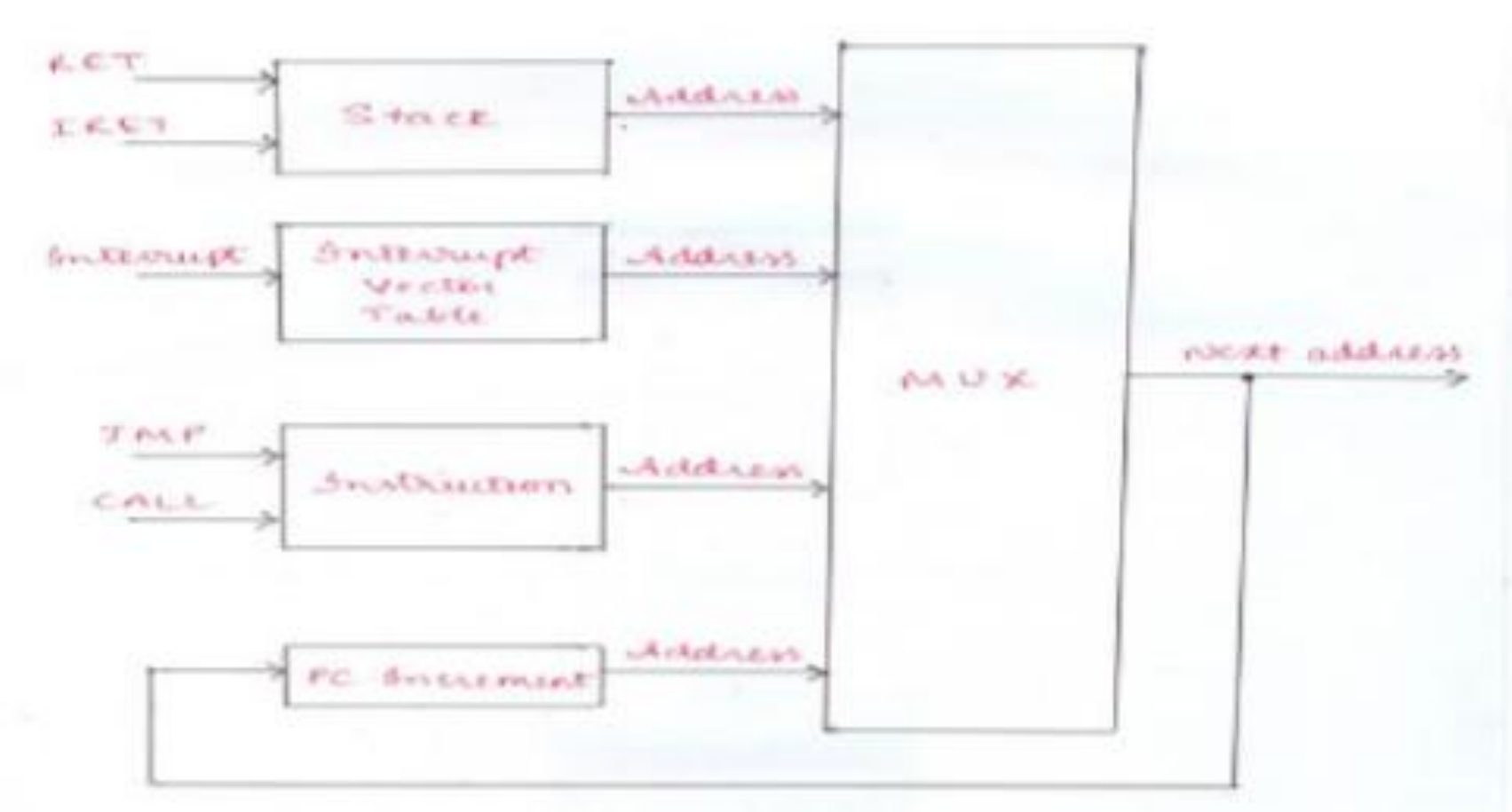


Fig 2.14 Program Sequencer

Queries ...?