# Department of Electronics & Communication Engg.

**Course : VLSI DESIGN-15EC63.** **Sem.: 6th**

## Course Coordinator:

## Prof. S. S. Kamate

# Module - 3
# Scaling and Subsystem design process

# Module 3

- **Scaling of MOS Circuits**: Scaling Models & Scaling Factors for Device Parameters

- **Subsystem Design Processes:** Some General considerations, An illustration of Design Processes,

- **Illustration of the Design Processes**- Regularity, Design of an ALU Subsystem, The Manchester Carry-chain and Adder Enhancement Techniques
- (5.1, 5.2, 7.1, 7.2, 8.2, 8.3, 8.4.1, 8.4.2 of TEXT 1).

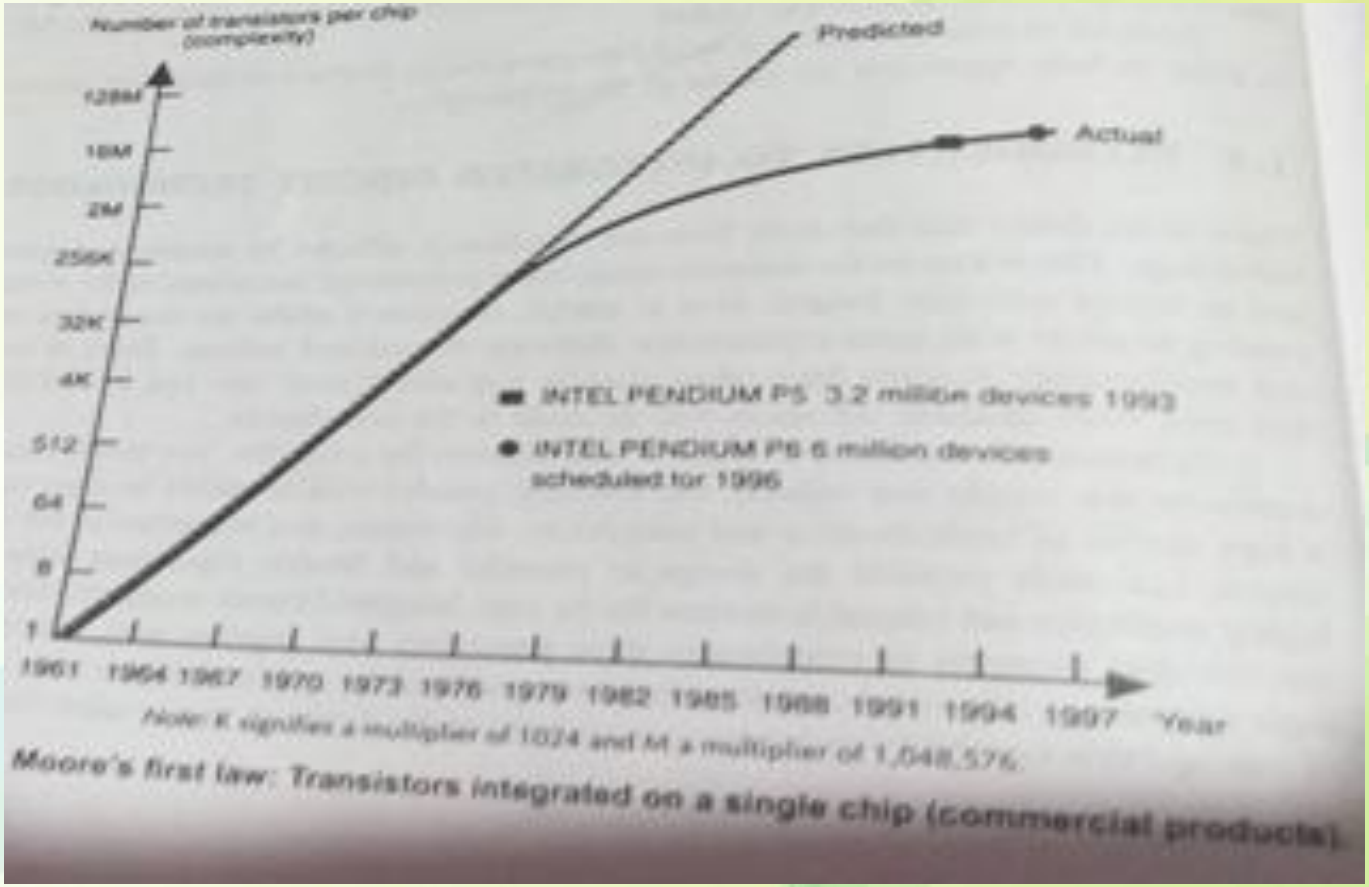
# **Scaling of MOS Circuits**:

Scaling Models & Scaling Factors for Device Parameters**:**

Moore's Law : Gordon Moore of Intel in 1960s has predicted regarding the rapid growth in the number of transistors.

The prediction says that number of transistors on the chip would double after every two years or 18 months

# Moore’s law


Number of transistors per chip (complexity)
128M
16M
2M
256K
32K
4K
512
64
8
1
Predicted
Actual
INTEL PENDIUM P5 3.2 million devices 1993
INTEL PENDIUM P6 6 million devices scheduled for 1996
1961 1964 1967 1970 1973 1976 1979 1982 1985 1988 1991 1994 1997
Year
Note: K signifies a multiplier of 1024 and M a multiplier of 1,048,576.
Moore's first law: Transistors integrated on a single chip (commercial products).

# Comparison of Technologies

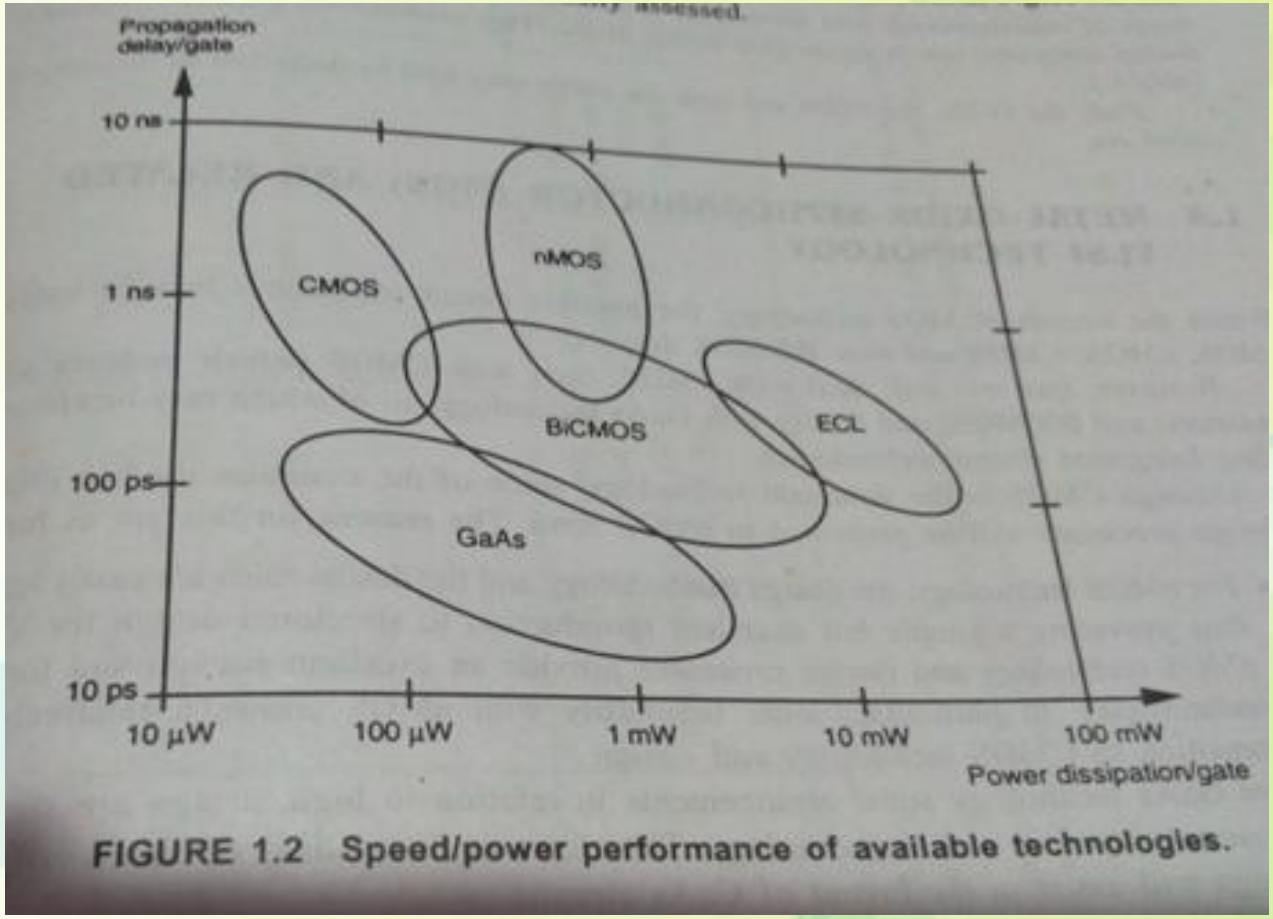
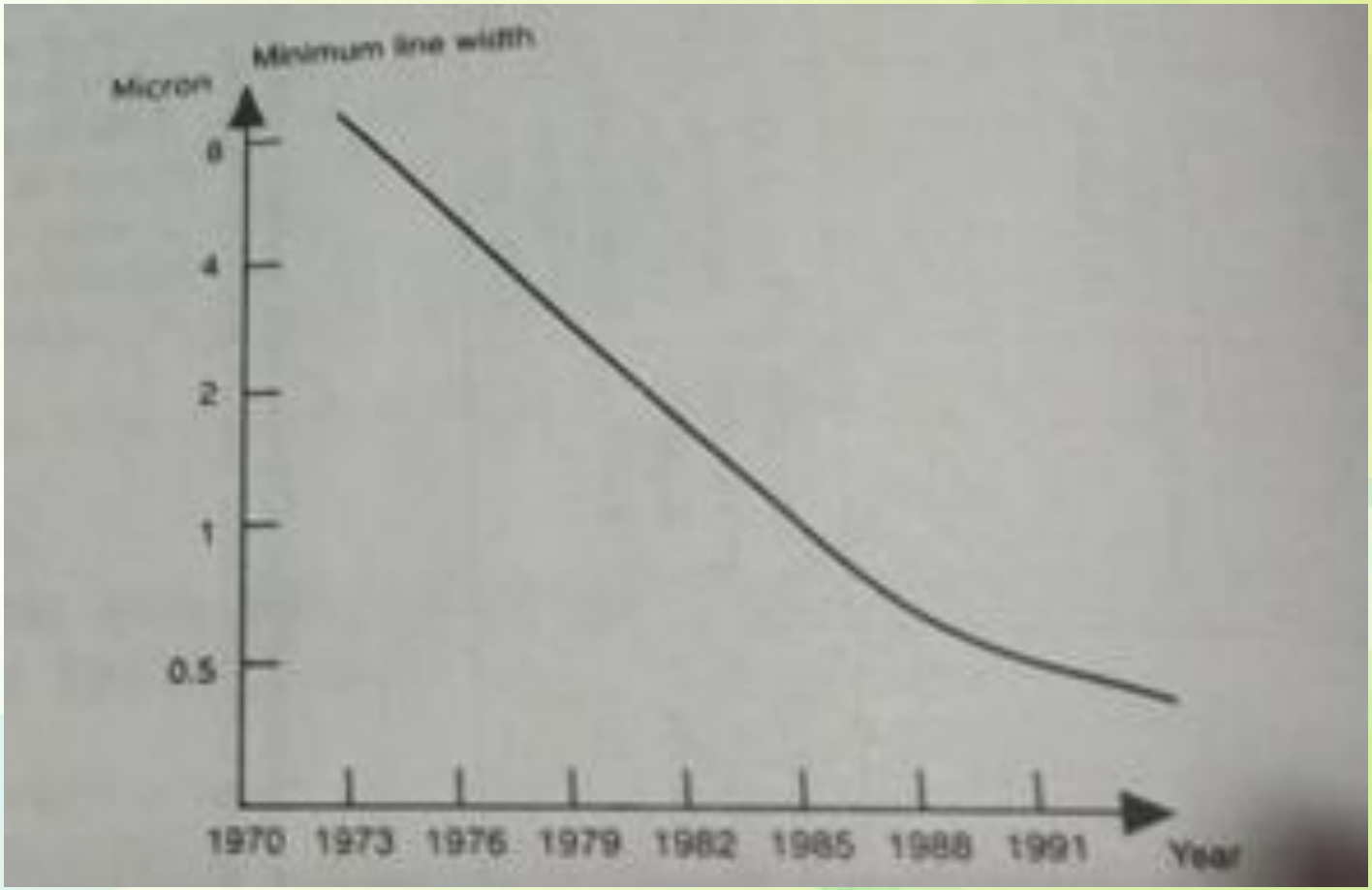



FIGURE 1.2 Speed/power performance of available technologies.

# Channel Length variation



## 1.8.3 Comparison between CMOS, Bipolar and GaAs Technology

| Sr. No. | Parameter | CMOS Technology | Bipolar Technology | GaAs Technology |
|---|---|---|---|---|
| 1. | Static power dissipation | Low | High | Medium |
| 2. | Input impedance | High | Low | High |
| 3. | Noise margin | High | Medium | Low |
| 4. | Voltage swing | High | Low | Low |
| 5. | Operating speed | Medium | High | Very high |
| 6. | Package density | High | Low | High |
| 7. | Output drive current | Low | High | Low |
| 8. | Directional capability | Bidirectional | Unidirectional | Bidirectional |
| 9. | Suitability for switching | Ideal device | Not ideal device | Reasonable device |
| 10. | Mask levels | 12 to 16 | 12 to 20 | 6 to 10 |

# Scaling

- The process of reducing the horizontal and vertical dimension of the transistor is called Scaling.
- The device is scaled by a factor S, This S is quantity grates than 1.
- There are two types of Scaling techniques
  1. Constant Field Scaling
  2. Constant Voltage scaling

Two scaling factors $1/\alpha$ and $1/\beta$ are used.

$1/\beta$ is the scaling factor for supply voltage and gate oxide thickness

- 1/α scaling factor for linear dimensions both horizontal and vertical dimensions.
- For Constant Field Scaling $\beta = \alpha$
- Constant Voltage scaling $\beta = 1$

1. Gate area Ag = LW

2. Gate Capacitance per unit Area Co or Cox

   Co = εox /D

3. Gate Capacitance Cg

   Cg = CoWL

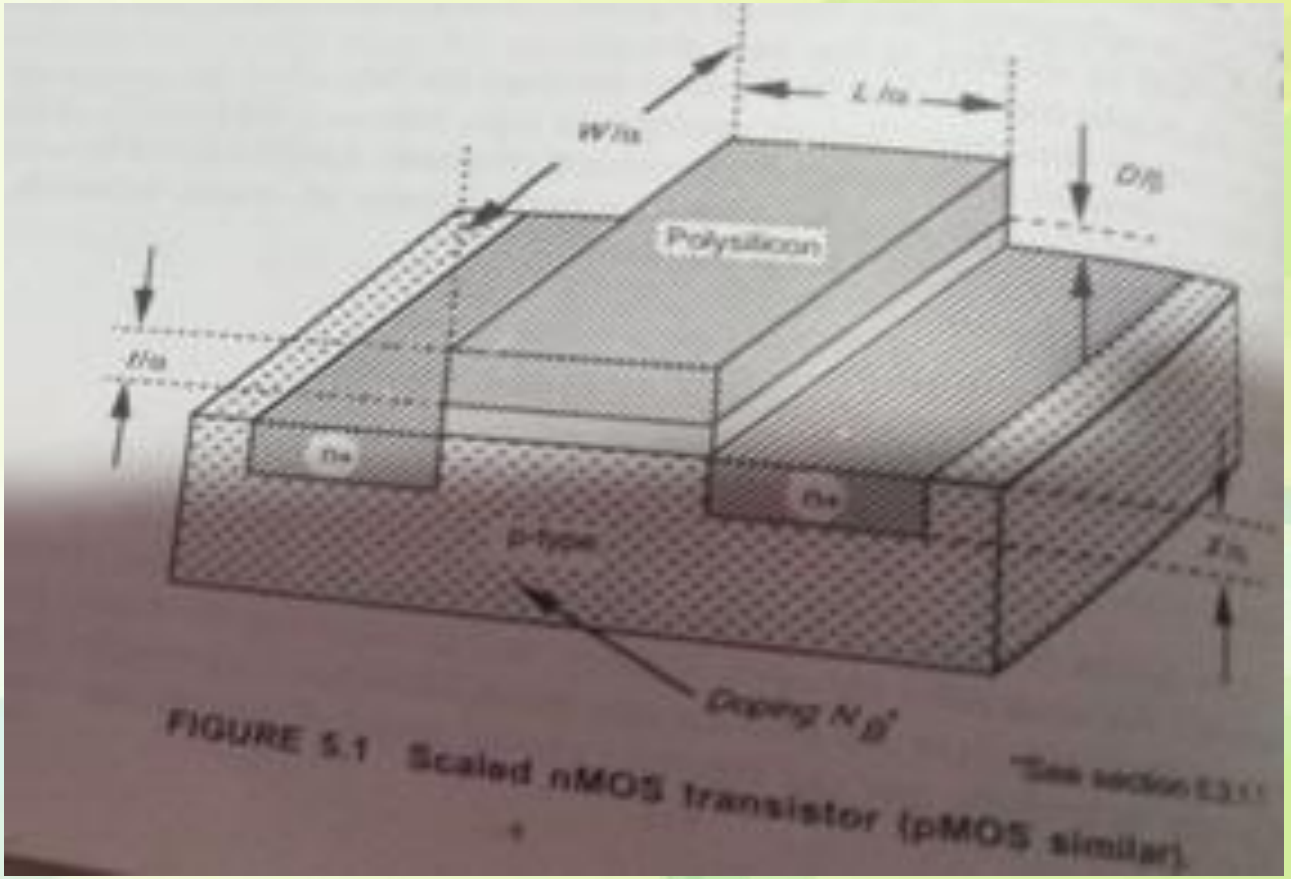
4. Parasitic Capacitance

   Ax/d

d width of depletion region

Ax is the area of the depletion region $1/\alpha^2$

# Cross-sectional view of MOSFET



# Contd…

5. **Carrier density in channel Qon**

$$Qon = Co\ Vgs$$

6. **Channel Resistance Ron**

$$Ron = L/W$$

7. **Gate Delay Td**

$$Td = Ron\ Cg$$

8. **Max. operationg Frequency**

$$Fo = W/L\ uCoVDD/Cg$$

9. **Saturation Current**

$$Idss = Cou/2W/L(Vgs - Vt)^2$$

10. **Current density J**

$$J = Idss/A$$

11. **Switching Energy per gate**

$$Eg = \tfrac{1}{2}\ cg\ Vdd^2$$

# Contd…

12.Power Dissipation per gate Pg

$Pg = Pgs + Pgd$

$Pgs = Vdd^2/Ron$

$Pgd = Egfo$

13.Power dissipation per unit Area

$Pa = Pg/Ag$

14. Power Speed Product $P_T$

$PT = PgTd$

mentioned earlier.

TABLE 5.1 Scaling effects

| Parameters | | Combined V and D | Constant E | Constant V |
|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | $1/\beta$ | $1/\alpha$ | 1 |
| $L$ | Channel length | $1/\alpha$ | $1/\alpha$ | $1/\alpha$ |
| $W$ | Channel width | $1/\alpha$ | $1/\alpha$ | $1/\alpha$ |
| $D$ | Gate oxide thickness | $1/\beta$ | $1/\alpha$ | 1 |
| $A_g$ | Gate area | $1/\alpha^2$ | $1/\alpha^2$ | $1/\alpha^2$ |
| $C_{ox}$ (or $C_{ox}$) | Gate C per unit area | $\beta$ | $\alpha$ | 1 |
| $C_g$ | Gate capacitance | $\beta/\alpha^2$ | $1/\alpha$ | $1/\alpha^2$ |
| $C_s$ | Parasitic capacitance | $1/\alpha$ | $1/\alpha$ | $1/\alpha$ |
| $Q_{inv}$ | Carrier density | 1 | 1 | 1 |
| $R_{on}$ | Channel resistance | 1 | 1 | 1 |
| $I_{dss}$ | Saturation current | $1/\beta$ | $1/\alpha$ | 1 |
| $A_c$ | Conductor X-section area | $1/\alpha^2$ | $1/\alpha$ | 1 |
| $I$ | Current density | $\alpha^2/\beta$ | $1/\alpha^2$ | $1/\alpha^2$ |
| $V_d$ | Logic 1 level | $1/\beta$ | $\alpha$ | $\alpha^2$ |
| $E_d$ | Switching energy | $1/\alpha^2\beta$ | $1/\alpha$ | 1 |
| $P_d$ | Power dissn per gate | $1/\beta^2$ | $1/\alpha^3$ | $1/\alpha^2$ |
| $N$ | Gates per unit area | $\alpha^2$ | $1/\alpha^2$ | 1 |
| $P_a$ | Power dissn per unit area | $\alpha^2/\beta^2$ | $\alpha^2$ | $\alpha^2$ |
| $T_d$ | Gate delay | $\beta/\alpha^2$ | 1 | $\alpha^2$ |
| $f_0$ | Max. operating frequency | $\alpha^2/\beta$ | $1/\alpha$ | $1/\alpha^3$ |
| $P_T$ | Power-speed product | $1/\alpha^2\beta$ | $\alpha$ | $\alpha^2$ |
| | | | $1/\alpha^3$ | $1/\alpha^2$ |

Constant E: $\beta = \alpha$; Constant V: $\beta = 1$

# Queries ...?