Department of Electronics & Communication Engg.

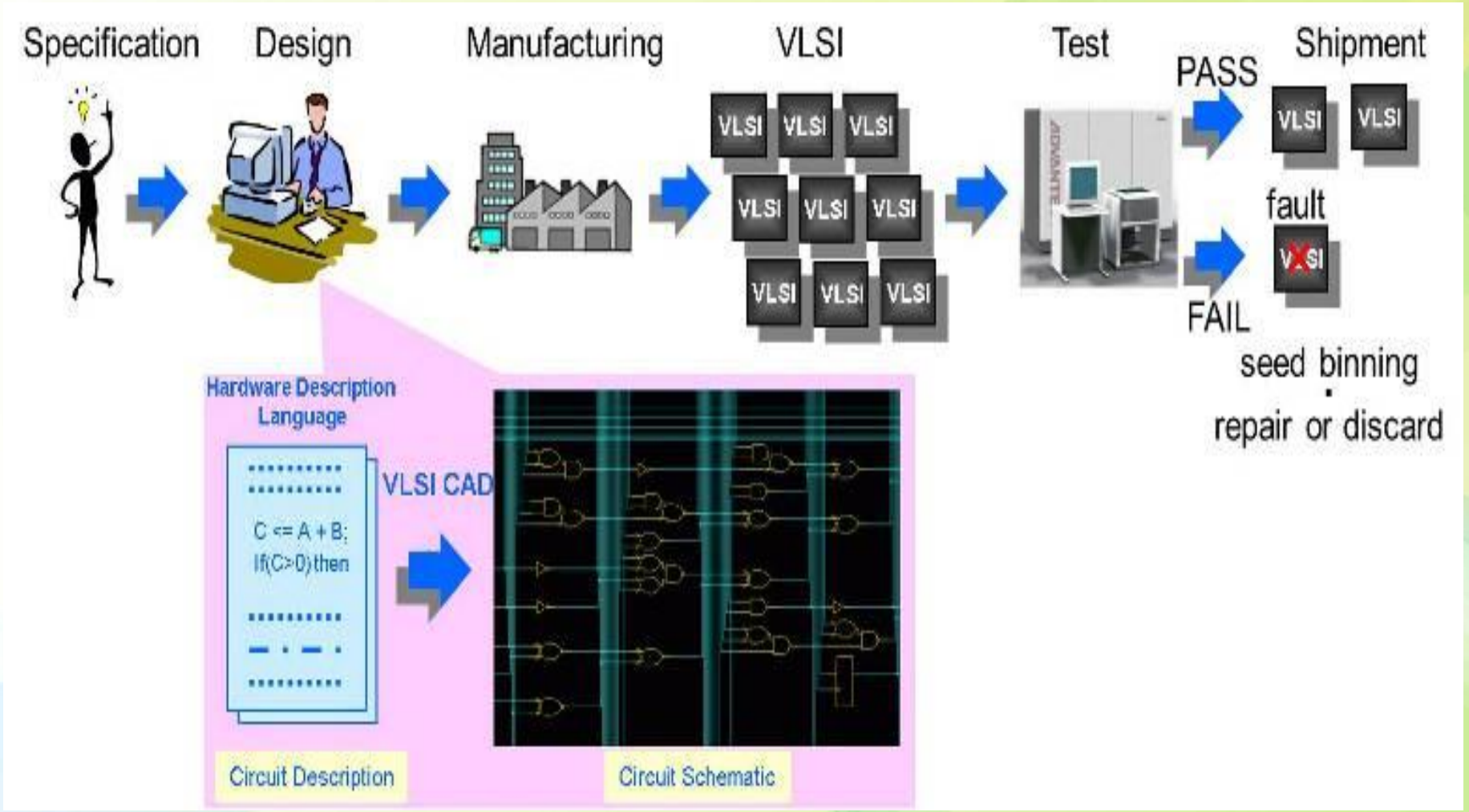
Course : VLSI DESIGN-15EC63. **Sem.: 6th**

Course Coordinator:

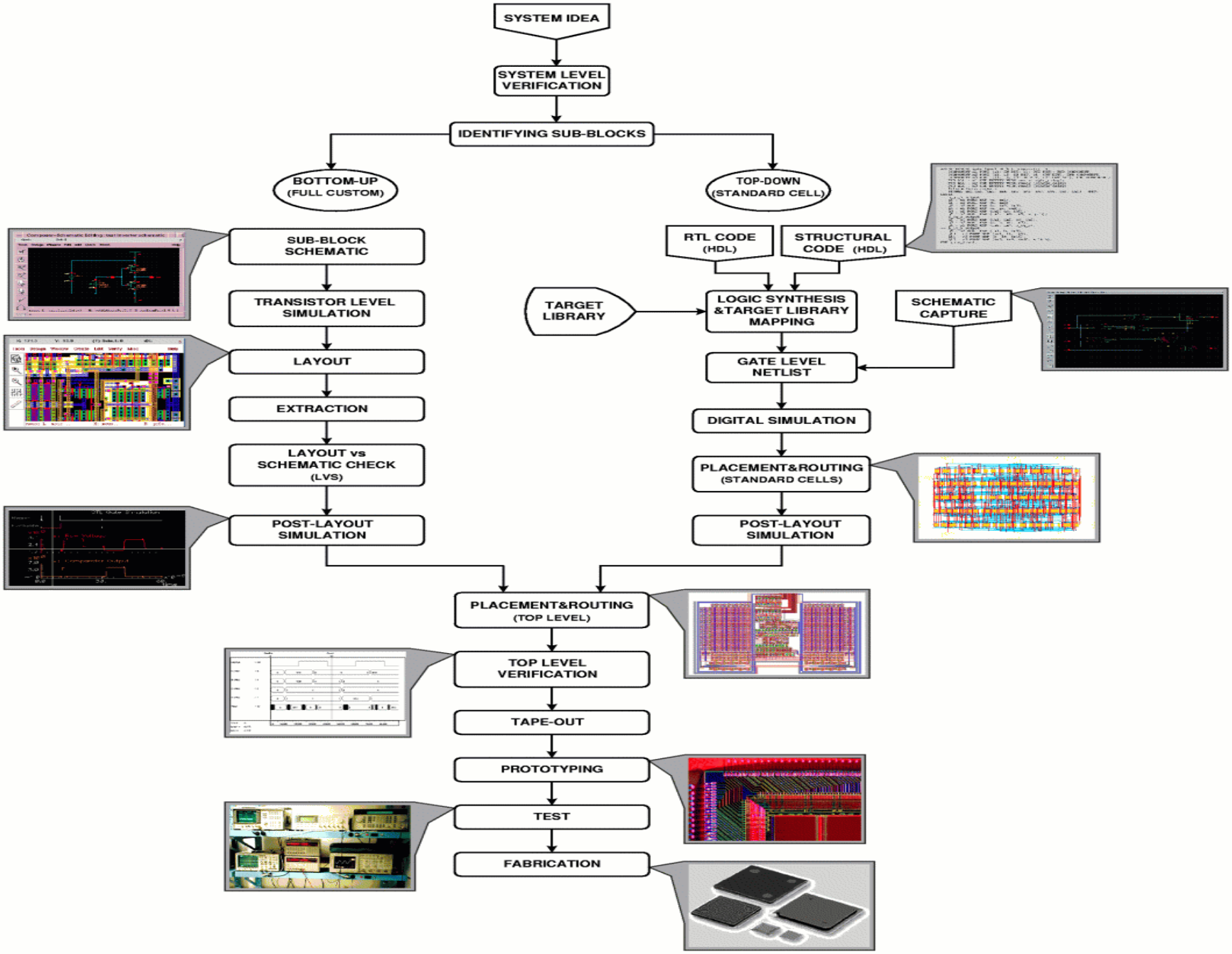
Prof. S. S. Kamate

Module 2

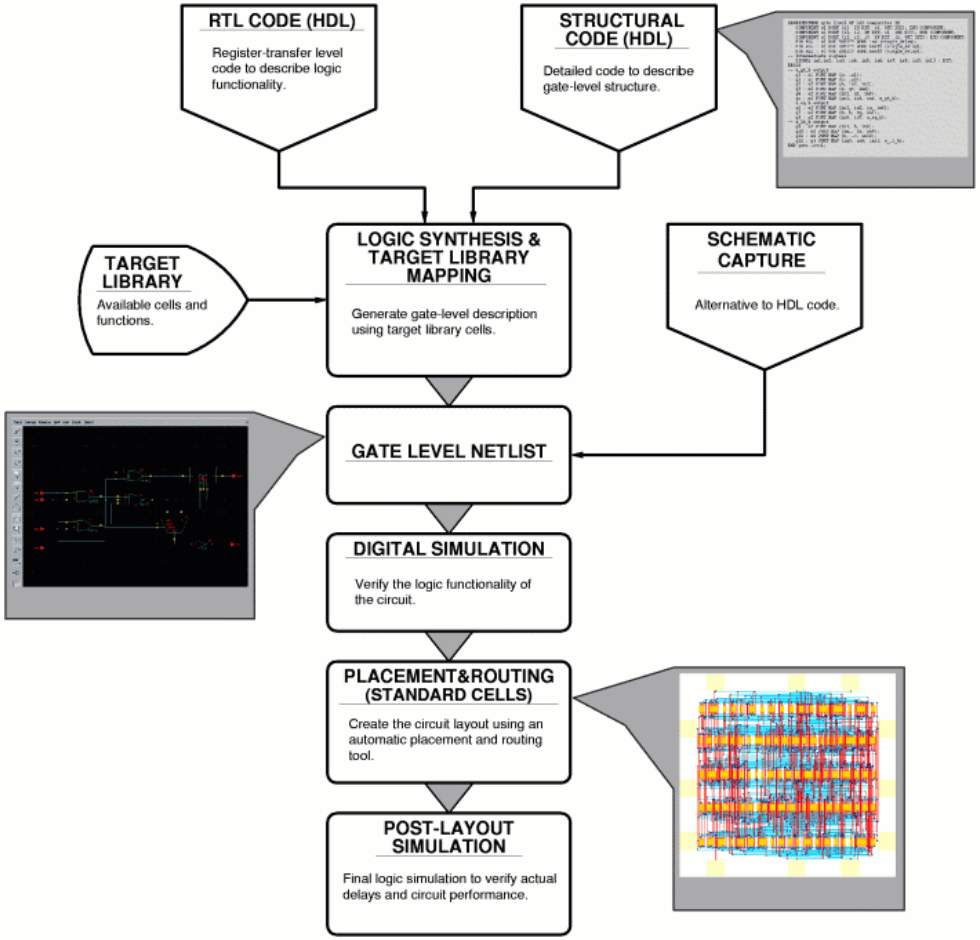
CIRCUIT DESIGN PROCESSES


Specification
Design
Manufacturing
VLSI
Test
Shipment
PASS
FAIL
fault
seed binning
repair or discard
Hardware Description Language
C <= A + B;
If(C>0)then
VLSI CAD
Circuit Description
Circuit Schematic

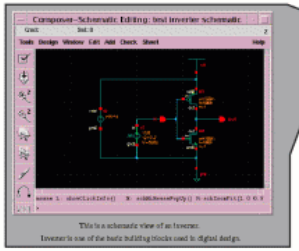
VLSI DESIGN FLOW



TOP-DOWN (STANDARD CELL) DESIGN METHODOLOGY



BOTTOM-UP
(FULL CUSTOM)
DESIGN METHODOLOGY



SUB-BLOCK SCHEMATIC

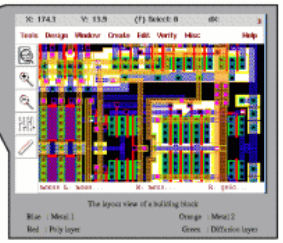
Transistor-level schematic drawings of the circuit blocks are created in Schematic Editor.

TRANSISTOR LEVEL SIMULATION

SPICE(or equivalent) simulation of circuit blocks is used to verify their functionality.

LAYOUT

Mask-layout of all circuit blocks are created in Layout Editor.

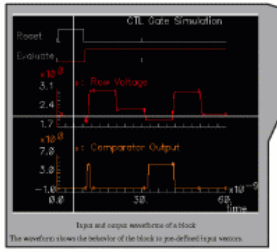


EXTRACTION

Actual device dimensions and parasitic parameters are determined from mask layout.

LAYOUT vs SCHEMATIC CHECK (LVS)

Automatic comparison of mask layout and circuit schematic.



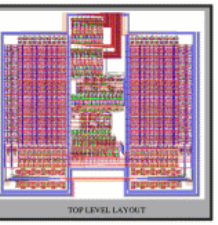
POST-LAYOUT SIMULATION

Final SPICE simulation of the circuit of the circuit blocks using extracted parameters.

FROM MASK LAYOUT TO FABRICATED CHIP

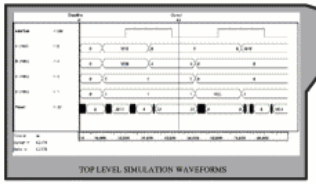
PLACEMENT&ROUTING (TOP LEVEL)

Mask level layout of the entire chip



TOP LEVEL VERIFICATION

Simulation (mixed-mode) to verify functionality and performance of the entire chip.

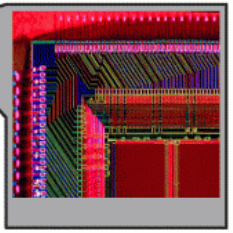


TAPE-OUT

Create universal format file to describe mask layers to manufacturer.

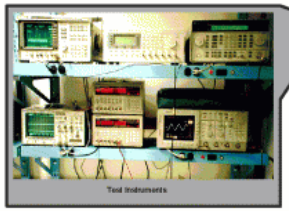
PROTOTYPING

Sample chips manufactured in fab.



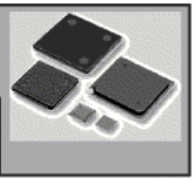
TEST

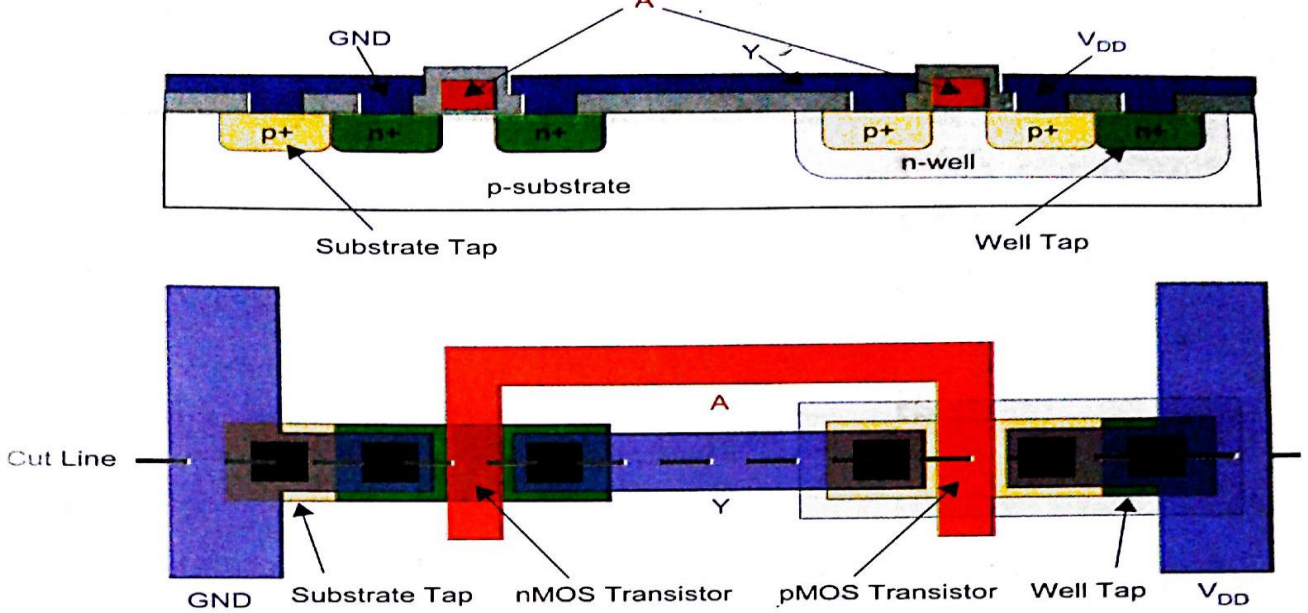
Performance verification and debugging of the prototype.



FABRICATION

Mass-production of the designed chip.





Figs 1.34–1.35(a) Inverter Cross-Section and Top View

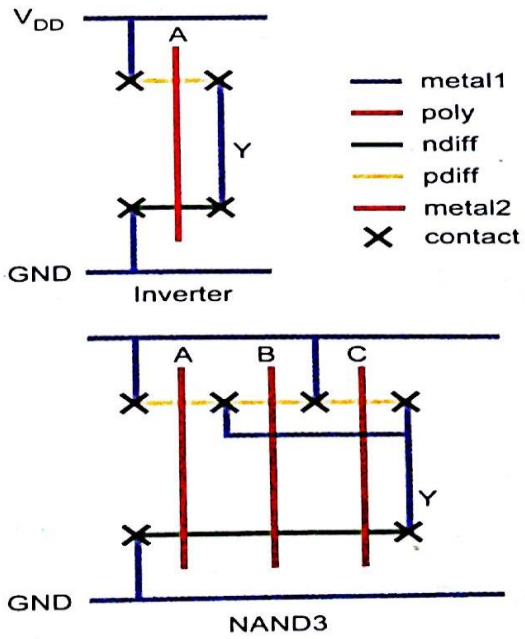


Fig 1.43 Stick Diagrams

✓MOS designs are used for making masks for fabrication.

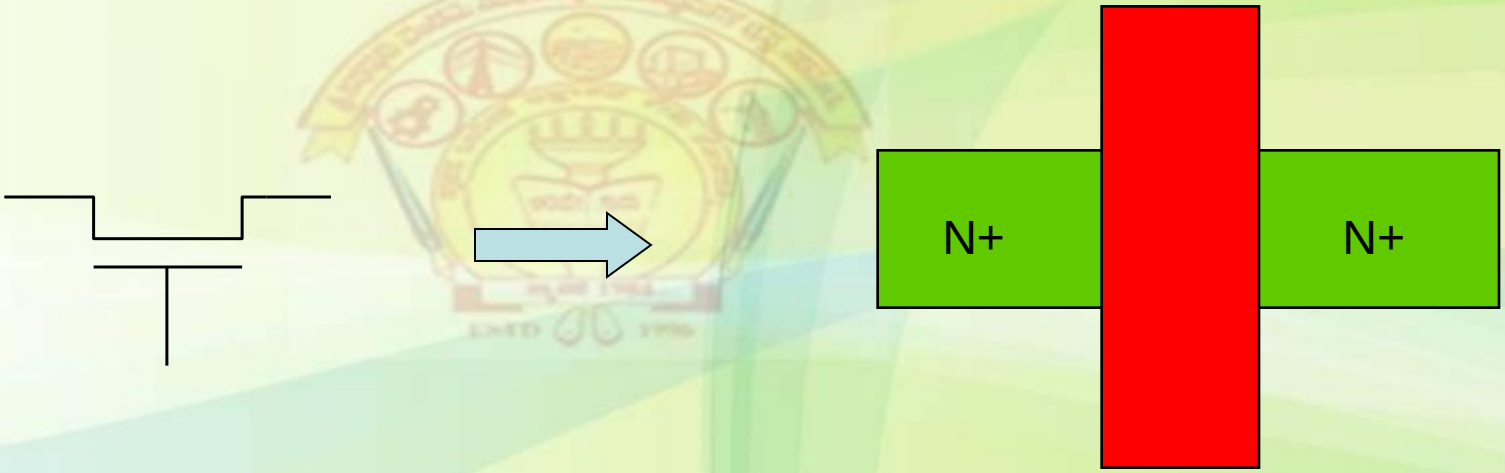
✓MOS circuits consists of four basic layers

n-diffusion
p-diffusion
polysilicon
metal

✓Stick diagram hides lower level circuit details and electrical parameters such as **current, speed and noise,** but comes one step closer to actual layout.

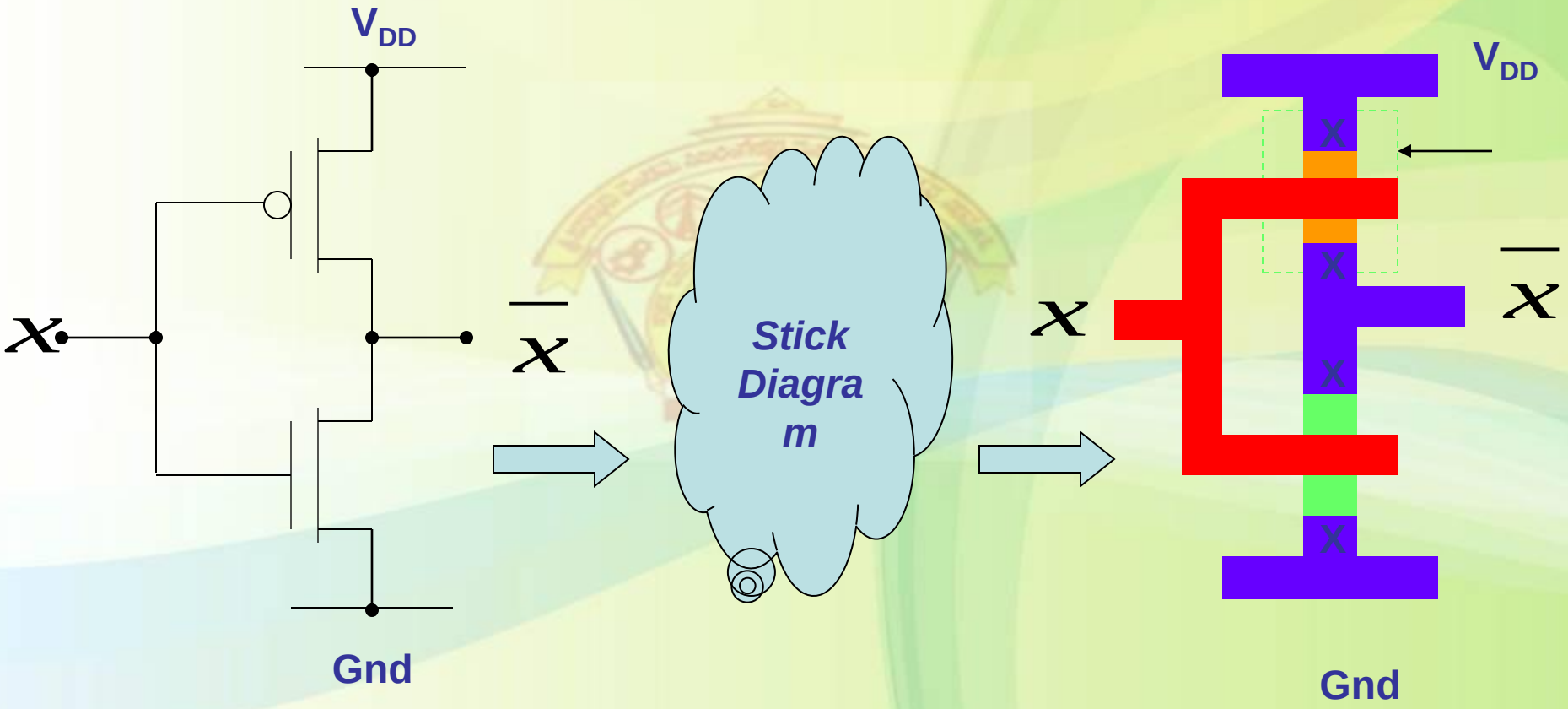
✓One of the fundamental difficulties in specifying design rules is that the fabrication processes are undergoing rapid evolutionary changes.

Stick Diagrams

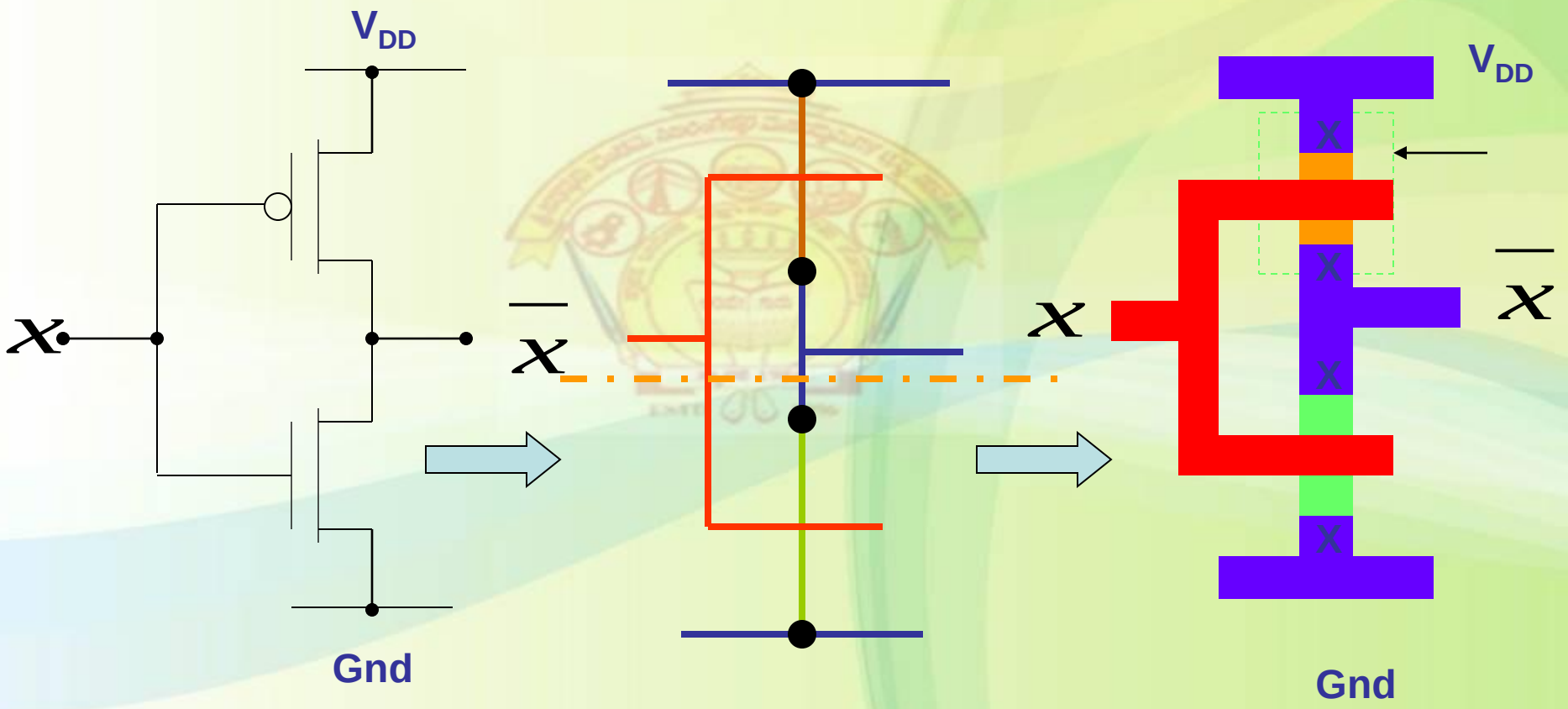


Stick diagram are used to convey layer information through the use of color code

Stick Diagrams



Stick Diagrams



Stick Diagrams

- VLSI design aims to translate circuit concepts onto silicon.
- stick diagrams are a means of capturing topography and layer information using simple diagrams.
- Stick diagrams convey layer information through colour codes (or monochrome encoding).
- Acts as an interface between symbolic circuit and the actual layout.

Stick Diagrams

- Does show all components/vias.
- It shows relative placement of components.
- Goes one step closer to the layout
- Helps plan the layout and routing

A stick diagram is a cartoon of a layout.

Stick Diagrams

- Does ***not*** show
  - Exact placement of components
  - Transistor sizes
  - Wire lengths, wire widths, tub boundaries.
  - Any other low level details such as parasitics..

Stick Diagrams

- Does ***not*** show
  - Exact placement of components
  - Transistor sizes
  - Wire lengths, wire widths, tub boundaries.
  - Any other low level details such as parasitics..

Stick Diagrams – Notations

Can also draw in shades of gray/line style.

Similarly for contacts, via, tub etc..

Stick Diagrams – Some rules

Rule 1.

When two or more ‘sticks’ of the same type cross or touch each other that represents electrical contact.

Stick Diagrams – Some rules

Rule 2.

When two or more ‘sticks’ of different type cross or touch each other there is no electrical contact.

(If electrical contact is needed we have to show the connection explicitly).

Stick Diagrams – Some rules

Rule 3.

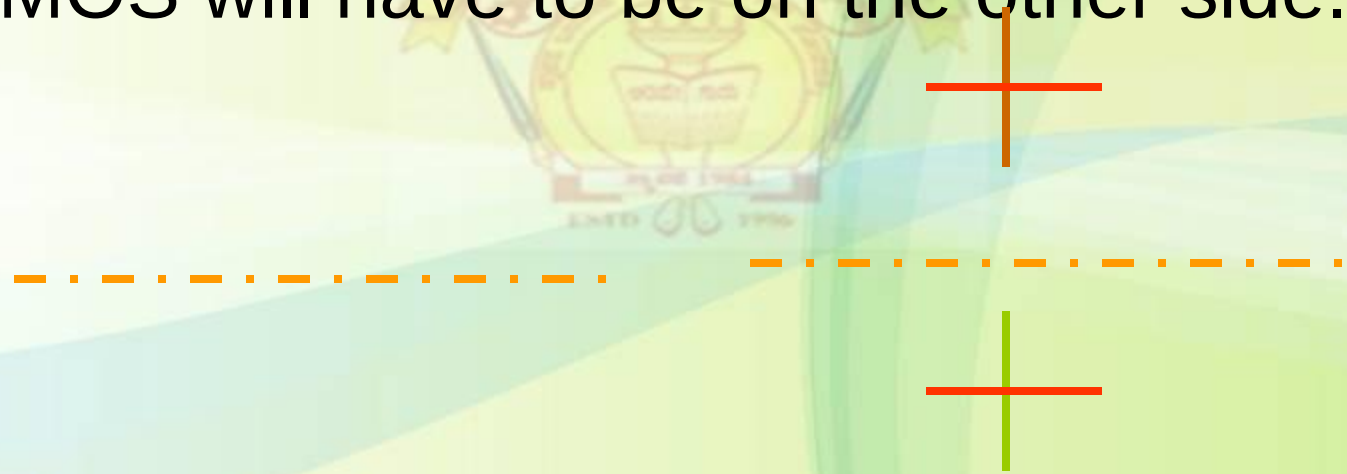
When a poly crosses diffusion it represents a transistor.

Note: If a contact is shown then it is ***not*** a transistor.

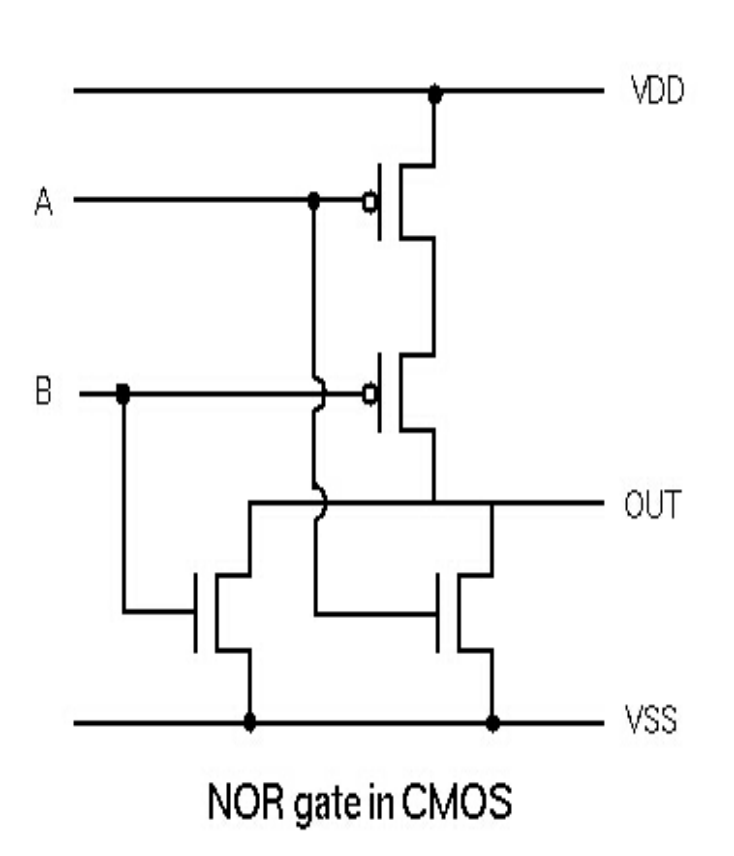
Stick Diagrams – Some rules

Rule 4.

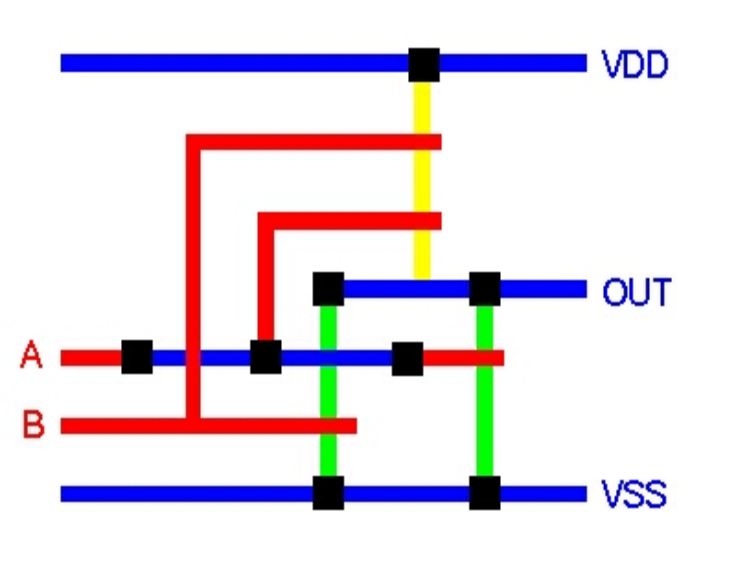
In CMOS a demarcation line is drawn to avoid touching of p-diff with n-diff. All pMOS must lie on one side of the line and all nMOS will have to be on the other side.



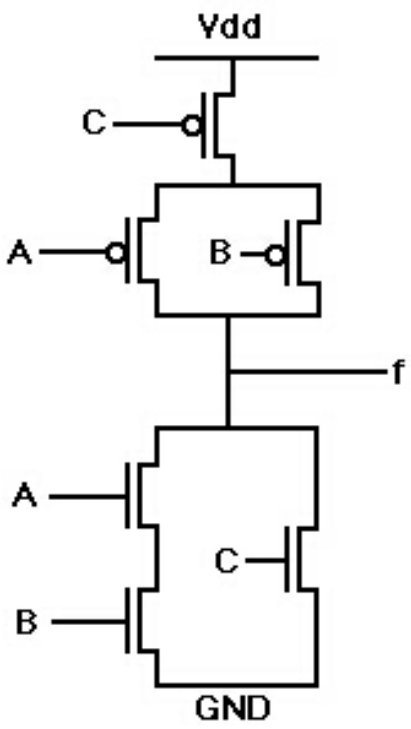
How to draw Stick Diagrams

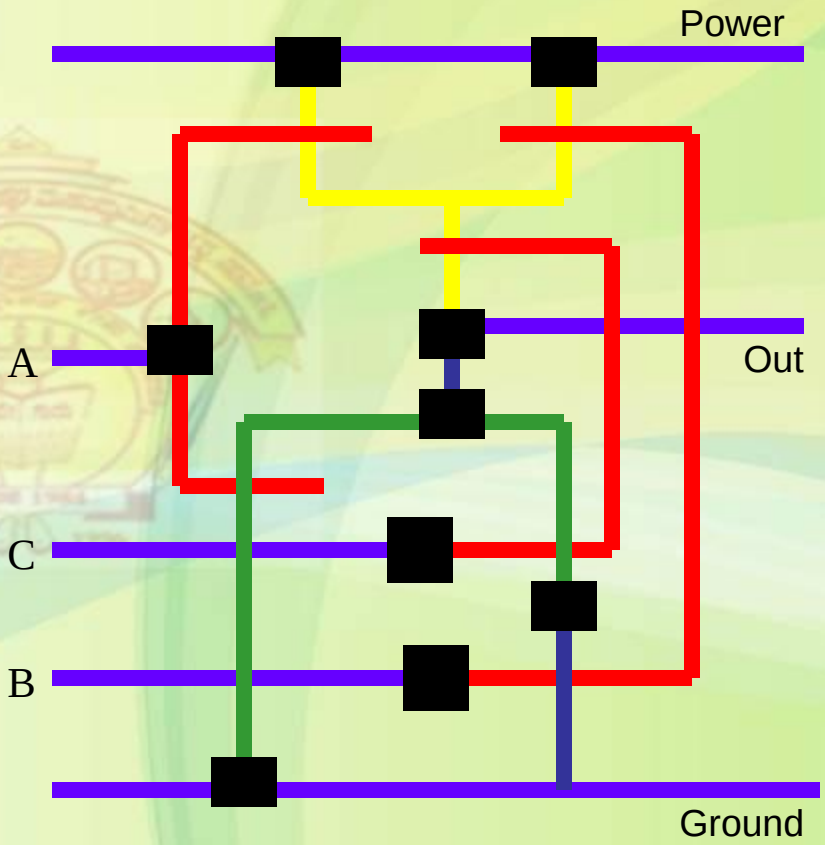


NOR gate in CMOS



Example: $f = \overline{(A \bullet B) + C}$





Stick Diagrams

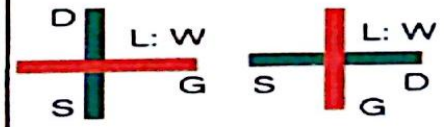
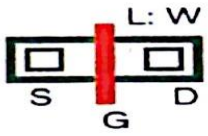
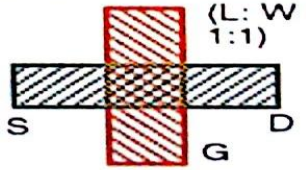
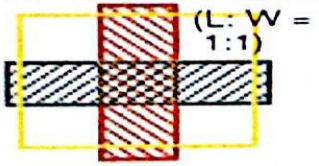
- Summary:
  - What is stick diagram?
  - Why stick diagram?
  - Conventions and rules related to stick diagram.
  - Drawing stick diagrams.

Stick Diagrams

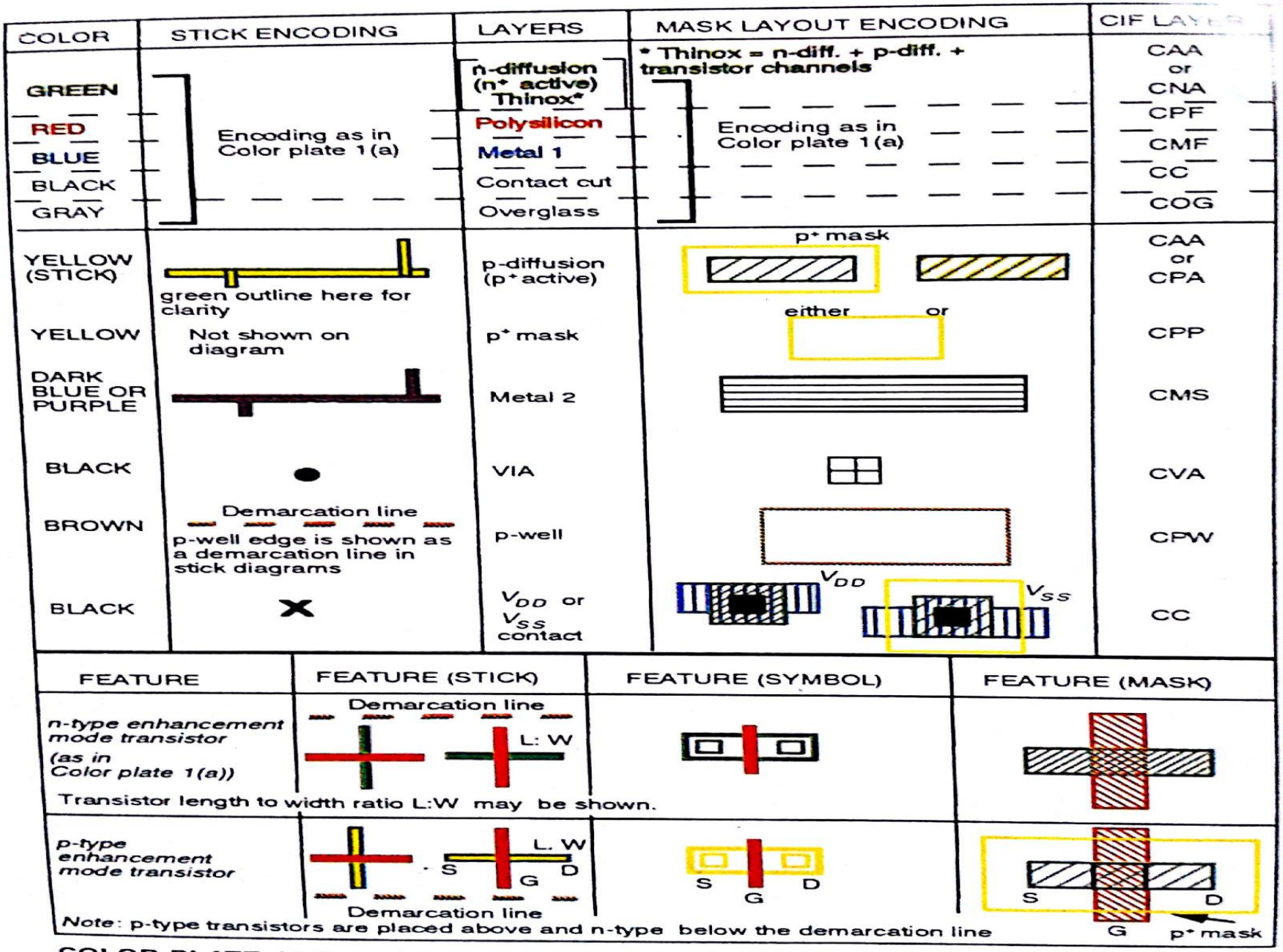
- Home work:
  1. Draw the stick diagram for two input CMOS NAND gate.
  2. Draw the stick diagram for two input NAND gate using NMOS Logic.
  3. Draw the stick diagram for 2:1 MUX using
     a) Pass transistors
     b) Transmission gates.

Drawing stick diagram is truly Fun!!. Enjoy it.

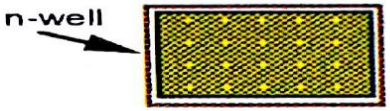
COLOR	STICK ENCODING	LAYERS	MASK LAYOUT ENCODING	CIF LAYER
GREEN		n-diffusion (n+ active) Thinox*	 *Thinox = n-diff. + transistor channels	ND
RED		Polysilicon		NP
BLUE		Metal 1		NM
BLACK		Contact cut		NC
GRAY	NOT APPLICABLE	Overglass		NG
nMOS ONLY YELLOW		Implant		NI
nMOS ONLY BROWN		Buried contact		NB

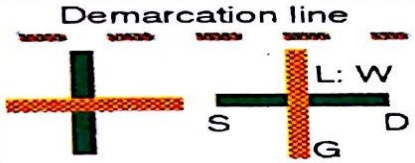
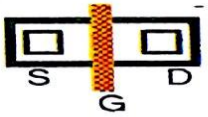
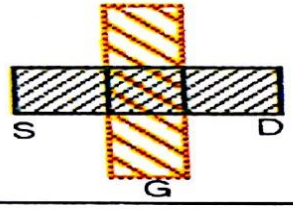
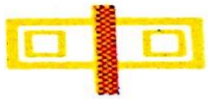
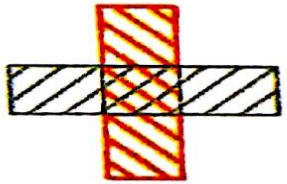
FEATURE	FEATURE (STICK)	FEATURE (SYMBOL)	FEATURE (MASK)
n-type enhancement mode transistor			
Transistor length to width ratio L: W should be shown.			
n-type depletion mode transistor nMOS only			
Source, drain and gate labelling will not normally be shown.			

COLOR PLATE 1(a) **Encodings for a simple single metal nMOS process. (See Figure 3.1(a) for nMOS monochrome encoding details.)**

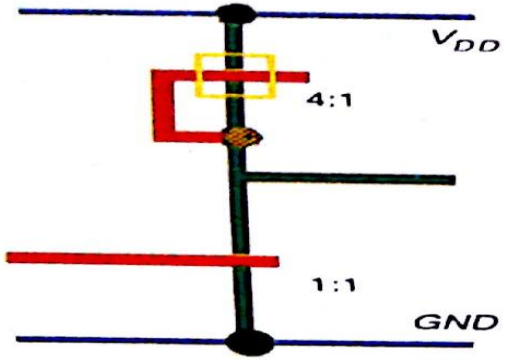


COLOR PLATE 1(b) **Color encodings for a double metal CMOS p-well process. The same well encoding and demarcation line is used for an n-well process. For a p-well process, the n features are in the well. For an n-well process, the p features are in the well. (See Figure 3.1(b) for CMOS monochrome encoding details.)**

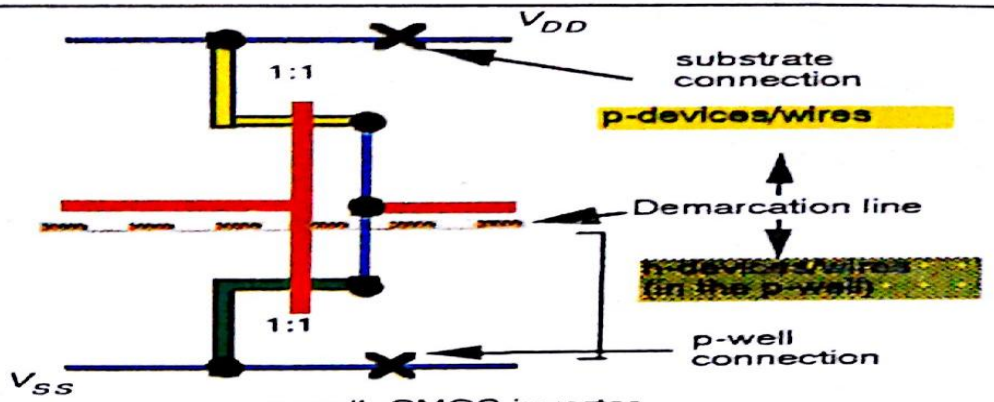
COLOR	STICK ENCODING	LAYERS	MASK LAYOUT ENCODING	CIF LAYER
ORANGE		Polysilicon 2		CPS
		Bipolar npn transistor	See Color plate 6 also Figure 3.13(f)	Not applicable
PINK	Not separately encoded	p-base of bipolar npn transistor		CBA
PALE GREEN	Not separately encoded	Buried collector of bipolar npn transistor		CCA

FEATURE	FEATURE (STICK)	FEATURE (SYMBOL)	FEATURE (MASK)
n-type enhancement poly. 2 transistor.			
Transistor length to width ratio L: W may be shown.			
p-type enhancement poly. 2 transistor			
Note: p-type transistors are placed above and n-type below the demarcation line			
npn bipolar transistor			See Figure 3.13(f) and Color plate 6

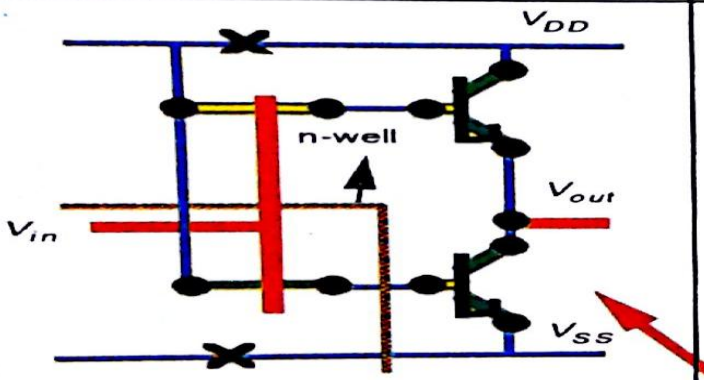
COLOR PLATE 1(c) **Additional encodings for a double metal double poly. BiCMOS n-well process. The same well encoding and demarcation line as in Figure 3.1(b) is used for an n-well process. For a p-well process, the n features are in the well. (See Color plate 6 for additional BiCMOS color encoding details and see Figure 3.1(c) for more stroke encoding details).**



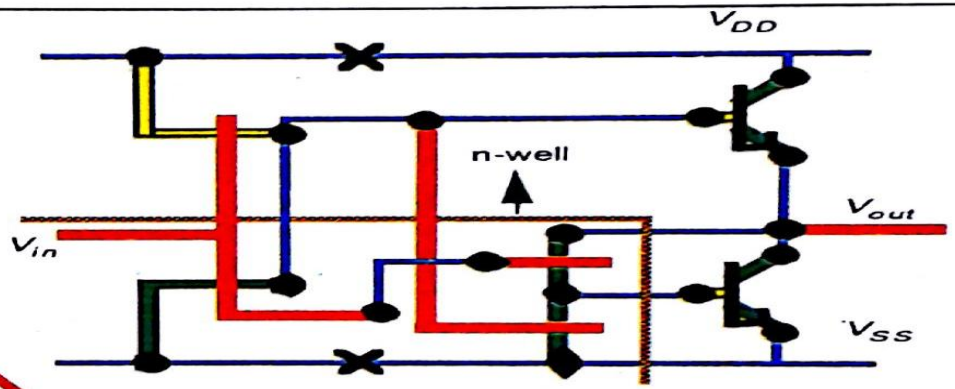
4:1 nMOS inverter



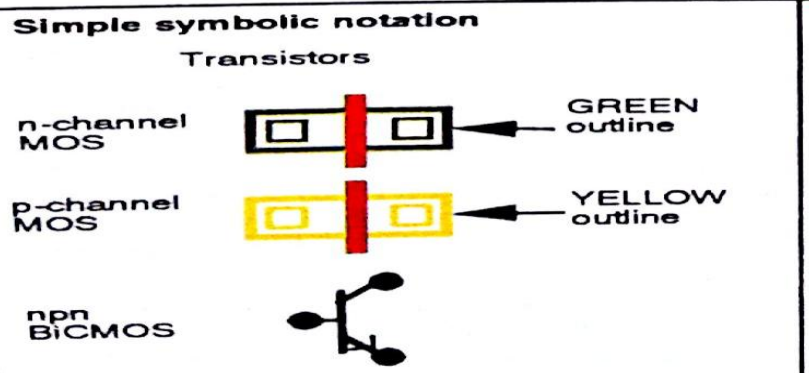
p-well CMOS inverter

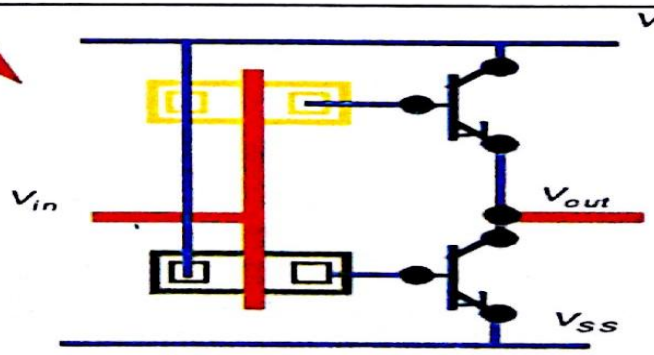


Simple n-well based BiCMOS inverter (stick diagram)



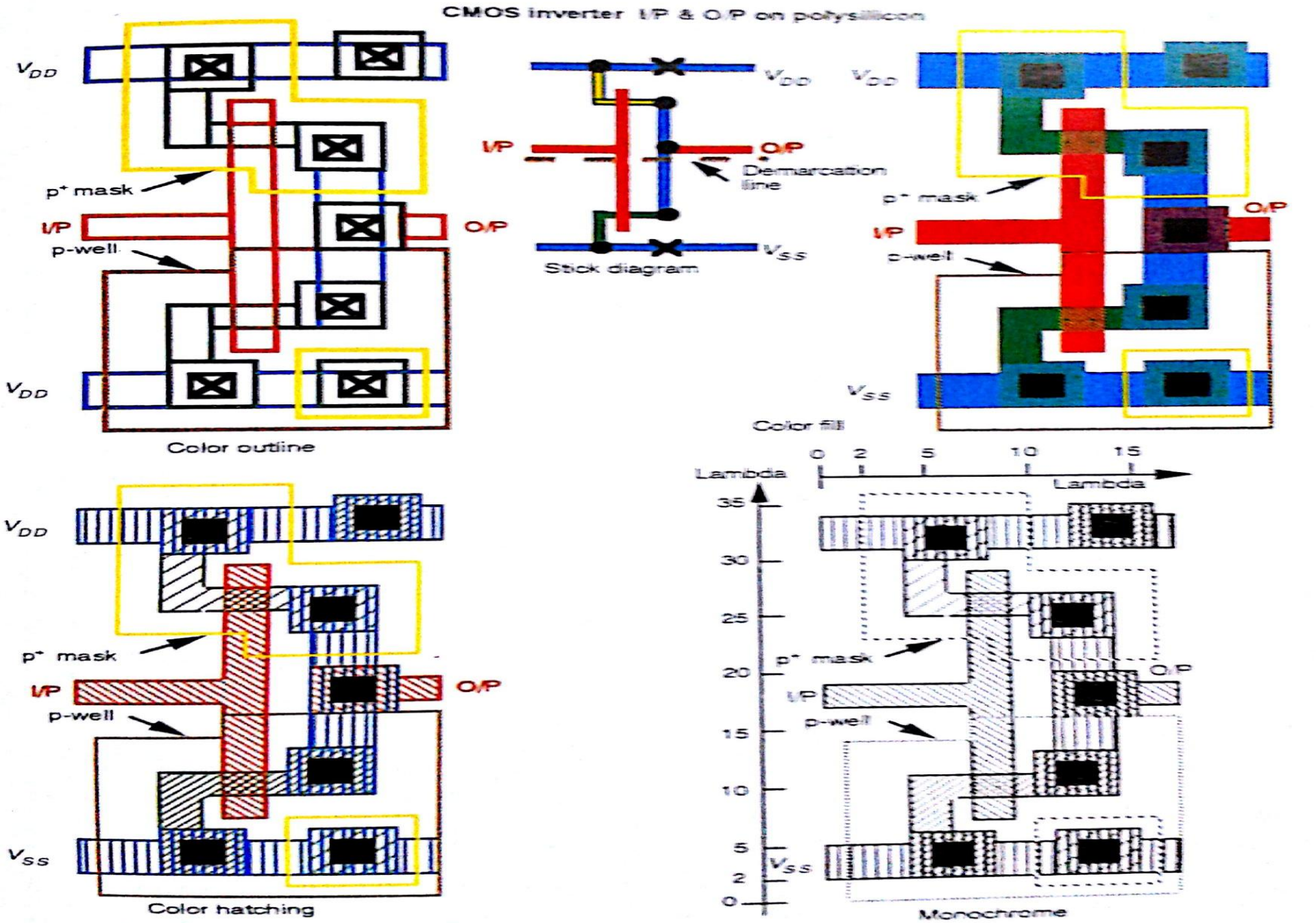
Alternative design for an n-well based BiCMOS inverter





Simple n-well based BiCMOS inverter (symbolic diagram)

COLOR PLATE 1(d) **Color stick diagram examples. (See Figure 3.1(d) monochrome stick diagrams and simple symbolic encoding.)**



COLOR PLATE 2 Example layout encodings.

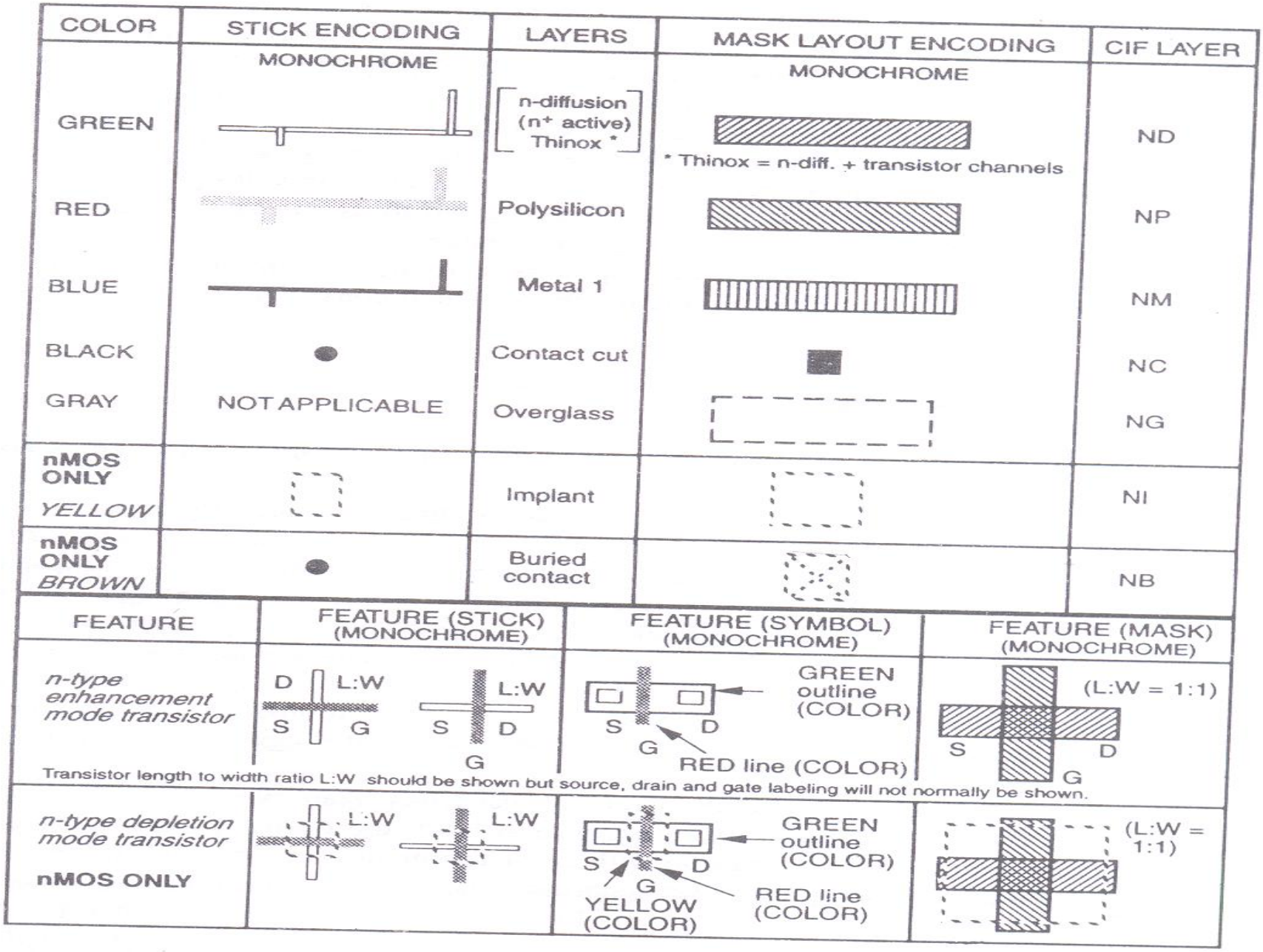
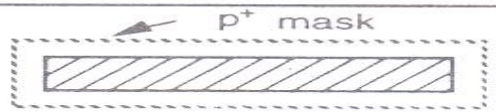
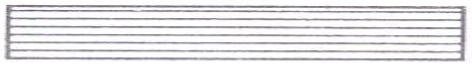
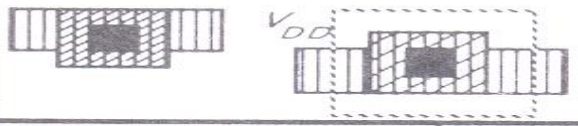
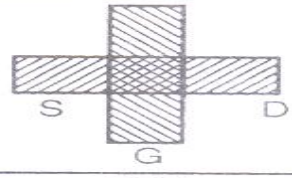
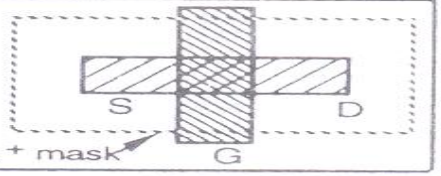


FIGURE 3.1(a) Encodings for a simple metal nMOS process (see Color plate 1(a) for nMOS color encoding details).

COLOR	STICK ENCODING	LAYERS	MASK LAYOUT ENCODING	CIF LAYER
GREEN	MONOCHROME	n-diffusion (n + active) Thinox *	MONOCHROME * Thinox = n-diff. + p-diff.+ transistor channels	CAA or CNA
RED	ENCODING AS IN FIGURE 3–1(a)	Polysilicon	ENCODING AS IN FIGURE 3–1(a)	CPF
BLUE		Metal 1		CMF
BLACK		Contact cut		CC
GRAY		Overglass		COG
GREEN IN P+ (MASK) YELLOW (STICK)		p-diffusion (p + active)		CAA or CPA
YELLOW	NOT SHOWN IN STICK DIAGRAM	p+ mask		CPP
DARK BLUE OR PURPLE		Metal 2		CMS
BLACK		VIA		CVA
BROWN	DEMARCATION LINE p-well edge is shown as a demarcation line in stick diagrams	p-well		CPW
BLACK		V_{DD} or V_{SS} CONTACT		CC

FEATURE	FEATURE (STICK) (MONOCHROME)	FEATURE (SYMBOL) (MONOCHROME)	FEATURE (MASK) (MONOCHROME)
n-type enhancement mode transistor (as in Figure 3–1(a))			
Transistor length to width ratio L:W may be shown.			
p-type enhancement mode transistor			
Note: p-type transistors are placed above and n-type transistors below the demarcation line			

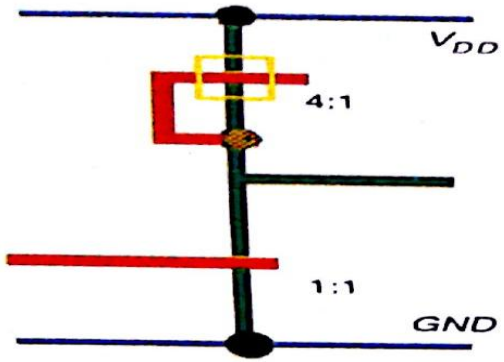
The same well encoding and demarcation line are used for an n-well process.
For p-well process, the n features are in the well. For an n-well process, the p features are in the well.

COLOR	STICK ENCODING	LAYERS	MASK LAYOUT ENCODING	CIF LAYER
	MONOCHROME		MONOCHROME	
ORANGE		Polysilicon 2		CPS
SEE COLOR PLATE 1(c)		Bipolar npn transistor	see Figure 3–13(f)	Not applicable
PINK	Not separately encoded	p-base of bipolar npn transistor		CBA
PALE GREEN	Not separately encoded	Buried collector of bipolar npn transistor	n-well	CCA

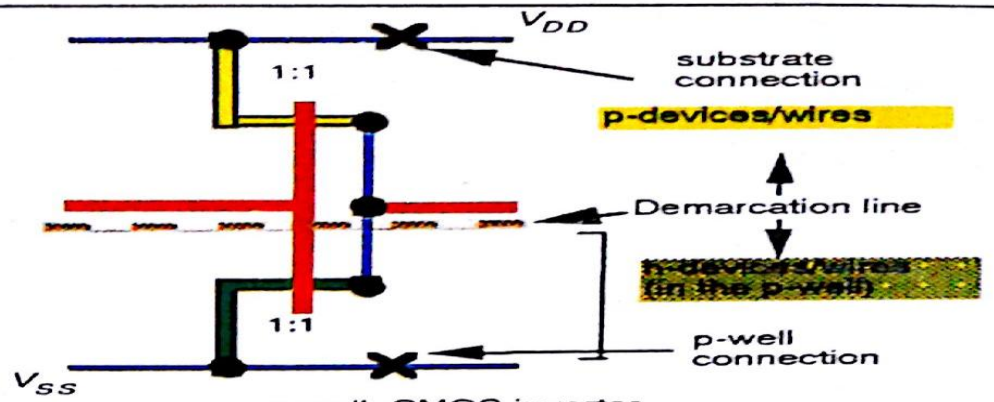
FEATURE	FEATURE (STICK) (MONOCHROME)	FEATURE (SYMBOL) (MONOCHROME)	FEATURE (MASK) (MONOCHROME)
n-type enhancement poly. 2 transistor	DEMARCATION LINE; L:W; S; D; G	GREEN; S; D; G; ORANGE	S; D; G
Transistor length to width ratio L:W may be shown.			
p-type enhancement poly. 2 transistor	L:W; DEMARCATION LINE	YELLOW; ORANGE	
Note: p-type transistors are placed above and n-type transistors below the demarcation line.			
npn bipolar transistor			See Figure 3–13(f) and Color plate 6

The same well encoding and demarcation line as in Figure 3–1(b) are used for an n-well process. For a p-well process, the n features are in the well. For an n-well process, the p features are in the well.

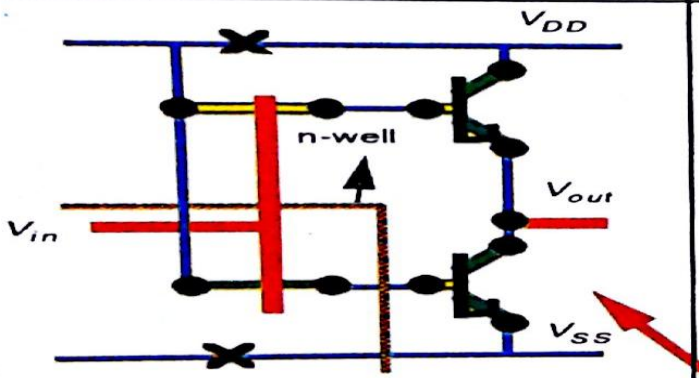
FIGURE 3.1(c) Additional encodings for a double metal double poly. BiCMOS n-well process (see Color plates 1(c) and 6 for additional CMOS and BiCMOS color encoding details).



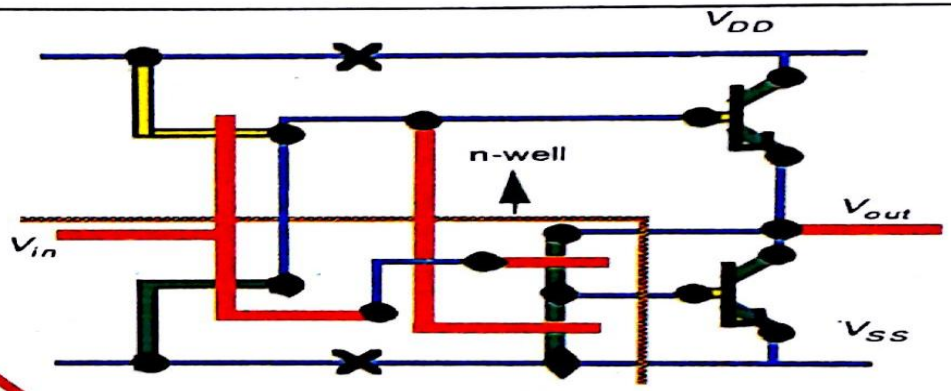
4:1 nMOS inverter



p-well CMOS inverter

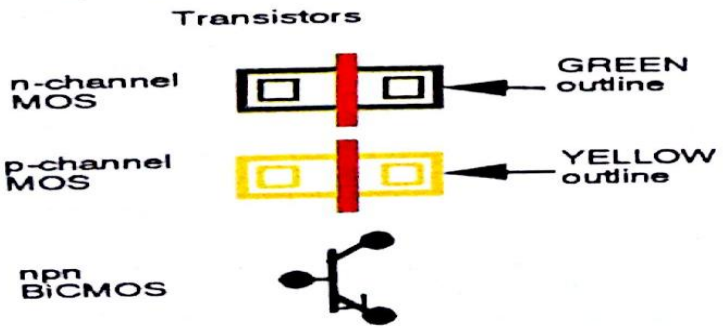


Simple n-well based BiCMOS inverter (stick diagram)

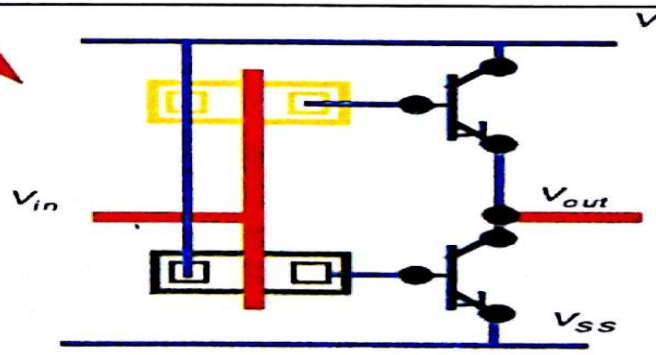


Alternative design for an n-well based BiCMOS inverter

Simple symbolic notation

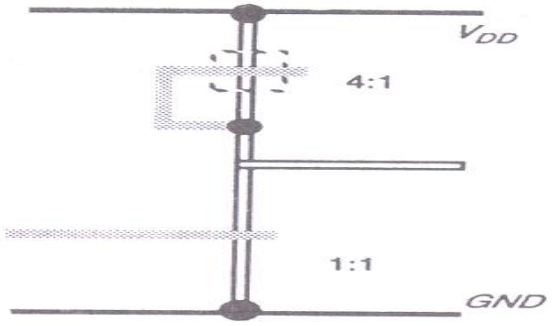


WIRES etc., as for stick diagrams

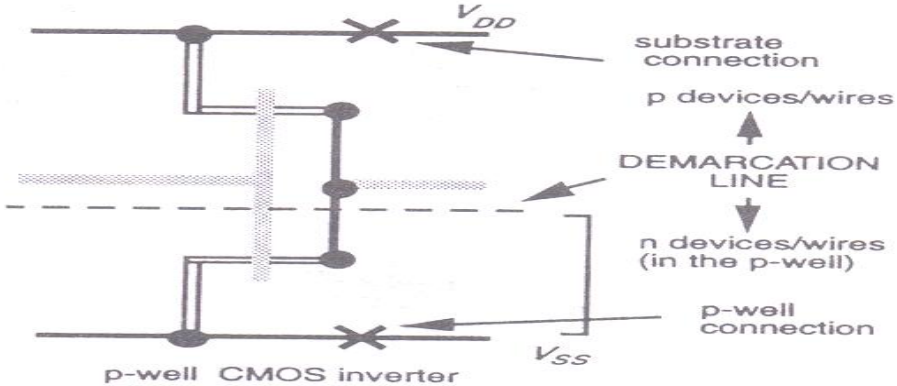


Simple n-well based BiCMOS inverter (symbolic diagram)

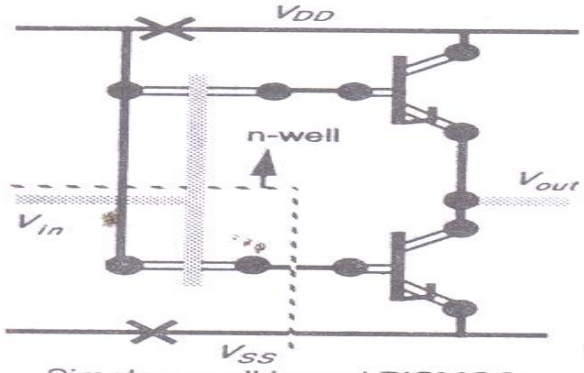
COLOR PLATE 1(d) **Color stick diagram examples. (See Figure 3.1(d) monochrome stick diagrams and simple symbolic encoding.)**



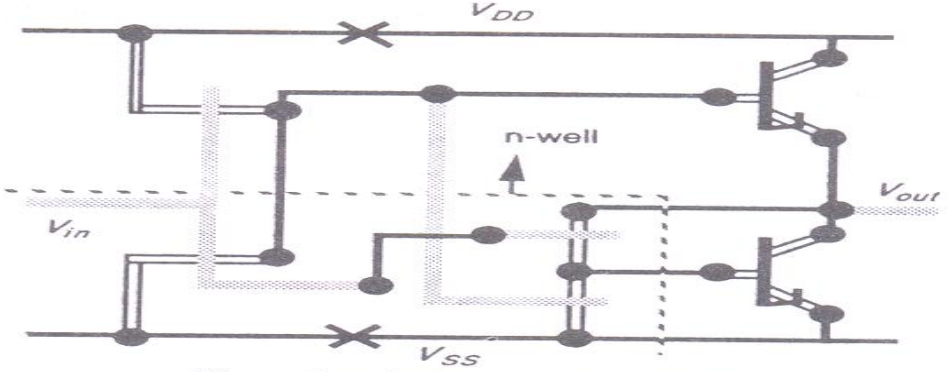
4:1 nMOS inverter



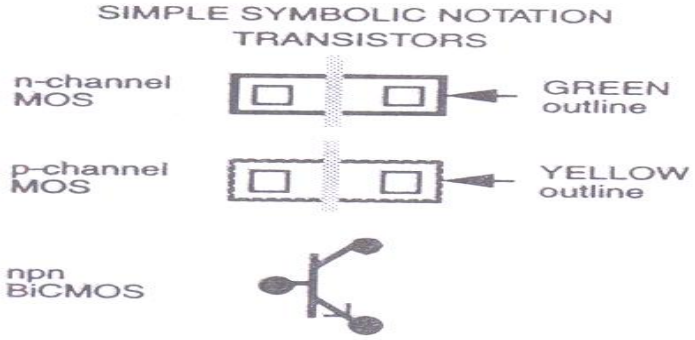
p-well CMOS inverter

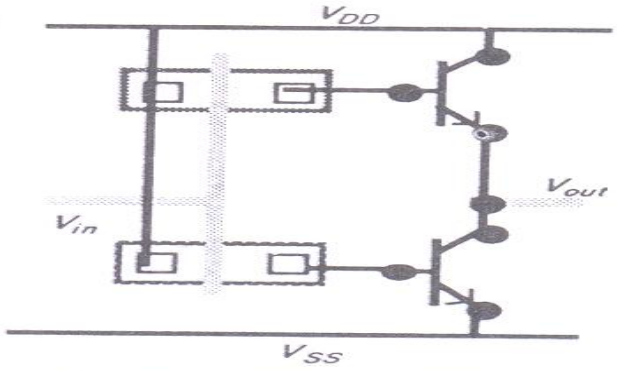


Simple n-well based BiCMOS inverter (stick diagram)



Alternative design of an n-well based BiCMOS inverter





Simple n-well based BiCMOS inverter (symbolic diagram)

Monochrome stick diagram examples

URE 3.1(d) Stick diagrams and simple symbolic encoding (see also Color plate 1(d)).

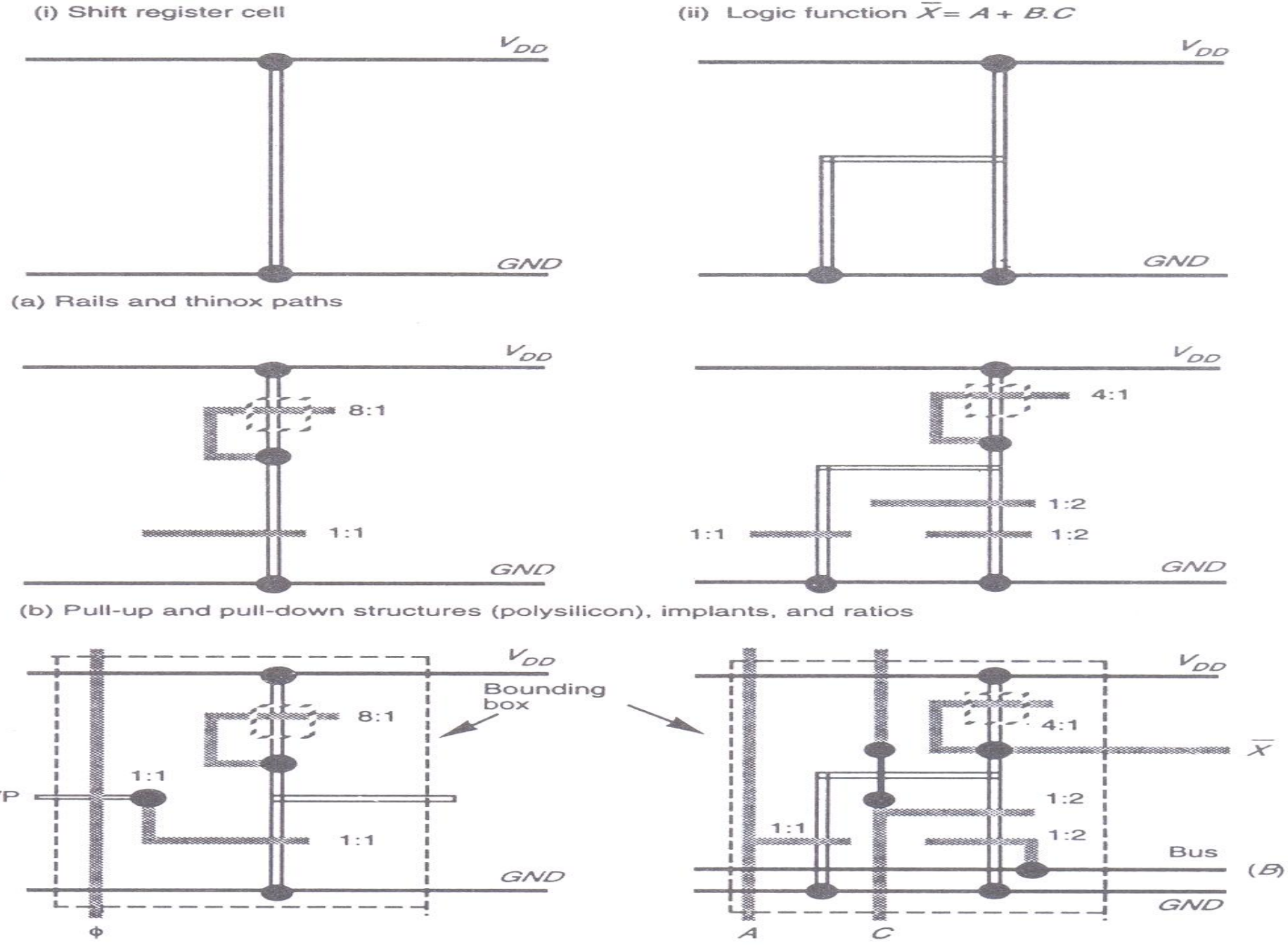
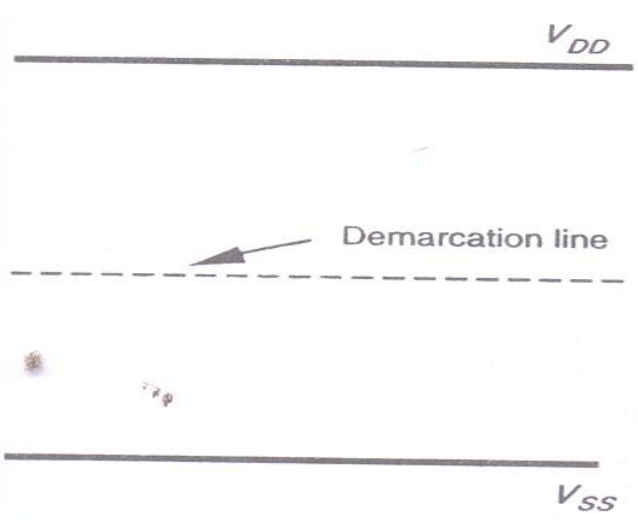
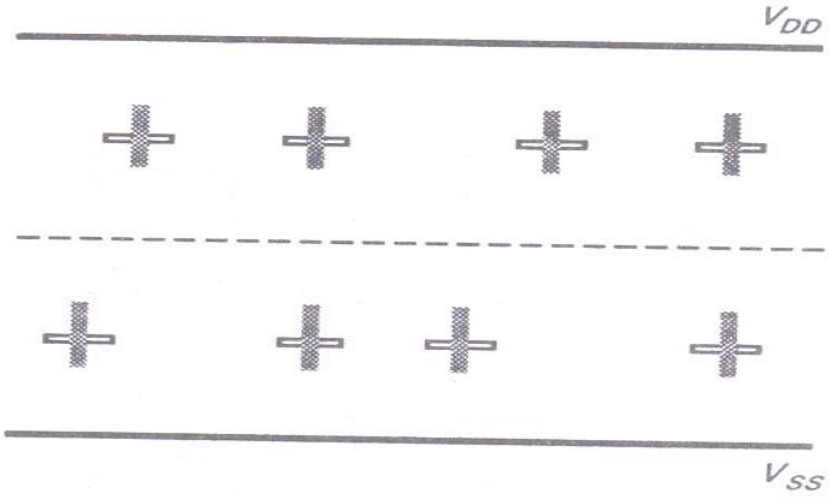


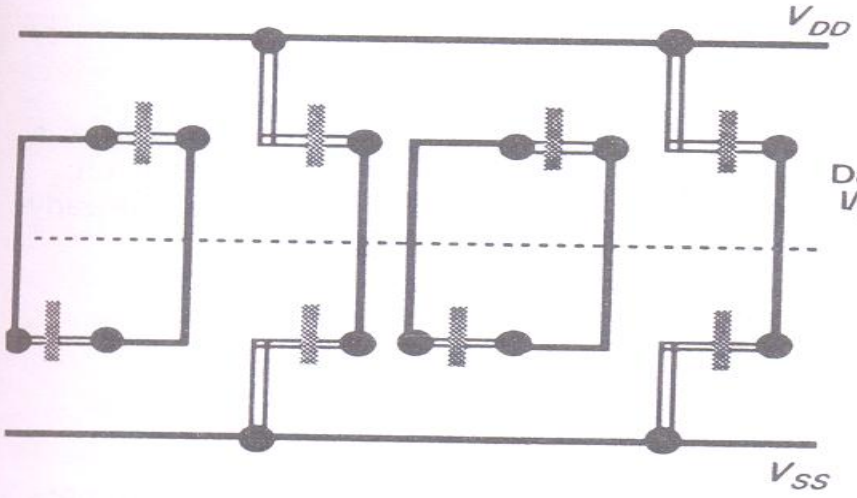
FIGURE 3.3 Examples of nMOS stick layout design style.



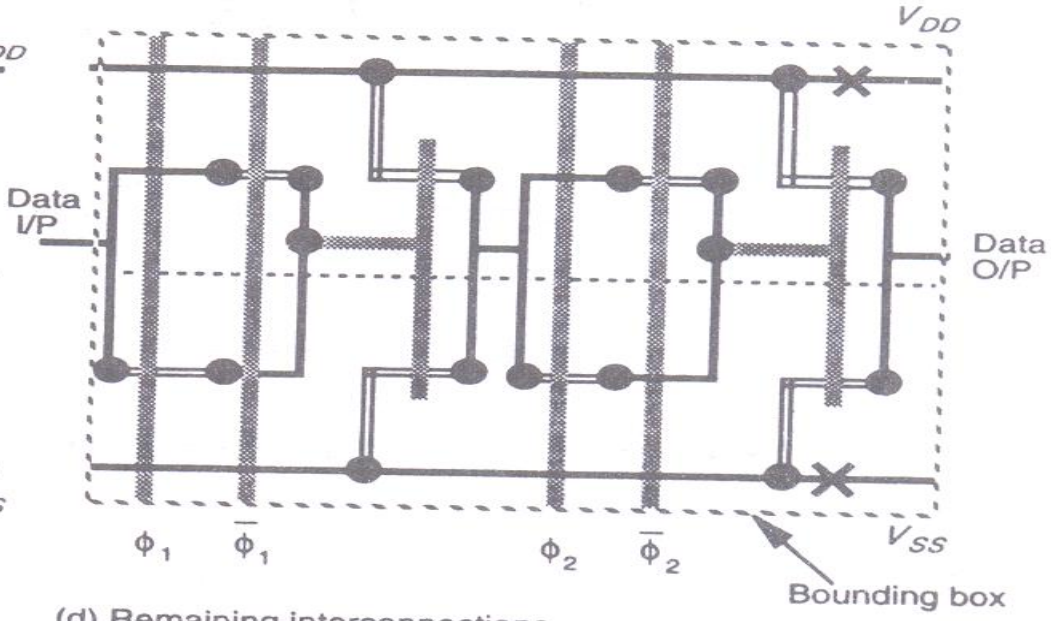
(a) Rails and demarcation line



(b) n- and p-transistors



(c) Metal and diffusion connections



(d) Remaining interconnections

Note: The contact crosses in (d) should represent one V_{DD} contact for every four p-transistors and one V_{SS} contact for every four n-transistors.

FIGURE 3.5 Example of CMOS stick layout design style.

Design Rules and Layout

The object of a set of design rules is to allow a ready translation of circuit design concepts, usually in stick diagram or symbolic form into actual geometry in silicon.

The design rules basically address two issues:

1. The interactions between different layers.
2. The geometrical reproduction of features that can be reproduced by the mask-making and lithographical process.

Lambda based Design Rules:

1. The lambda based design rule specify every dimension of a system in terms of a parameter
   λ which is subsequently assigned a value, such that the features resulting out of the design
   are supported by the fabrication process.
2. Defining lambda makes design independent of process therefore chip can be sealed to any
   ratio that means today's design remain usable when line widths are reduced(λ) by advances
   in future technology.
3. Under these rules, all dimensions in all layers will be dimensioned in λ units and after that λ
   is given an appropriate value acceptable to the feature size of the fabrication process.

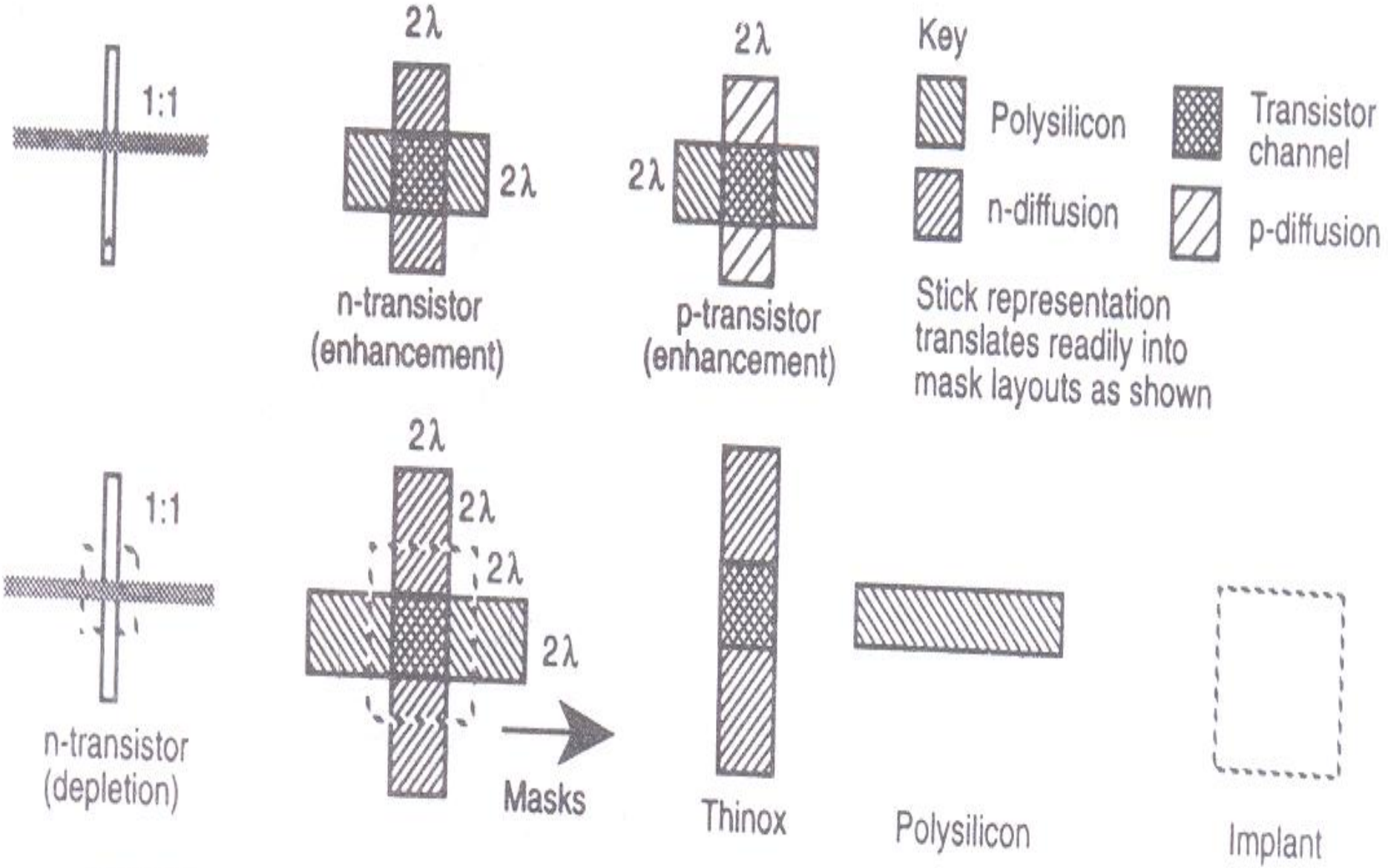


FIGURE 3.2 Stick diagrams and corresponding mask layout examples.

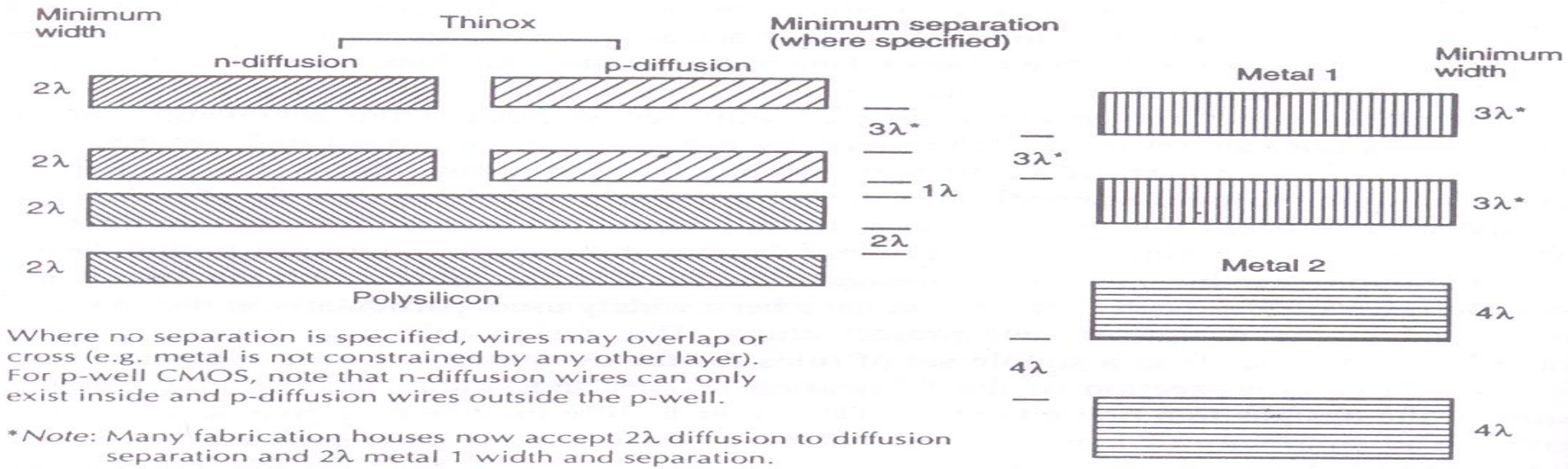


Figure 3–6 Design rules for wires (nMOS and CMOS)

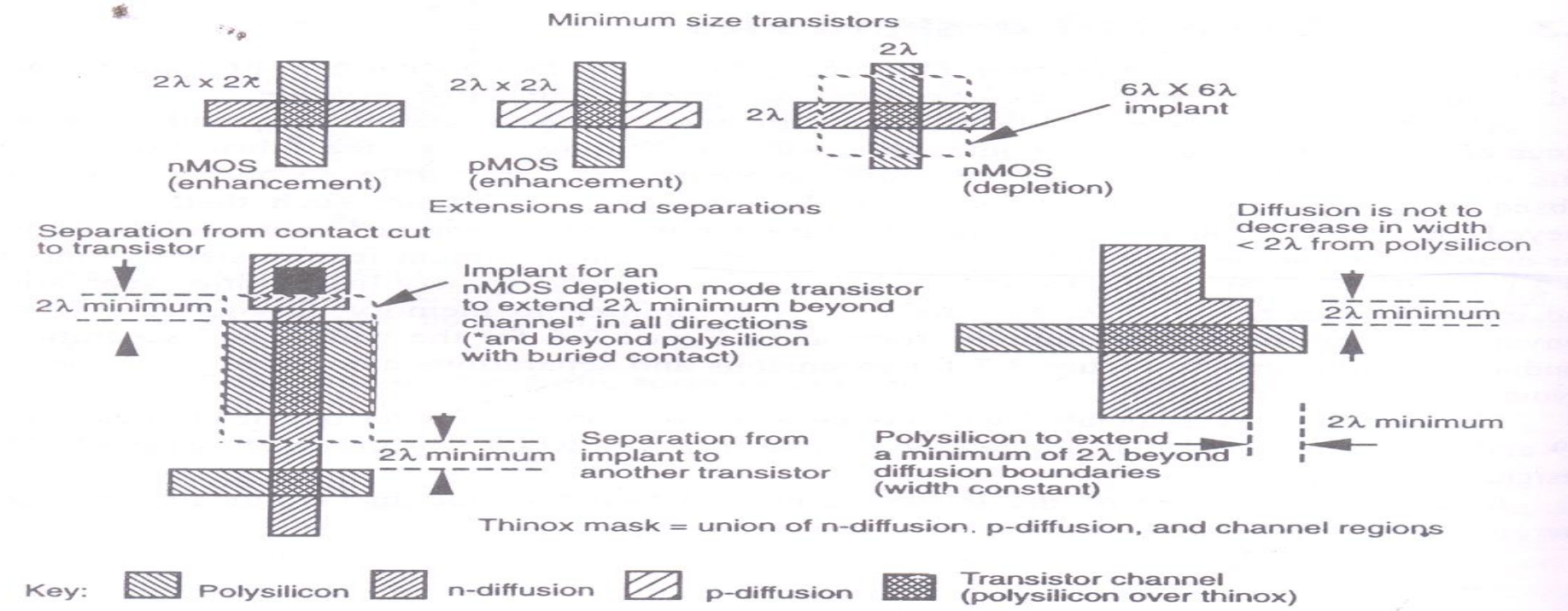
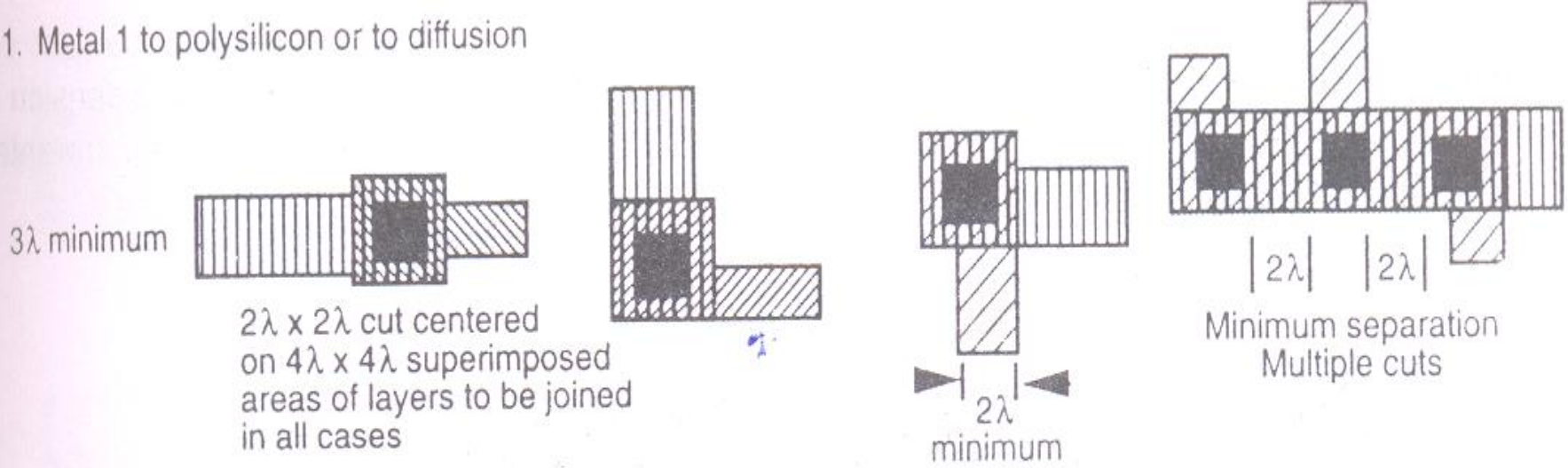


FIGURE 3.7 Transistor design rules (nMOS, pMOS and CMOS).

1. Metal 1 to polysilicon or to diffusion



2. Via (contact from metal 2 to metal 1 and thence to other layers)

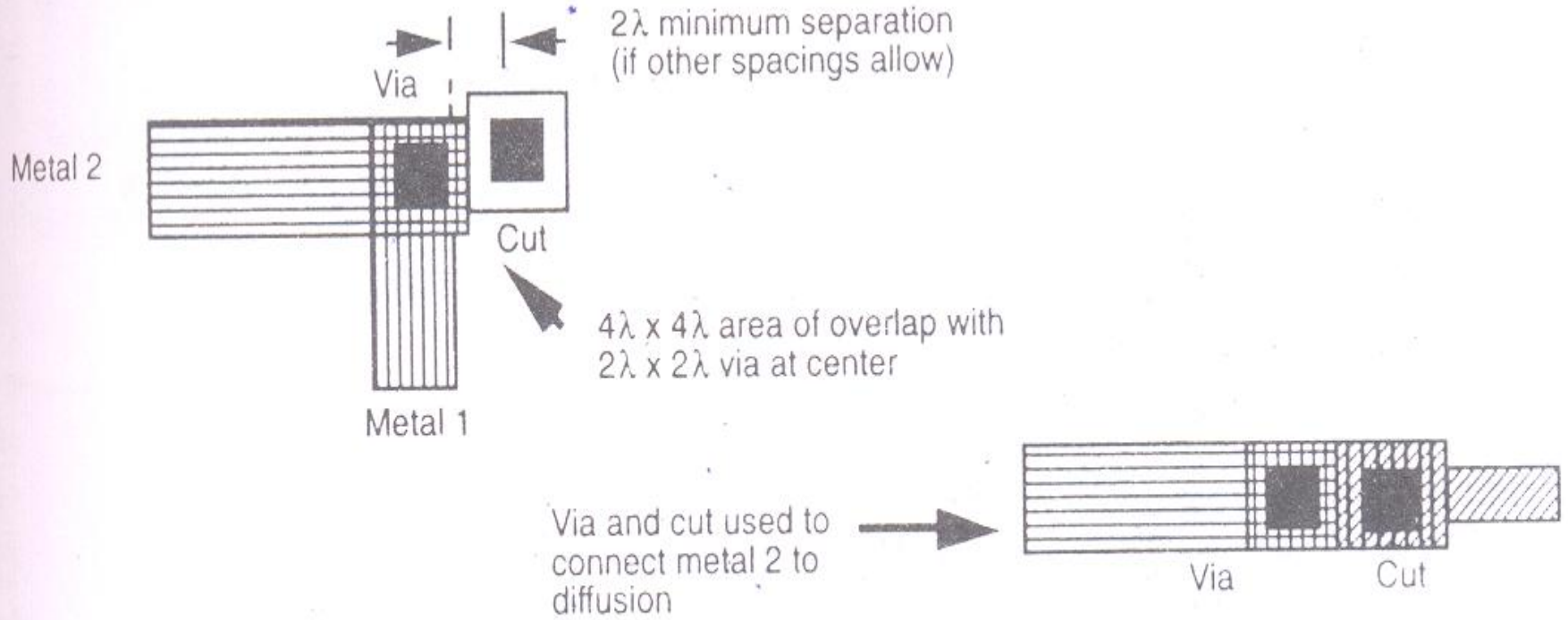


FIGURE 3.8 Contacts (nMOS and CMOS).

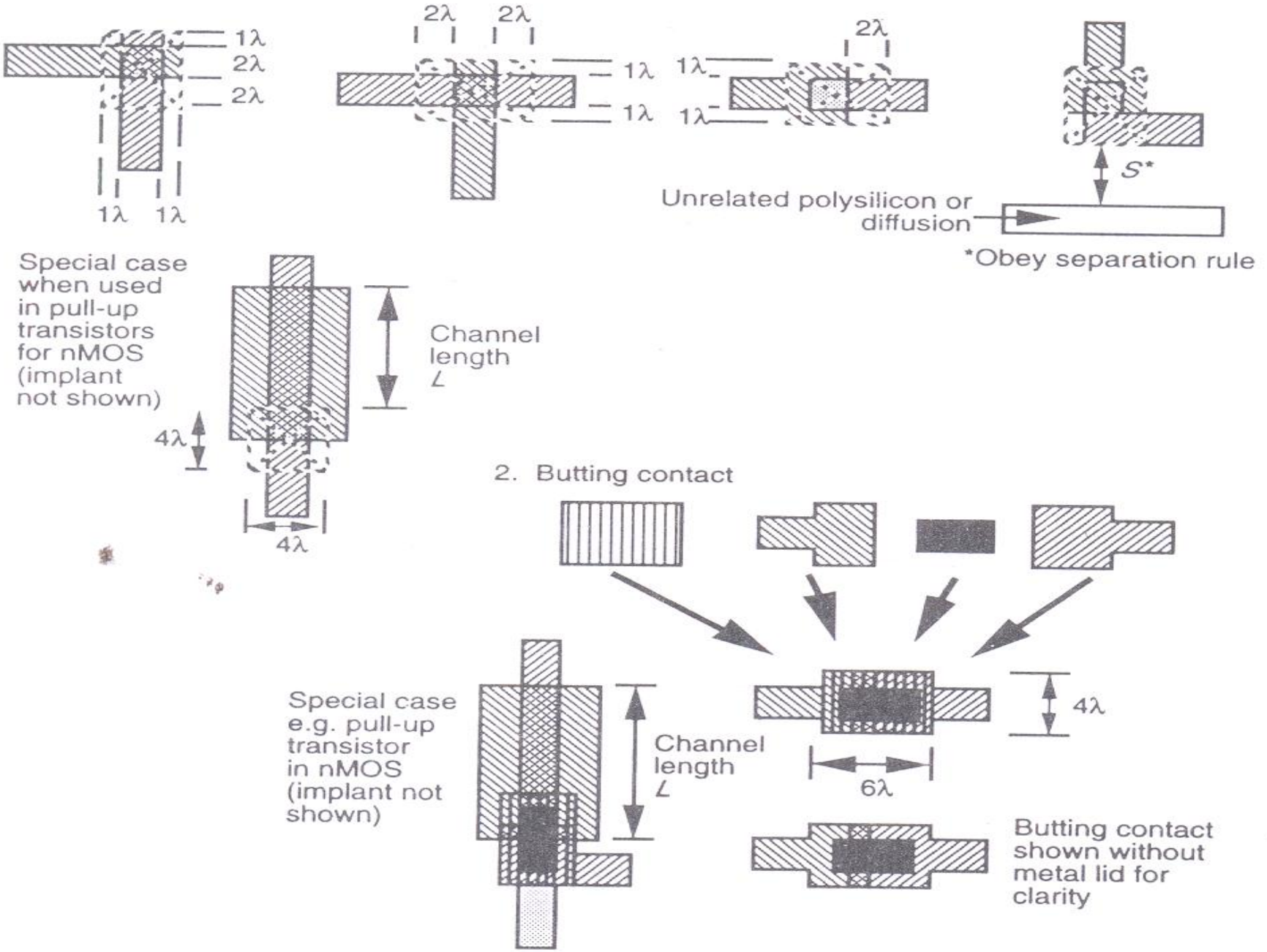
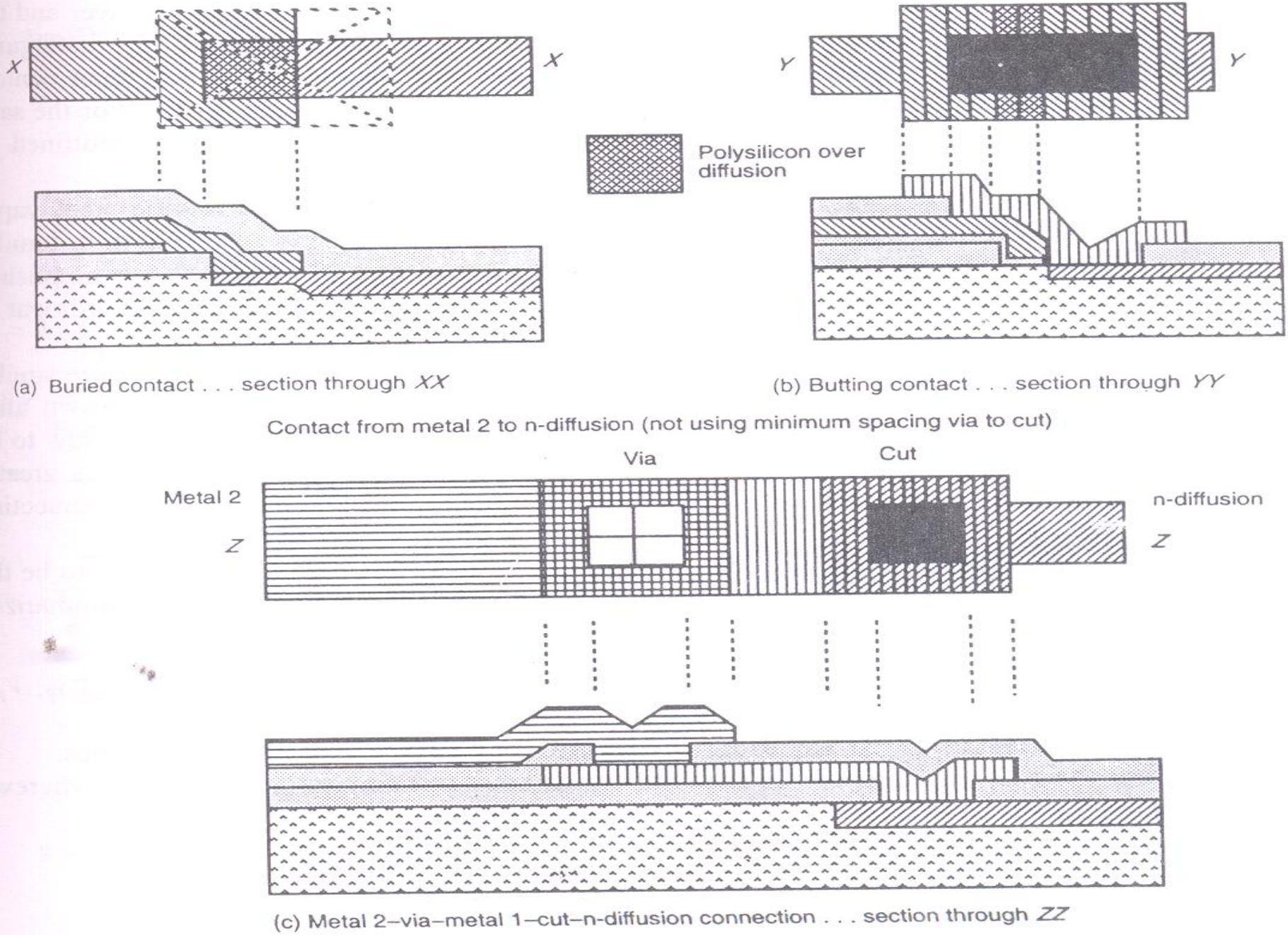


FIGURE 3.9 Contacts polysilicon to diffusion (nMOS only in the main text).



(a) Buried contact . . . section through *XX*

(b) Butting contact . . . section through *YY*

(c) Metal 2–via–metal 1–cut–n-diffusion connection . . . section through *ZZ*

FIGURE 3.10 Cross-sections through some contact structures.

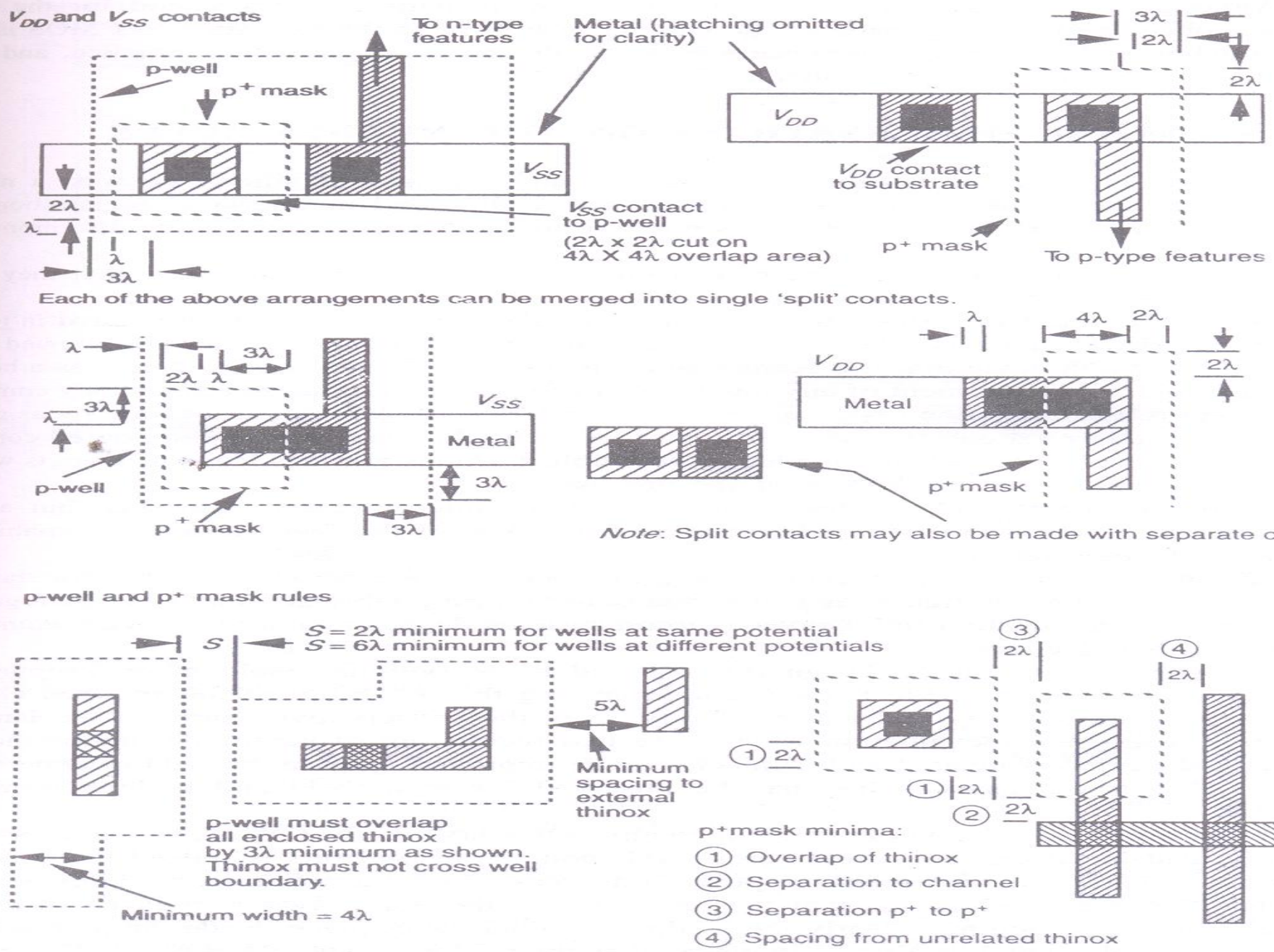


FIGURE 3.11 Particular rules for p-well CMOS process.

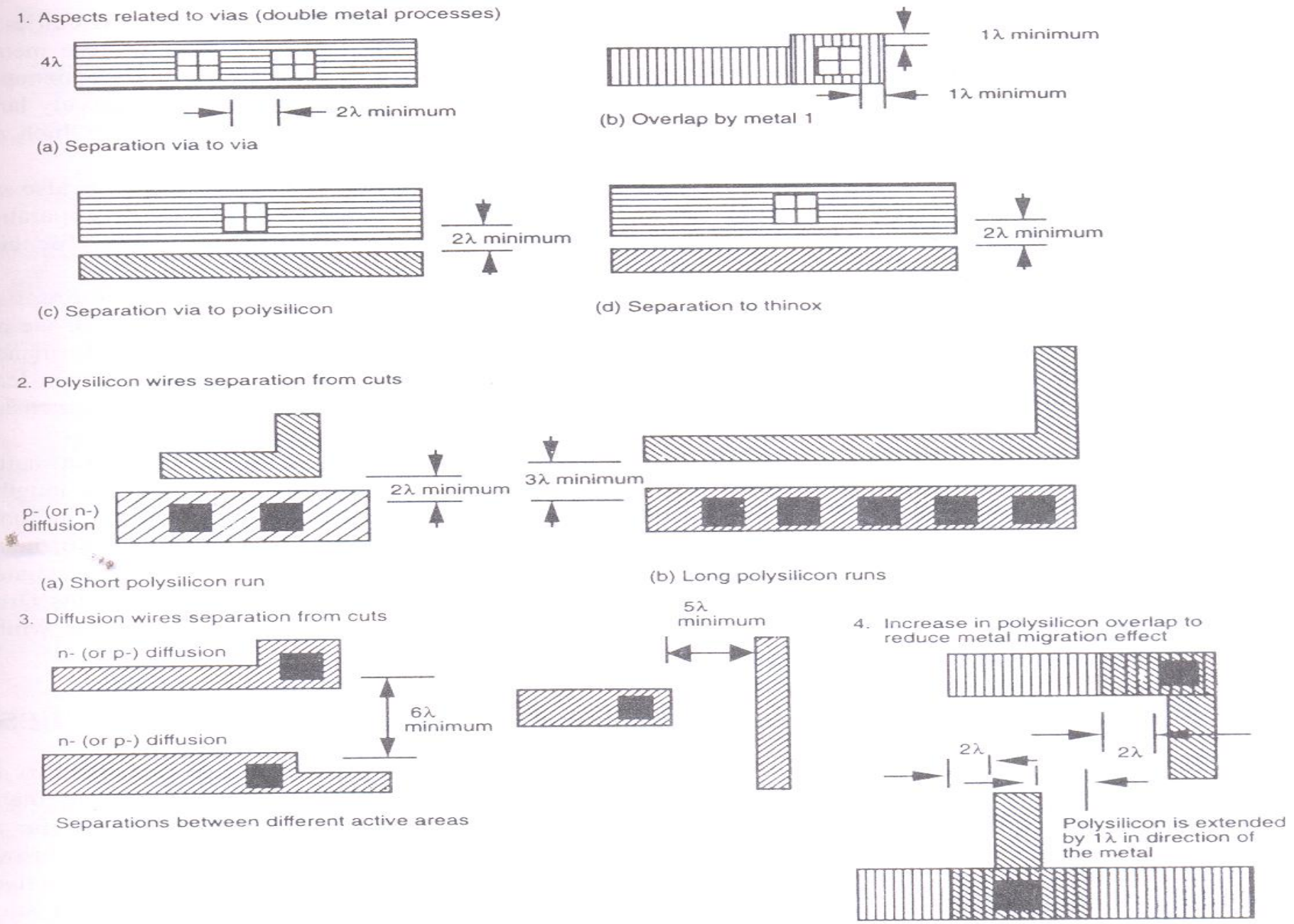
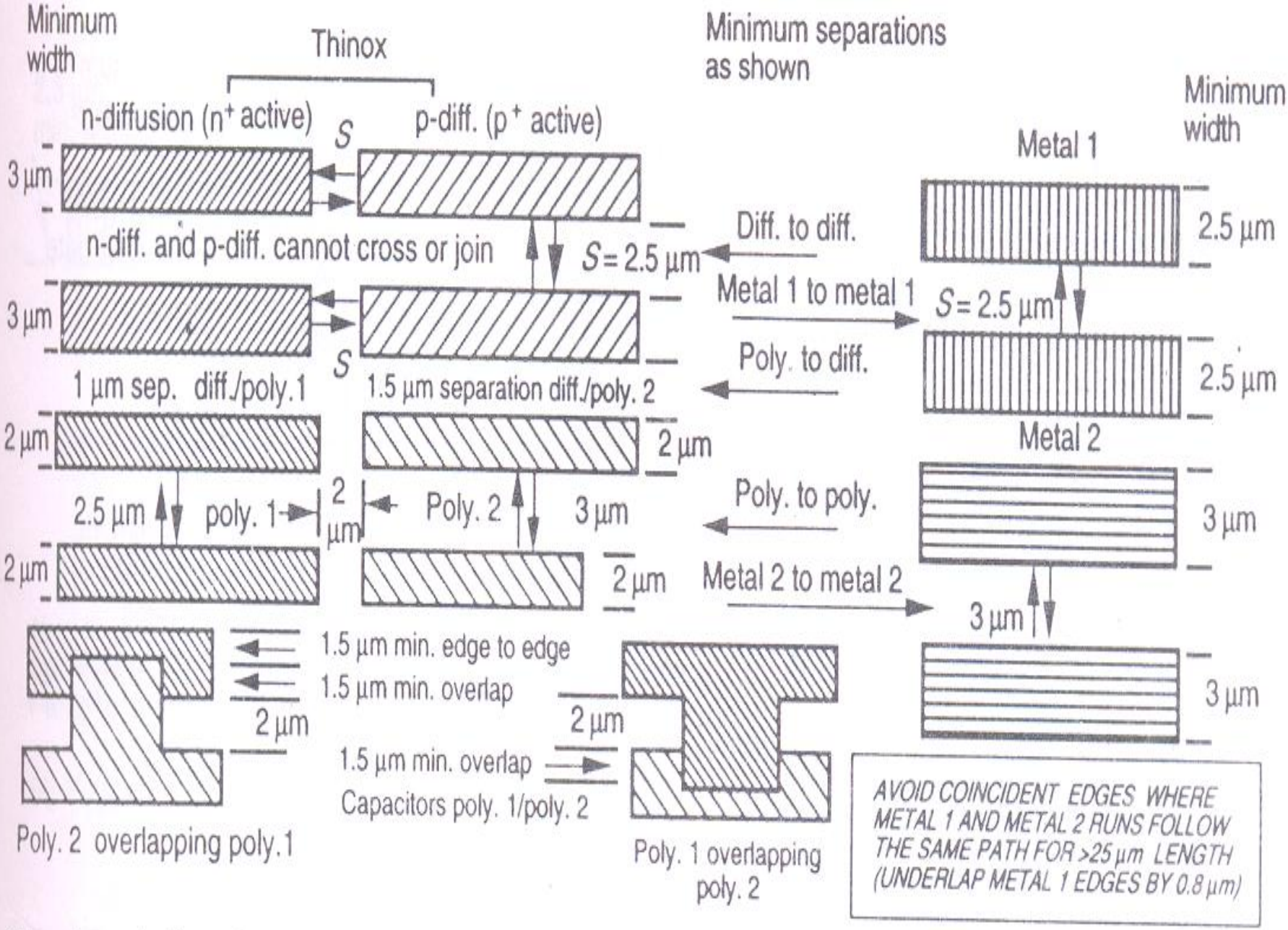


FIGURE 3.12 Further aspects of λ-based design rules for contacts, including some factors contributing to higher yield/reliability.



Otherwise polysilicon 2 must not be coincident with polysilicon 1

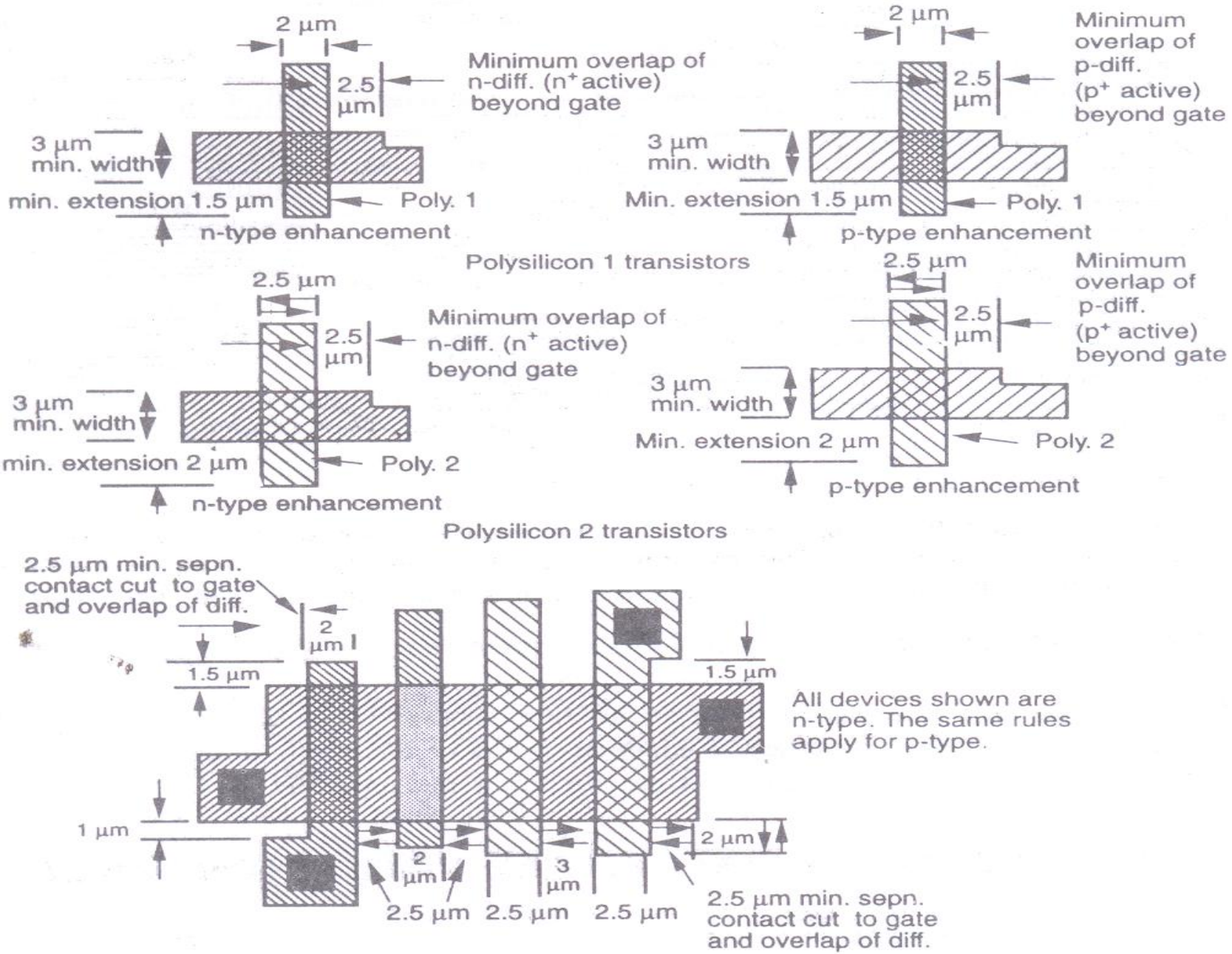


FIGURE 3.13(b) Transistor related design rules (Orbit 2 µm CMOS) minimum sizes and overlaps

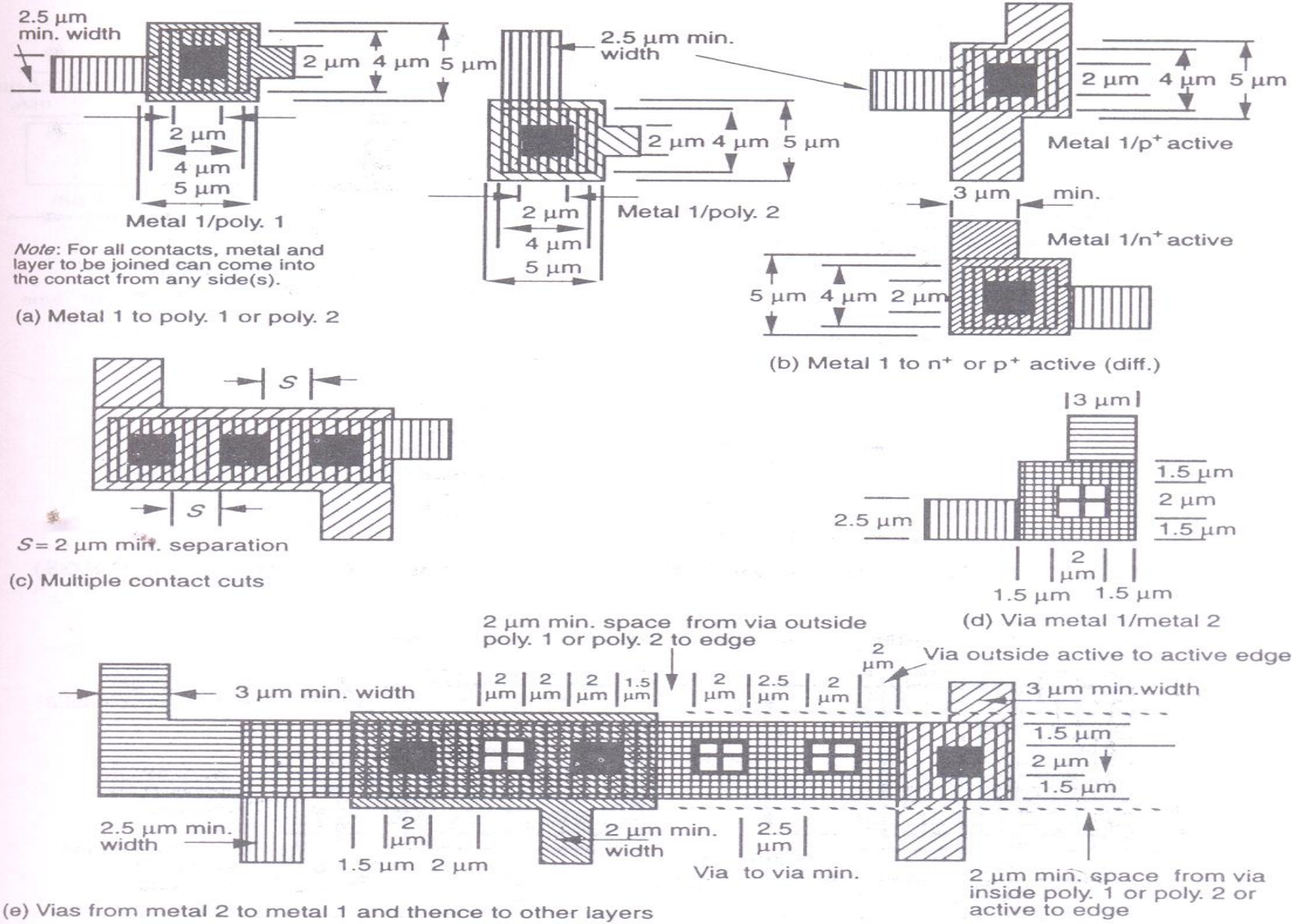


FIGURE 3.13(c) Rules for contacts and vias (Orbit 2 µm CMOS).

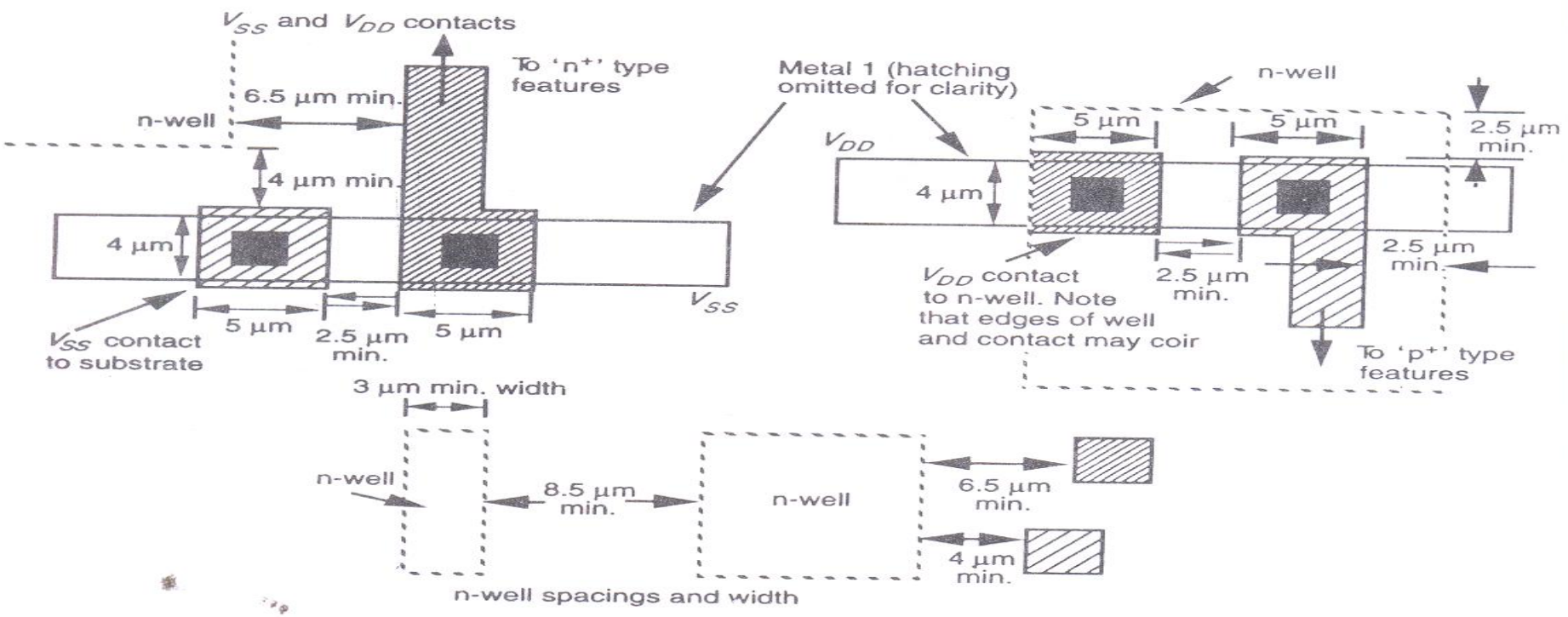
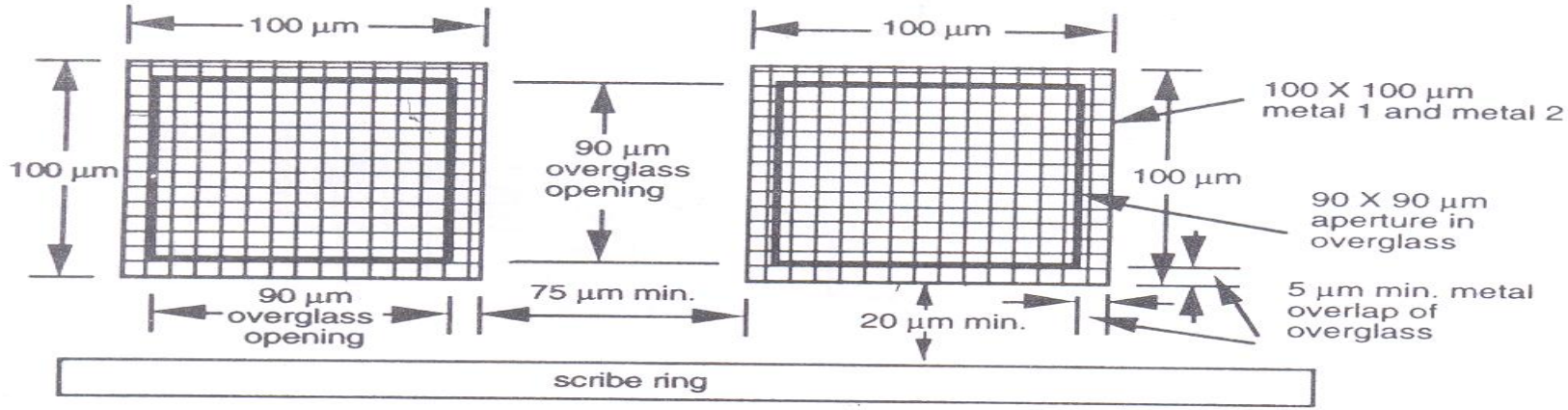
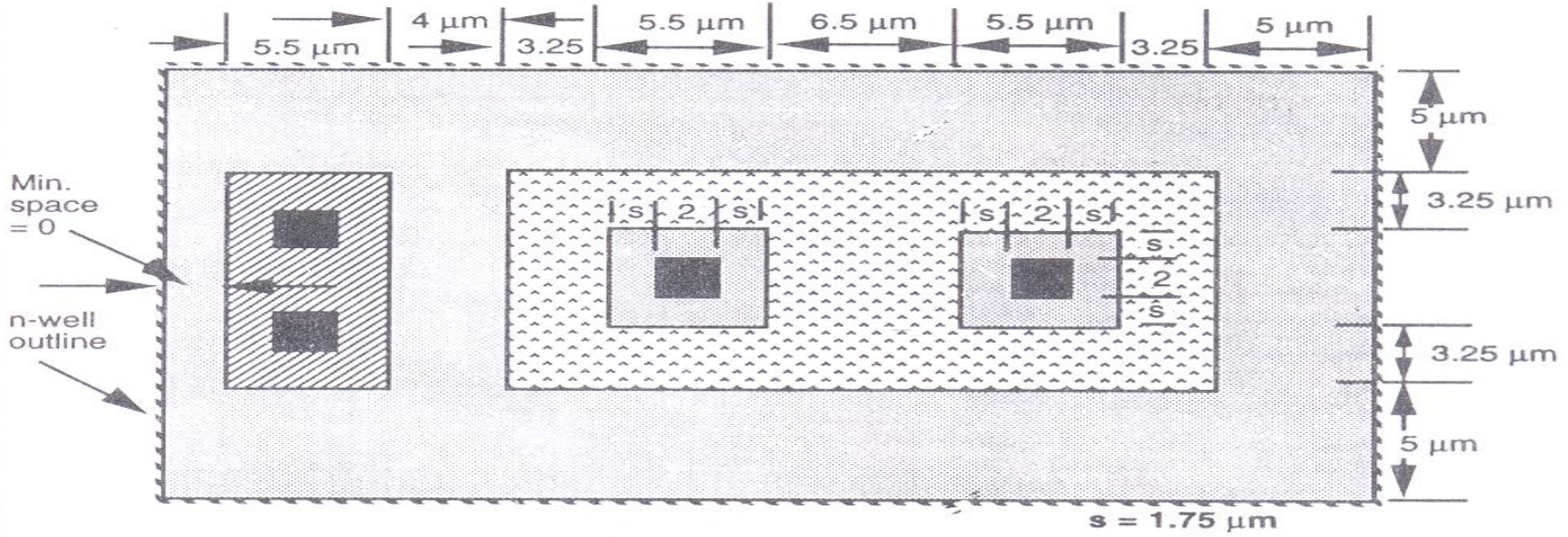


FIGURE 3.13(d) Rules for n-well and V_{DD} and V_{SS} contacts (Orbit 2 µm CMOS).

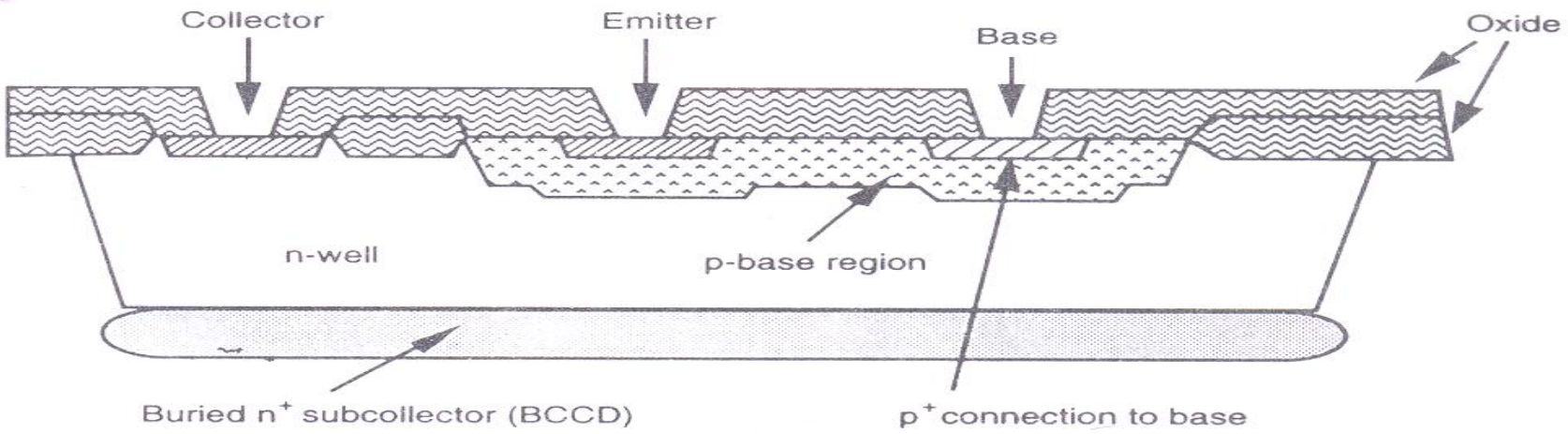


Other rules and encodings:
Via overlap of pad 2 µm.
Pad to active separation 20 µm min.
Color encoding for overglass mask . . . Gray

FIGURE 3.13(e) Rules for pad and overglass geometry (Orbit 2 µm CMOS).



Note: For clarity, the layers have not been drawn transparent but BCCD underlies the entire area and the p-base underlies all within its boundary.



Cross-section through npn transistor (Orbit 2 µm BiCMOS)

FIGURE 3.13(f) Special rules for BiCMOS transistors (Orbit 2 µm CMOS).

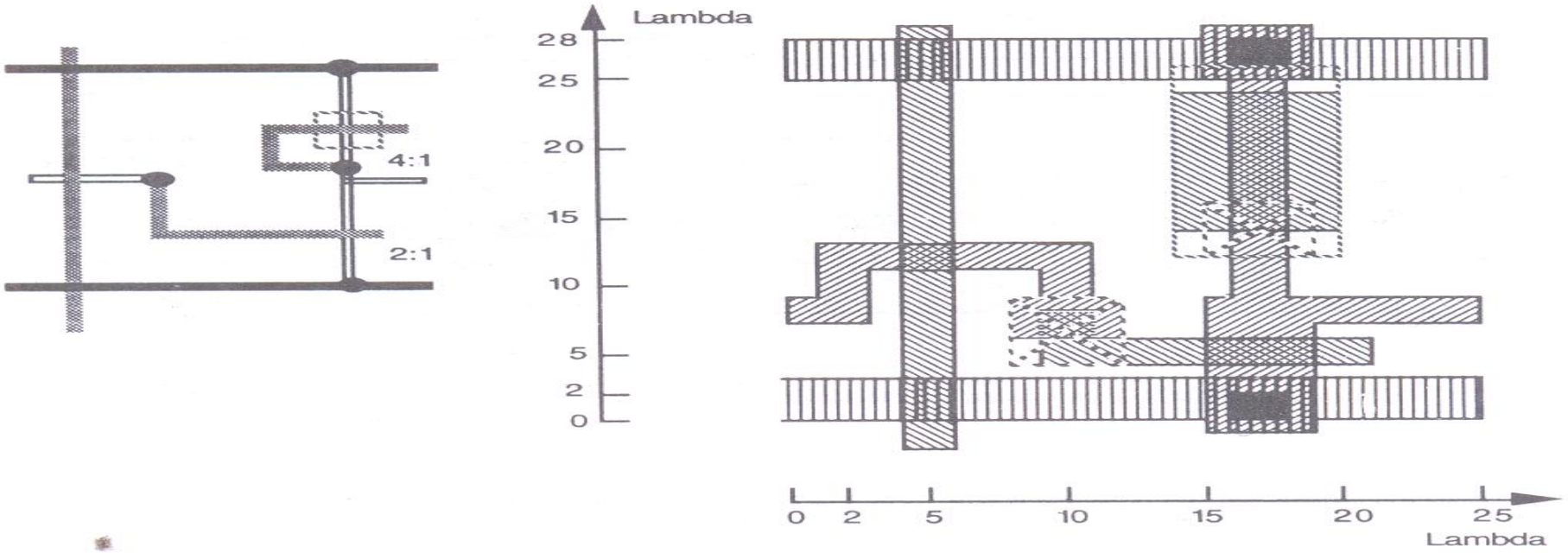


FIGURE 3.14 Stick diagram and layout for nMOS shift register cell.

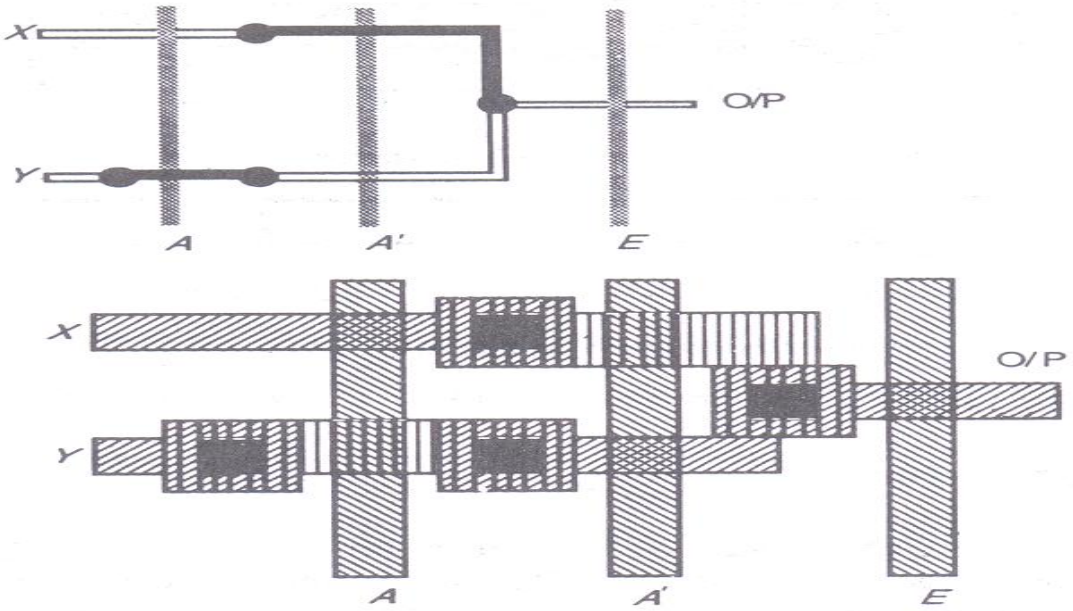


FIGURE 3.15 Two-way selector with enable.

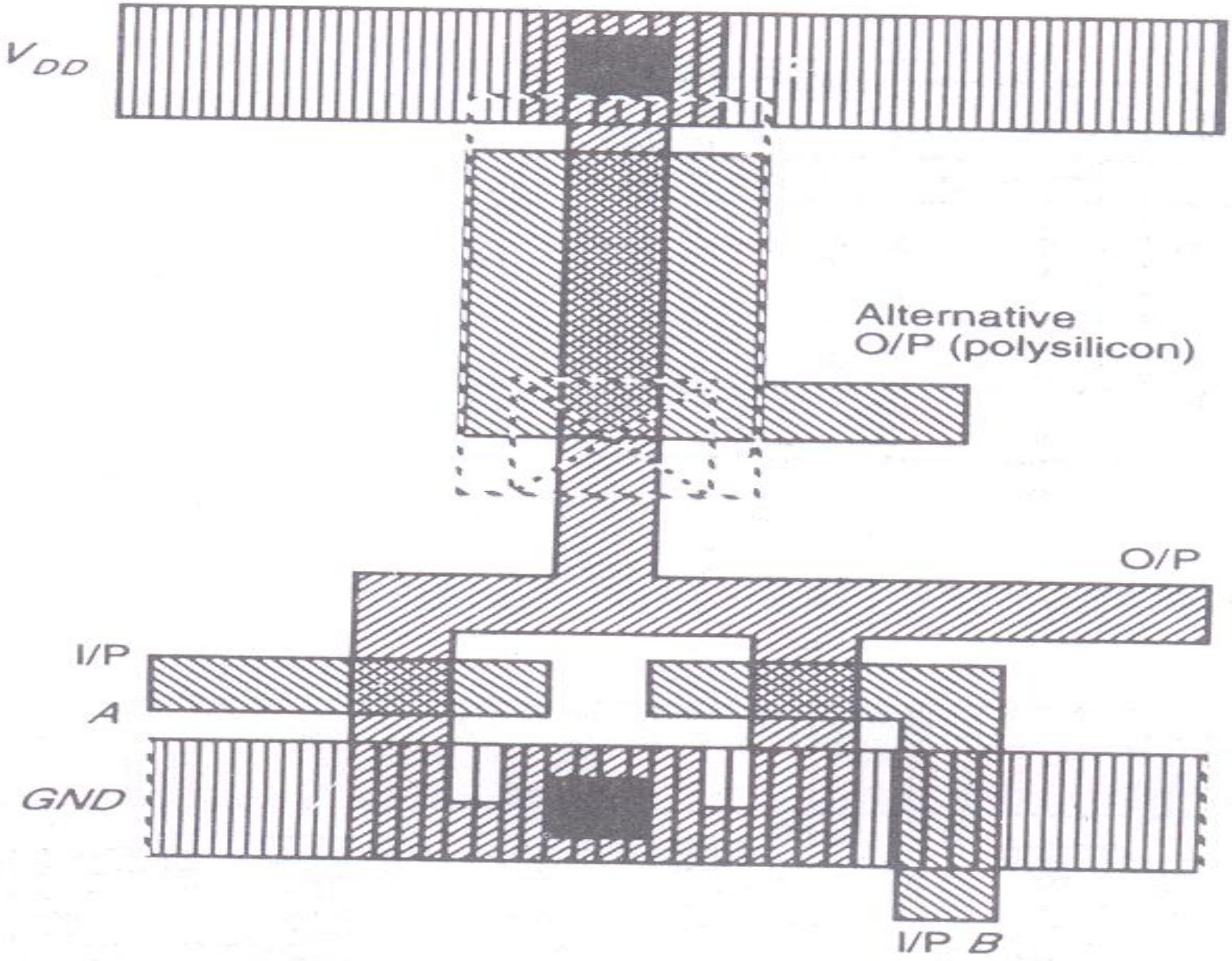


FIGURE 3.16 Two I/P nMOS *Nor* gate.

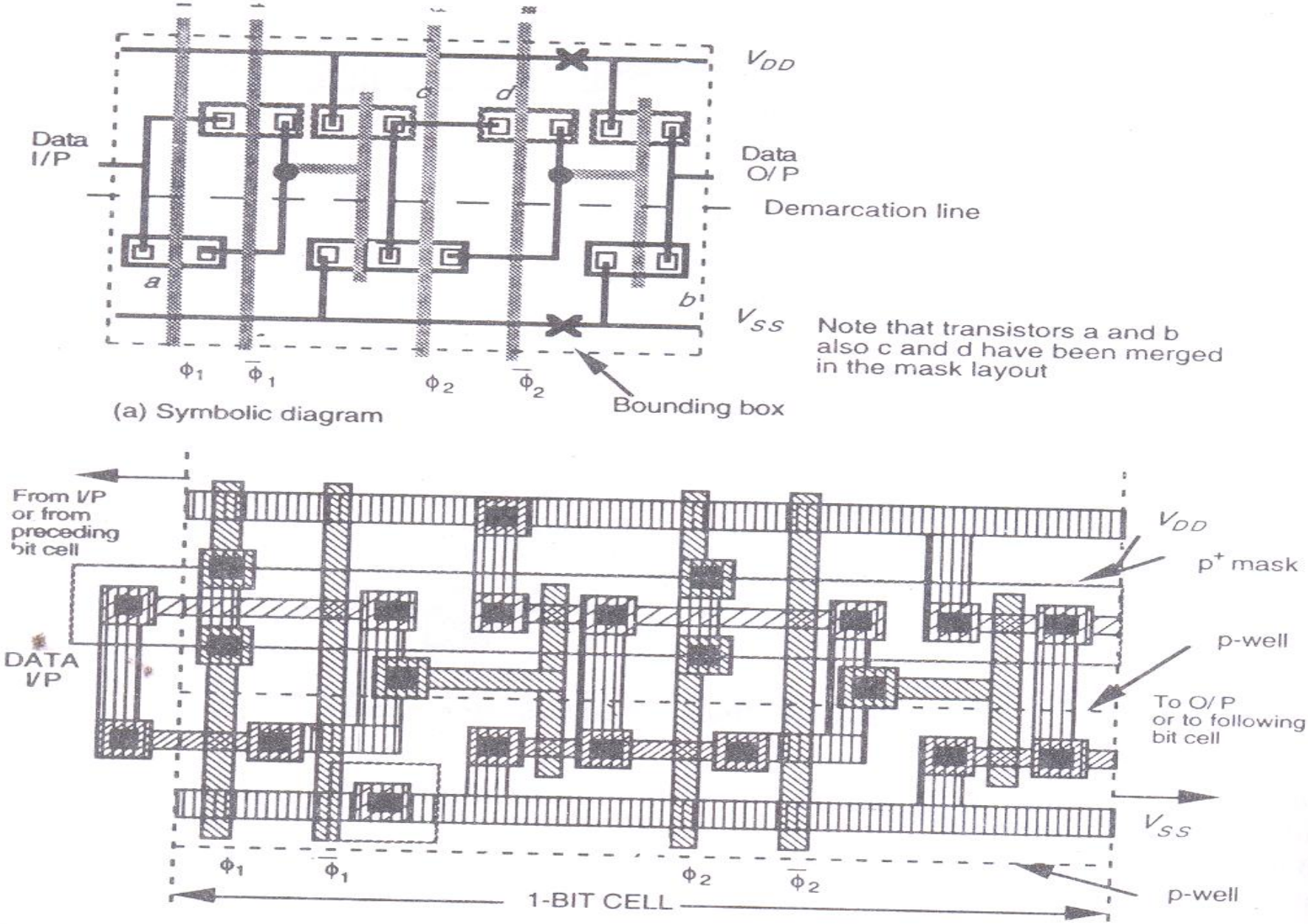


FIGURE 3.17 A 1-bit CMOS shift register cell.

Queries ...?