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Hirasugar Institute of Technology, Nidasoshi.

Inculcating Values, Promoting Prosperity

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ECE Dept.
VLSI DESIGN
VI Sem
2017-18

Department of Electronics & Communication Engg.

Course : VLSI DESIGN-15EC63. **Sem.: 6th**

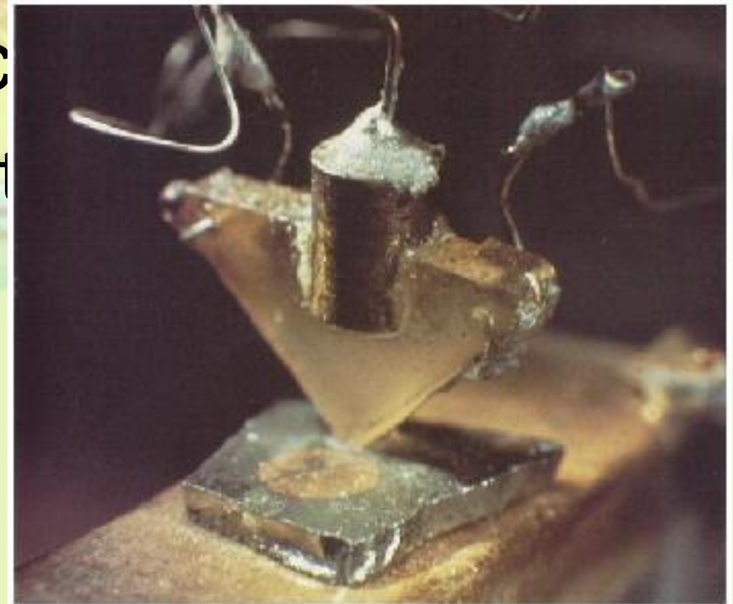
Course Coordinator:

Prof. S. S. Kamate

Invention of the Transistor

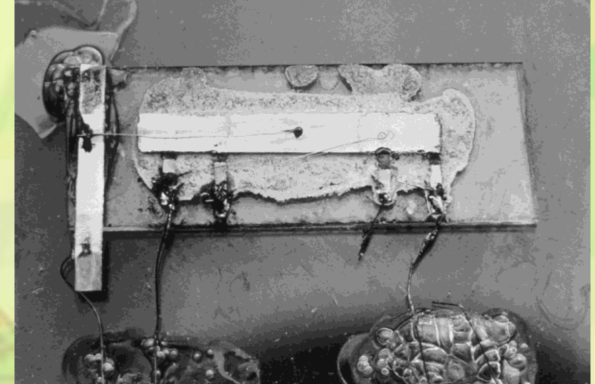
- Vacuum tubes ruled in first half of 20th century Large, expensive, power-hungry, unreliable
- 1947: first point contac
  - John Bardeen and Walt Labs
  - See *Crystal Fire*

    by Riordan, Hoddeson

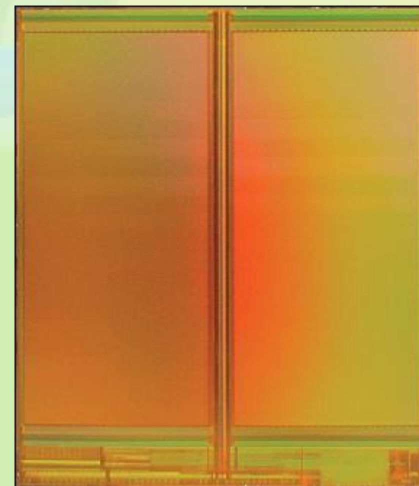


A Brief History

- 1958: First integrated circuit
  - Flip-flop using two transistors
  - Built by Jack Kilby at Texas Instruments
- 2010
  - Intel Core i7 μprocessor
    - 2.3 billion transistors
  - 64 Gb Flash memory
    - > 16 billion transistors



Courtesy Texas Instruments



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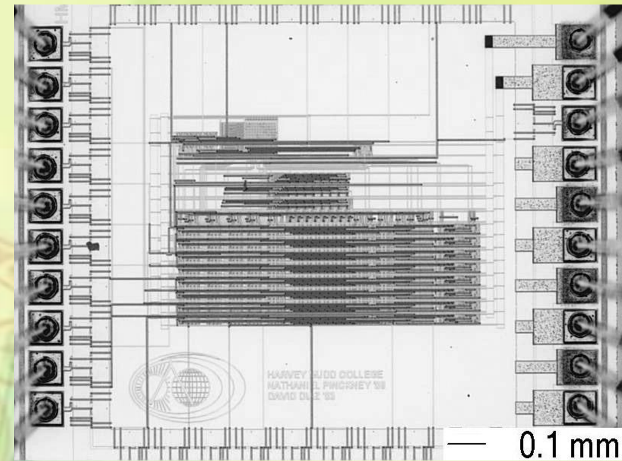
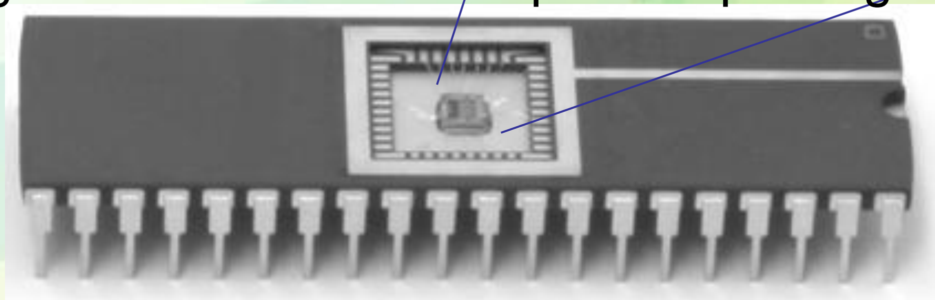
Fabrication & Packaging

- Tapeout final layout
- Fabrication
  - 6, 8, 12” wafers
  - Optimized for throughput, not latency (10 weeks!)
  - Cut into individual dice
- Packaging
  - Bond gold wires from die I/O pads to package





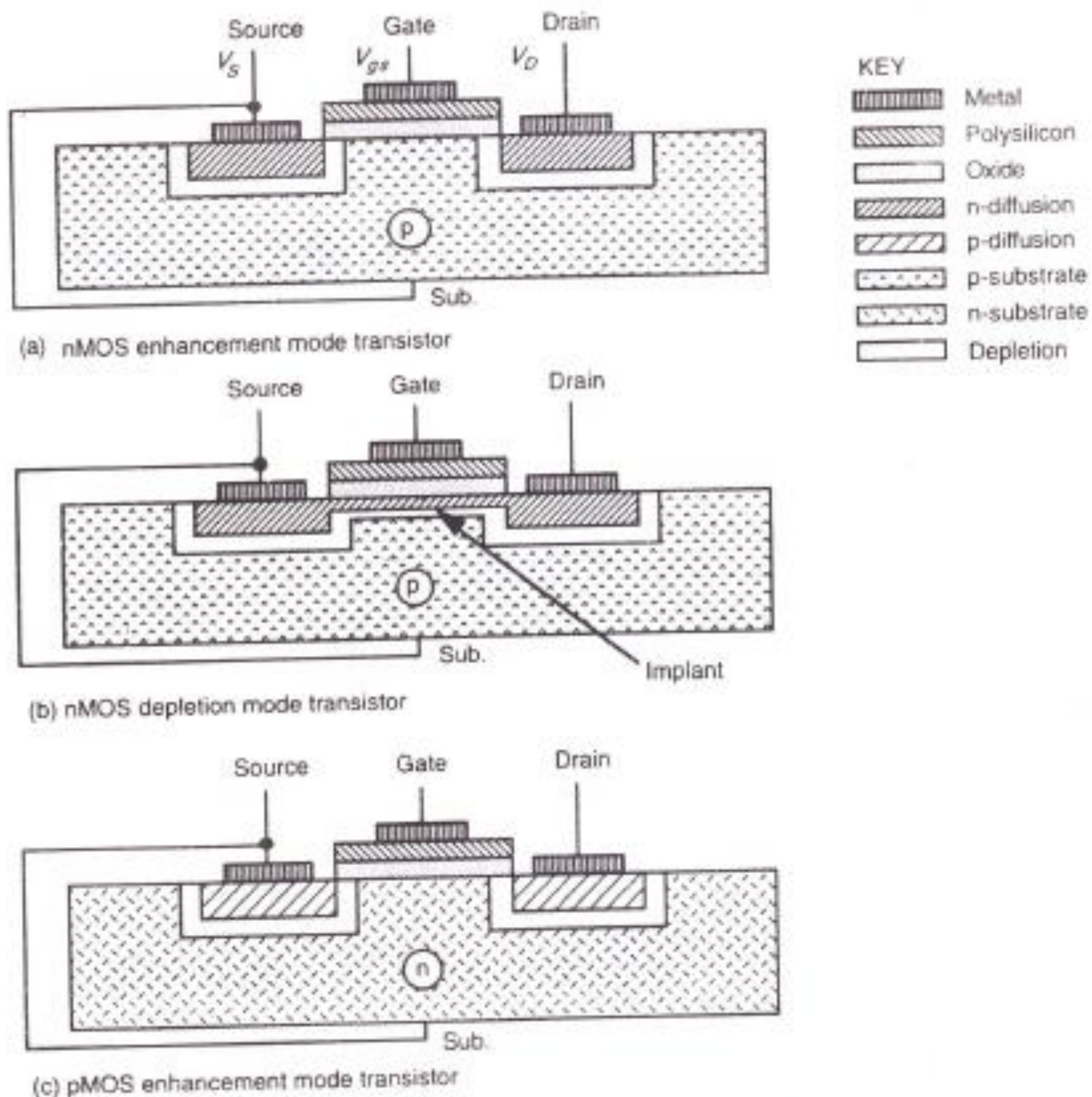
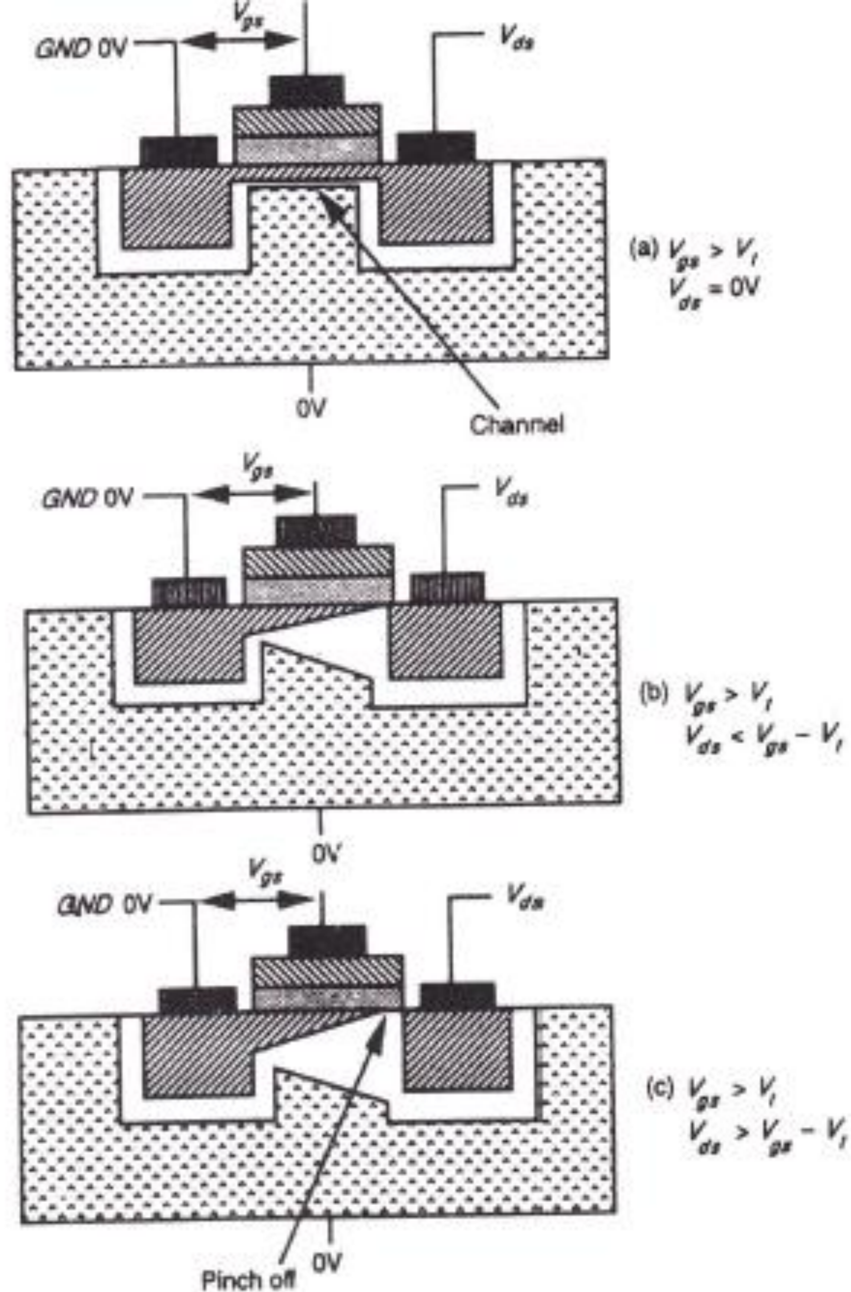
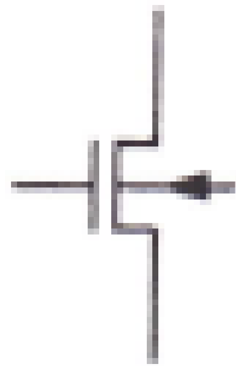
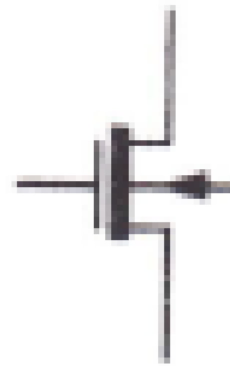
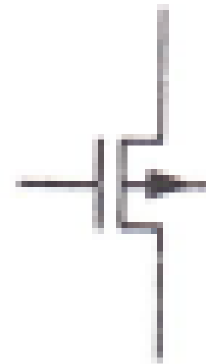
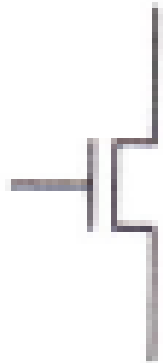
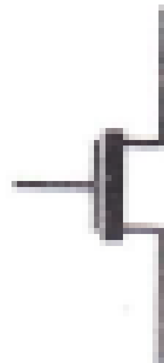
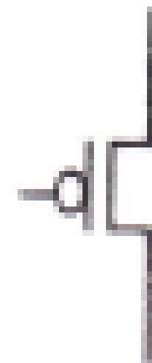


FIGURE 1.4 MOS transistors (V_D = 0 V. Source gate and substrate to 0 V).



Note: V_{ds} is the drain-to-source voltage. Substrate assumed connected to 0 V.

RE 1.5 Enhancement mode transistor for particular values of V_{ds} with ($V_{gs} > V_t$).

nMOS enhancement | nMOS depletion | pMOS enhancement

FIGURE 1.6 Transistor circuit symbols.

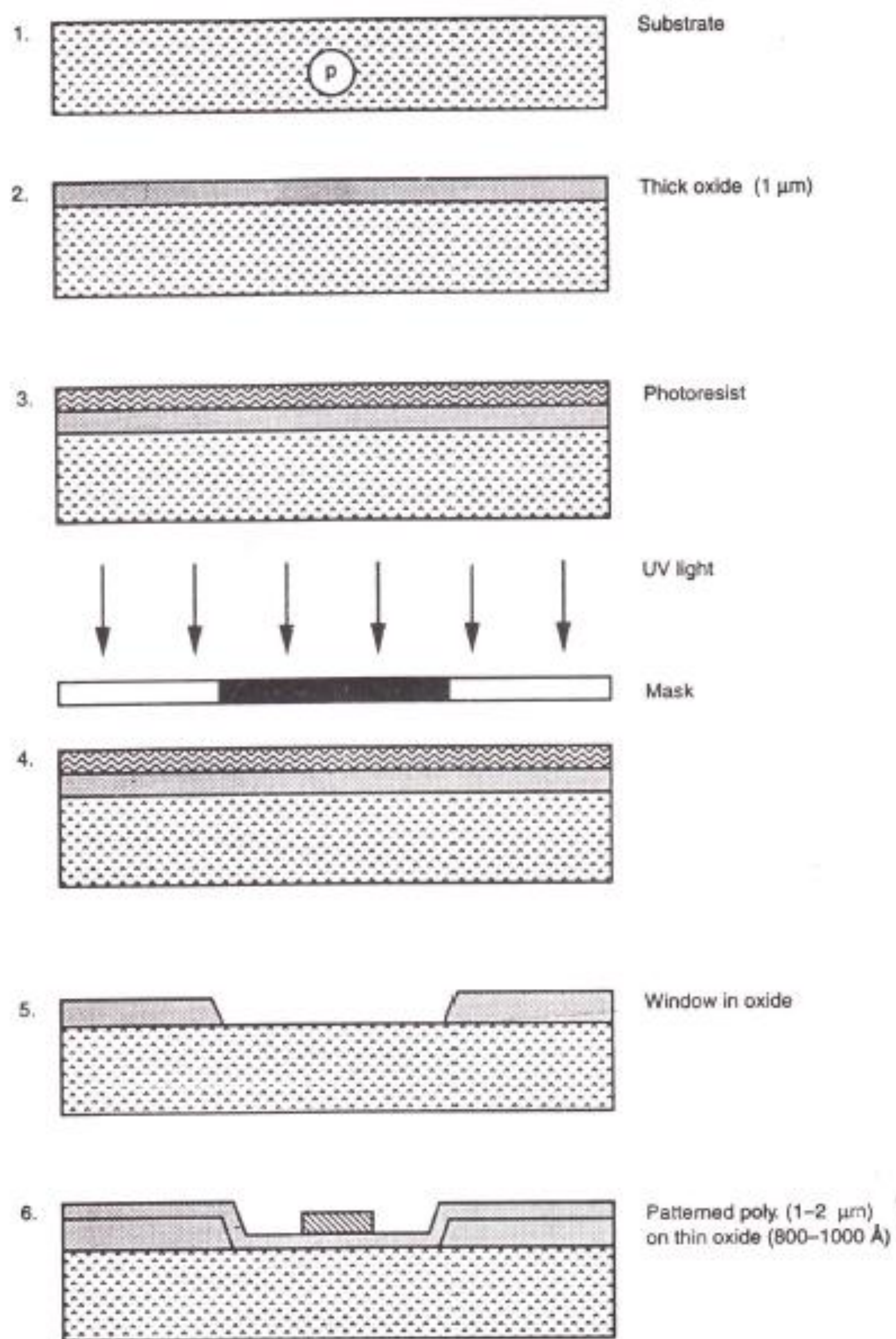
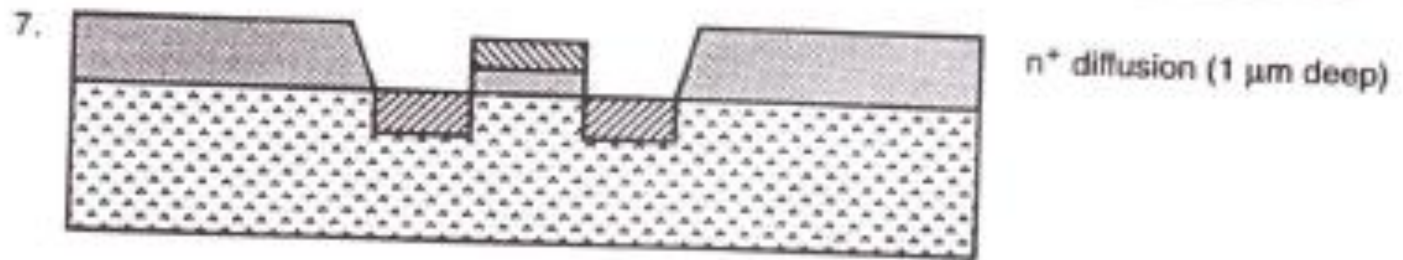
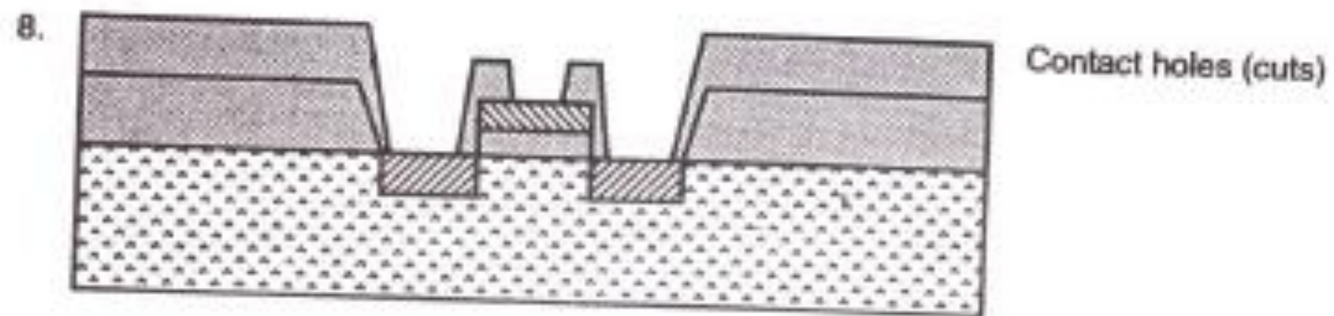


FIGURE 1.7 Continued





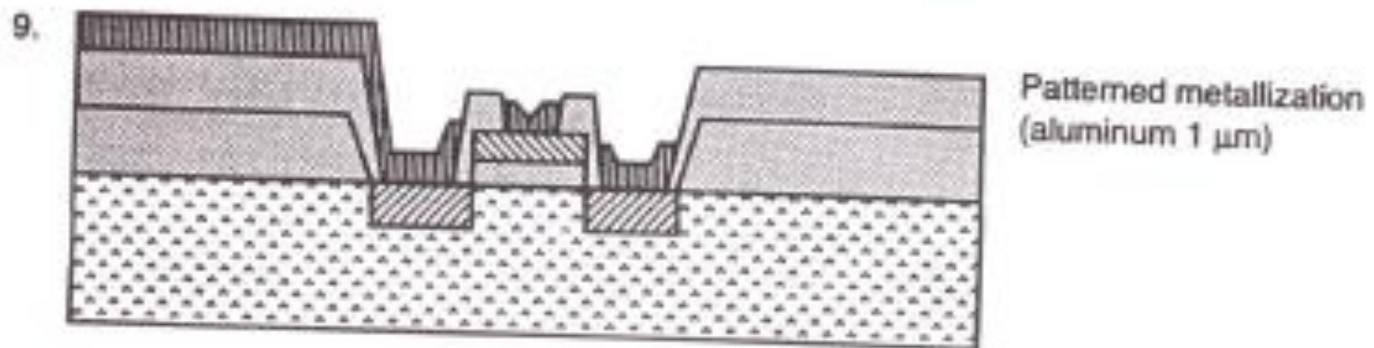
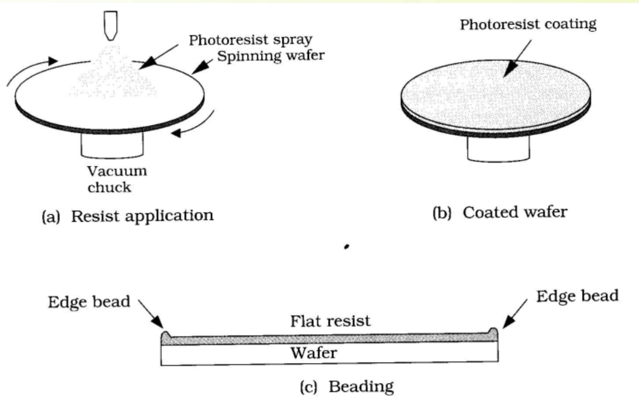
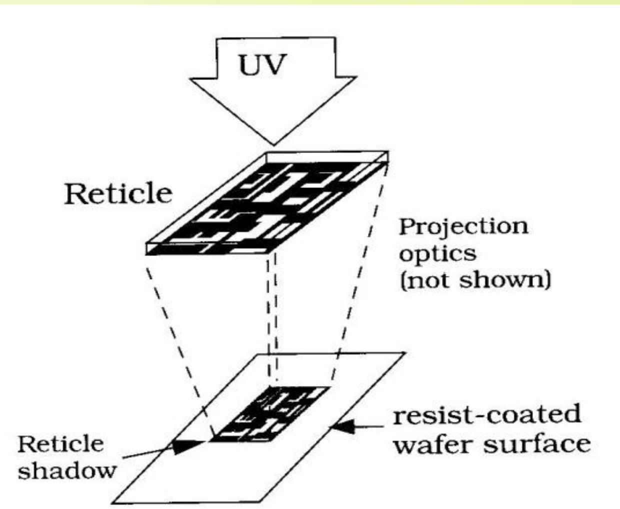
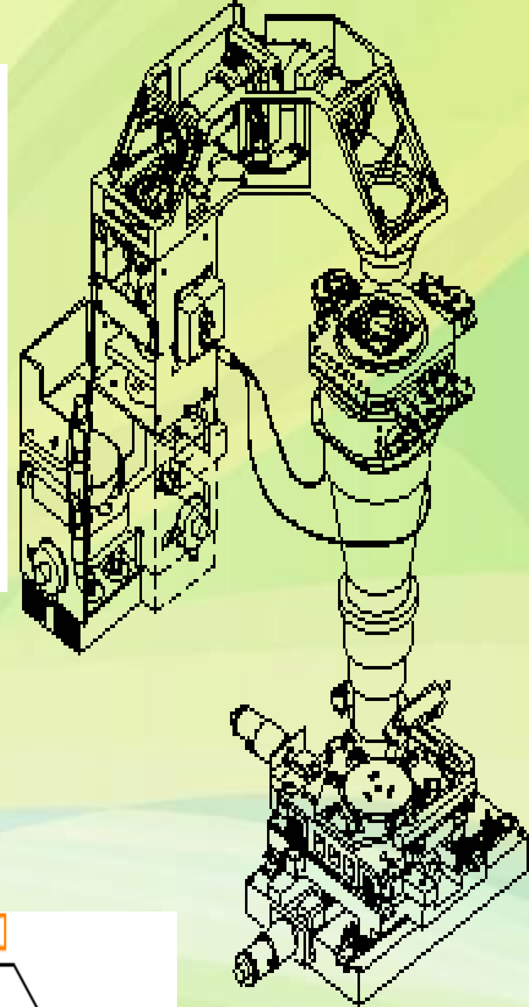
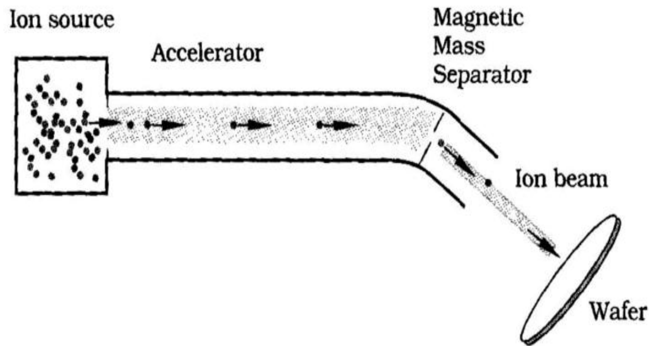


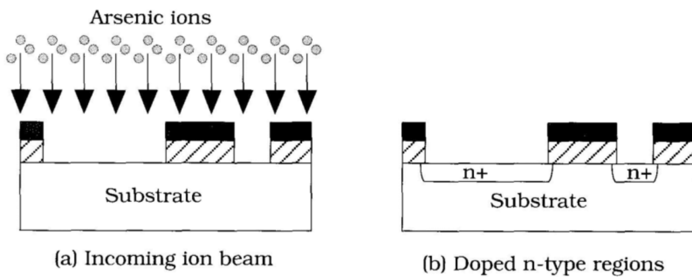
FIGURE 1.7 nMOS fabrication process.

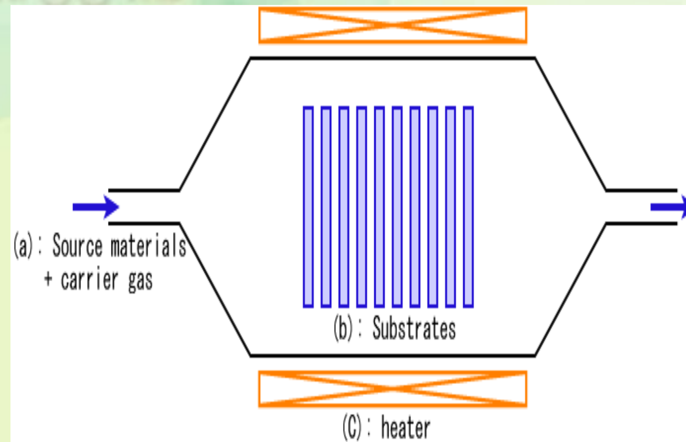

Photoresist spray
Spinning wafer
Vacuum chuck
(a) Resist application
Photoresist coating
(b) Coated wafer
Edge bead
Flat resist
Edge bead
Wafer
(c) Beading


UV
Reticle
Projection optics (not shown)
Reticle shadow
resist-coated wafer surface




Ion source
Accelerator
Magnetic Mass Separator
Ion beam
Wafer


Arsenic ions
Substrate
(a) Incoming ion beam
n+
n+
Substrate
(b) Doped n-type regions


(a): Source materials
+ carrier gas
(b): Substrates
(C): heater

1.7.1 Summary of An nMOS Process

- Processing takes place on a p-doped silicon crystal wafer on which is grown a 'thick' layer of SiO_2.
- *Mask* 1—Pattern SiO_2 to expose the silicon surface in areas where paths in the diffusion layer or gate areas of transistors are required. Deposit thin oxide over all. For this reason, this mask is often known as the *'thinox' mask* but some texts refer to it as the *diffusion mask*.
- *Mask* 2—Pattern the ion implantation within the thinox region where depletion mode devices are to be produced—*self-aligning*.
- *Mask* 3—Deposit polysilicon over all (1.5 µm thick typically), then pattern using Mask 3. Using the same mask, remove thin oxide layer where it is not covered by polysilicon.
- Diffuse n^+ regions into areas where thin oxide has been removed. Transistor drains and sources are thus self-aligning with respect to the gate structures.
- *Mask* 4—Grow thick oxide over all and then etch for contact cuts.
- *Mask* 5—Deposit metal and pattern with Mask 5.
- *Mask* 6—Would be required for the overglassing process step.

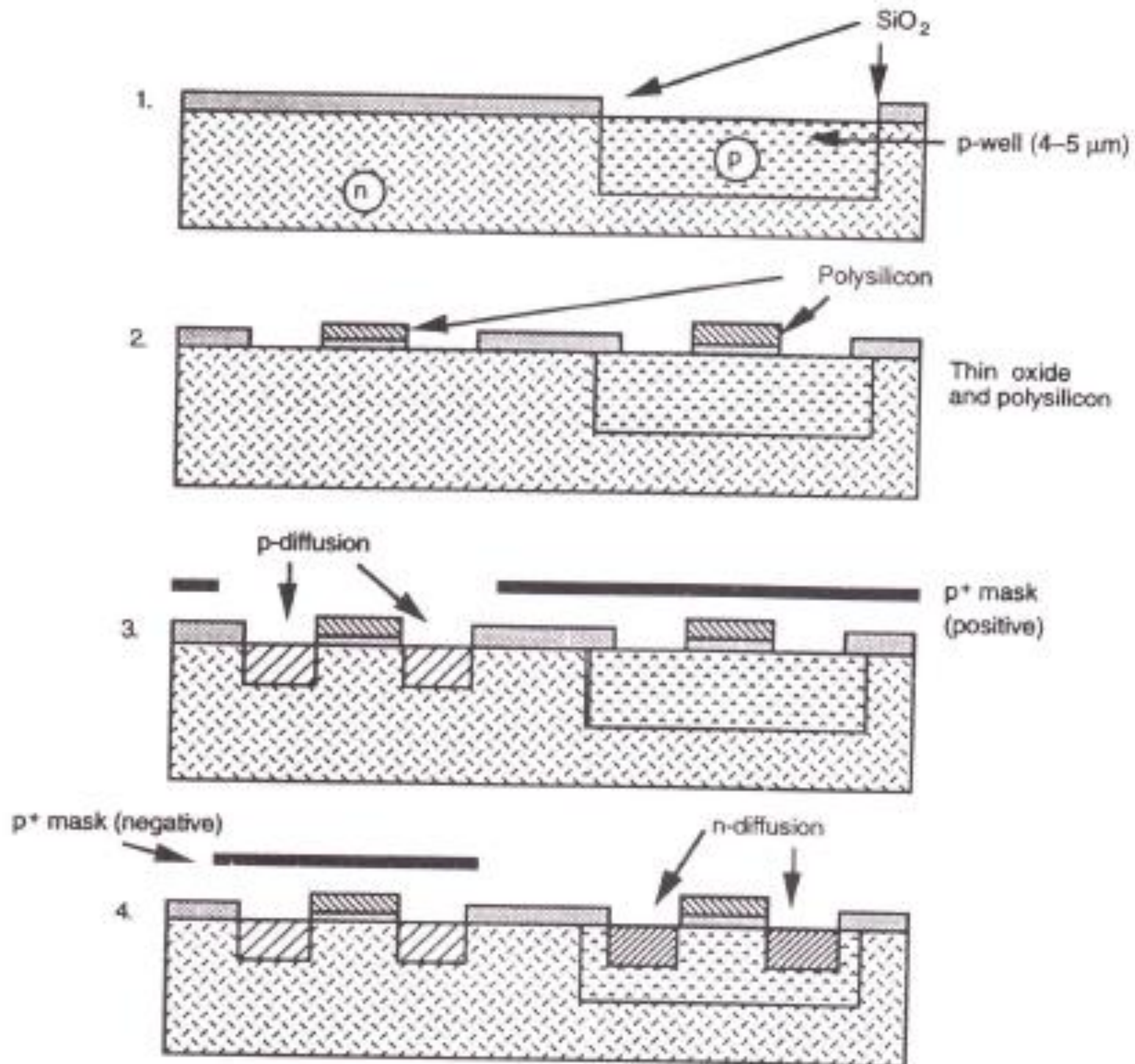


FIGURE 1.9 CMOS p-well process steps.

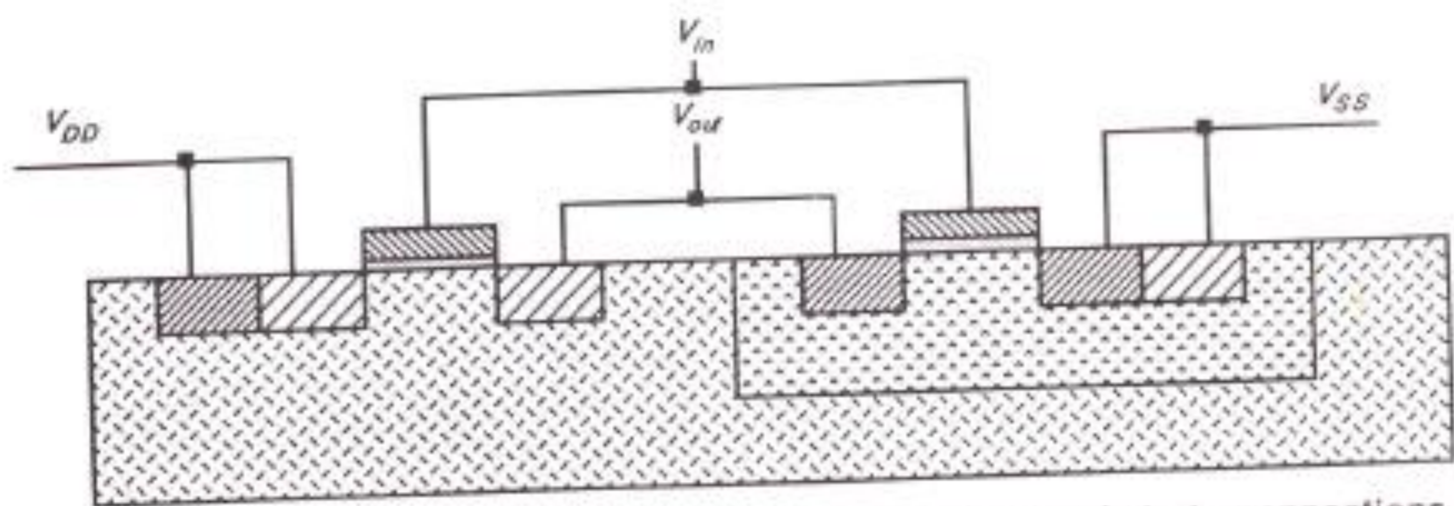


FIGURE 1.10 **CMOS p-well inverter showing V_{DD} and V_{SS} substrate connections.**

In all other respects—masking, patterning, and diffusion—the process is similar to nMOS fabrication. In summary, typical processing steps are:

- *Mask* 1 — defines the areas in which the deep p-well diffusions are to take place.
- *Mask 2* — defines the thinox regions, namely those areas where the thick oxide is to be stripped and thin oxide grown to accommodate p- and n-transistors and wires.
- *Mask* 3 — used to pattern the polysilicon layer which is deposited after the thin oxide.
- *Mask* 4 — A p-plus mask is now used (to be in effect "Anded" with Mask 2) to define all areas where p-diffusion is to take place.
- *Mask* 5 — This is usually performed using the negative form of the p-plus mask and defines those areas where n-type diffusion is to take place.
- *Mask* 6 — Contact cuts are now defined.
- *Mask* 7 — The metal layer pattern is defined by this mask.
- *Mask* 8 — An overall passivation (overglass) layer is now applied and Mask 8 is needed to define the openings for access to bonding pads.

Formation of n-well regions

↓

Define nMOS and pMOS active areas

↓

Field and gate oxidations (thinox)

↓

Form and pattern polysilicon

↓

p^+ diffusion

↓

n^+ diffusion

↓

Contact cuts

↓

Deposit and pattern metallization

↓

Over glass with cuts for bonding pads

↓

GURE 1.11 Main steps in a typical n-well process.

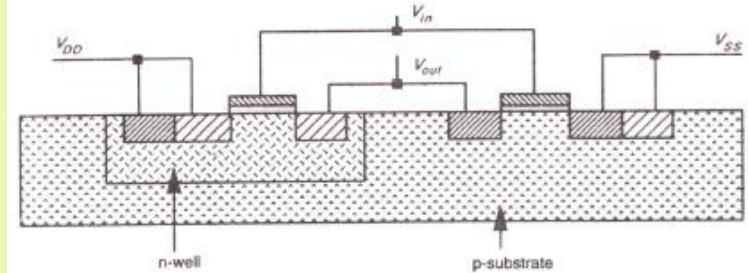


FIGURE 1.12 Cross-sectional view of n-well CMOS inverter.

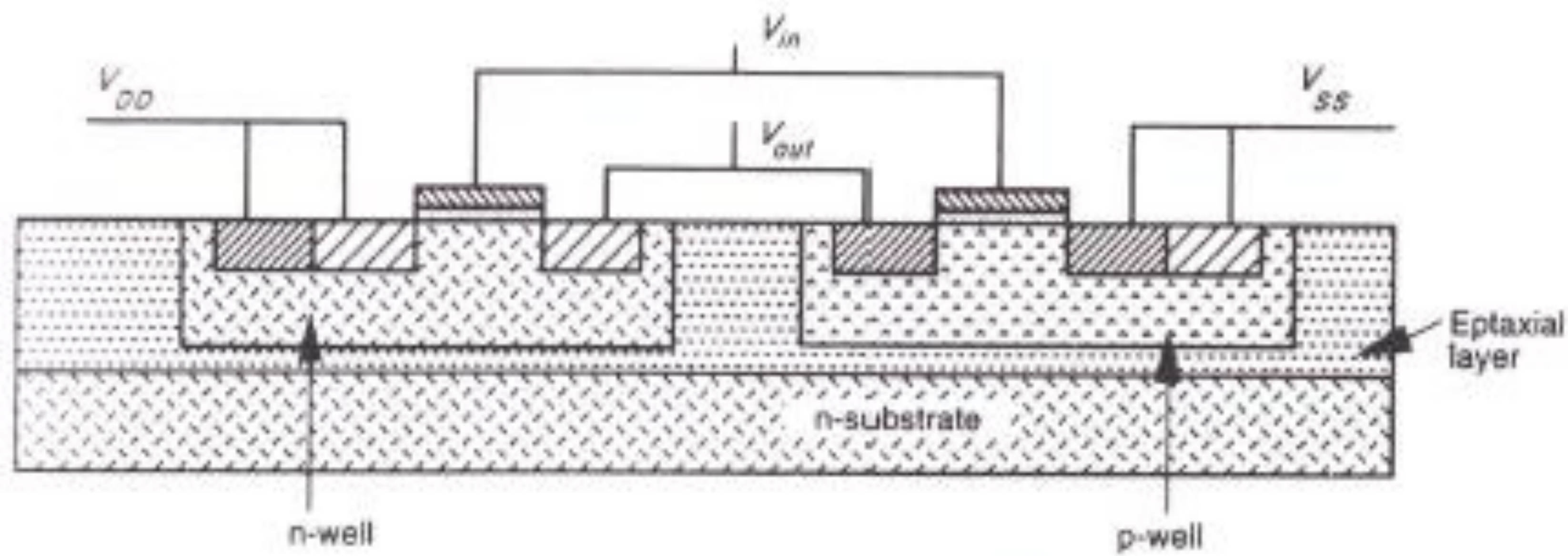
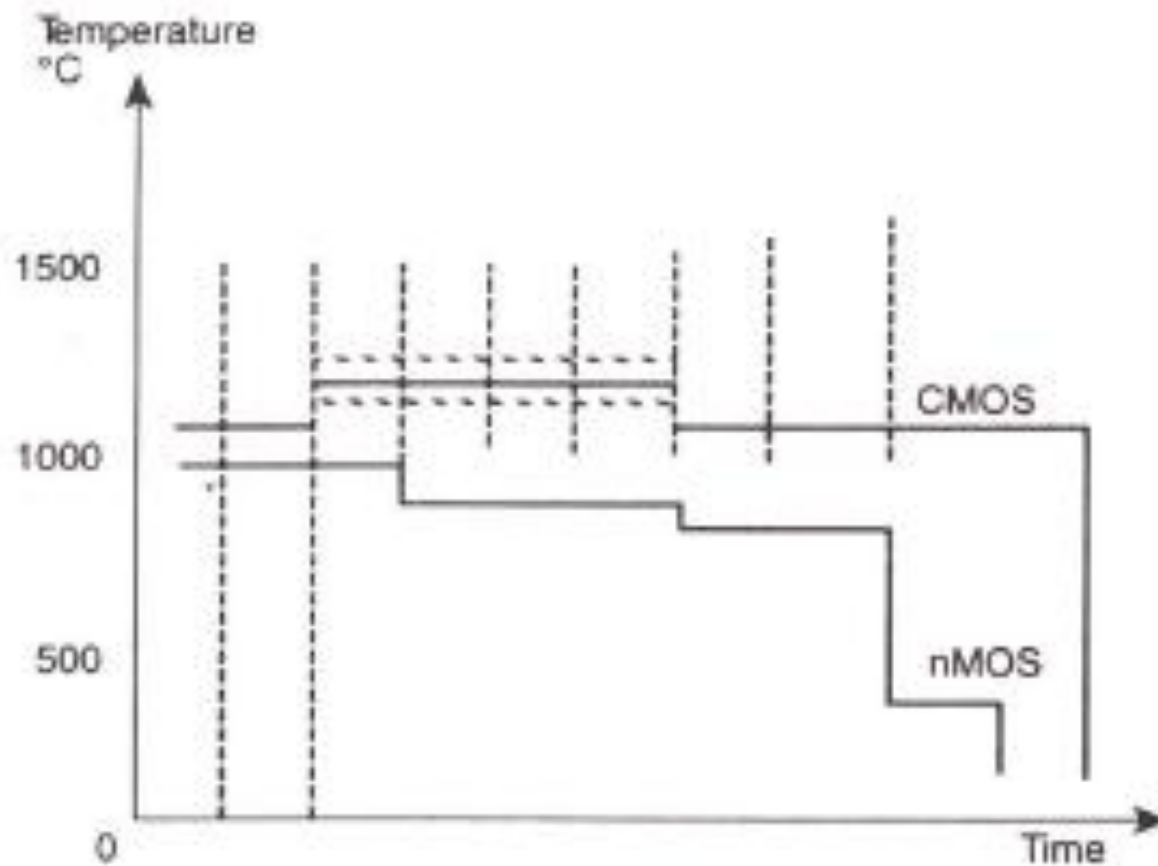


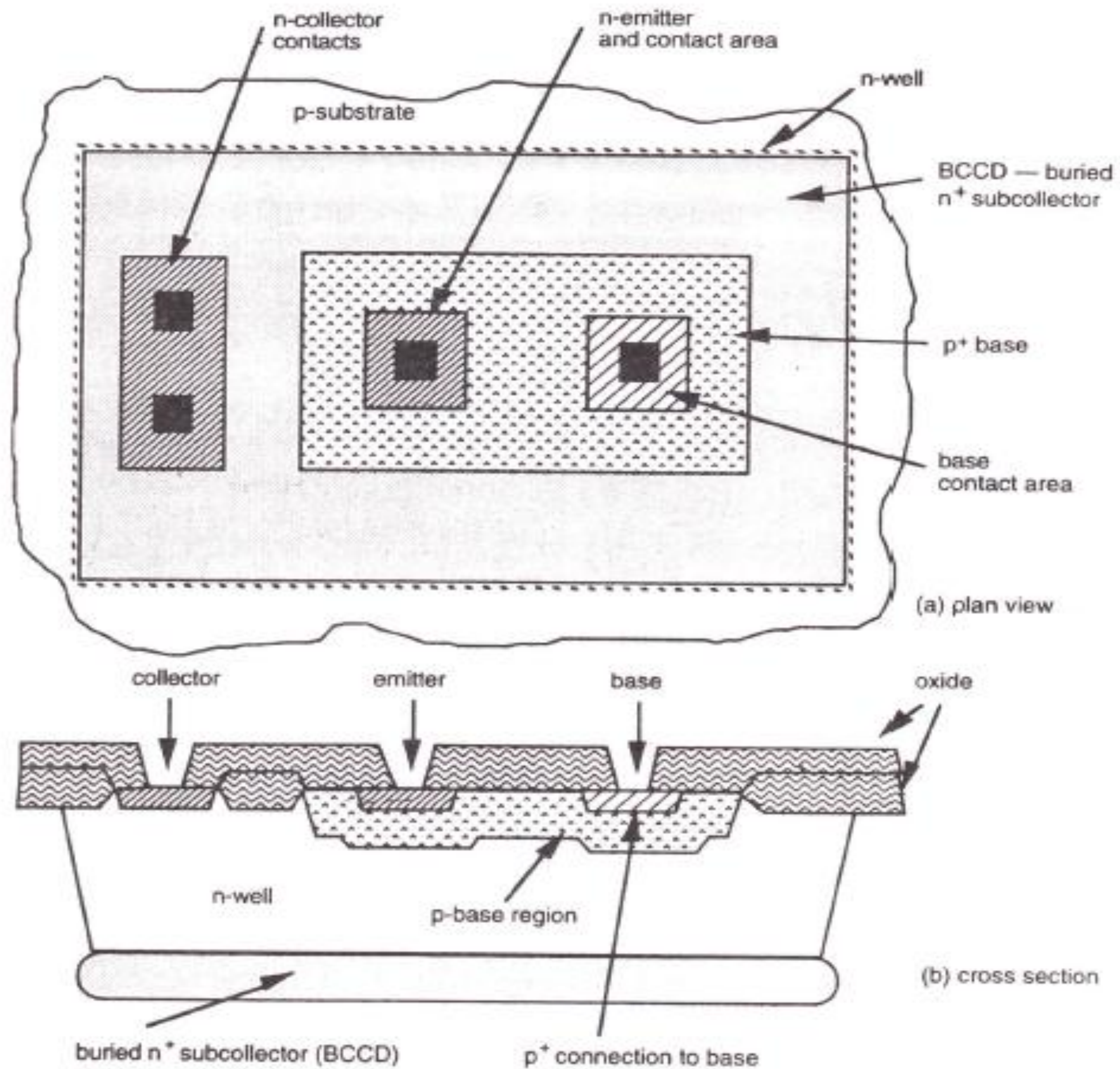
FIGURE 1.14 Twin-tub structure.



Thermal sequence difference between nMOS and CMOS processes.

TABLE 1.2 Comparison between CMOS and bipolar technologies

CMOS technology	*Bipolar technology*
• Low static power dissipation	• High power dissipation
• High input impedance (low drive current)	• Low input impedance (high drive current)
• Scalable threshold voltage	
• High noise margin	• Low voltage swing logic
• High packing density	• Low packing density
• High delay sensitivity to load (fan-out limitations)	• Low delay sensitivity to load
• Low output drive current	• High output drive current
• Low g_m ($g_m \alpha V_{in}$)	• High g_m ($g_m \alpha e^{V_{in}}$)
	• High f_t at low currents
• Bidirectional capability (drain and source are interchangeable)	• Essentially unidirectional
• A near ideal switching device	



Note: For clarity, the layers have not been drawn transparent but BCCD underlies the entire area and the p^+ base underlies all within its boundary.

FIGURE 1.16 Arrangement of BiCMOS npn transistor (Orbit 2 μm CMOS).

TABLE 1.3 n-well BiCMOS fabrication process steps

Single poly. single metal CMOS	*Additional steps for bipolar devices*
• Form n-well	
	• Form buried n^+ layer (BCCD)
• Delineate active areas • Channel stop	
	• Form deep n^+ collector
• Threshold V_t adjustment • Delineate poly./gate areas • Form n^+ active areas • Form p^+ active areas	
	• Form p^+ base for bipolars
• Define contacts • Delineate the metal areas	

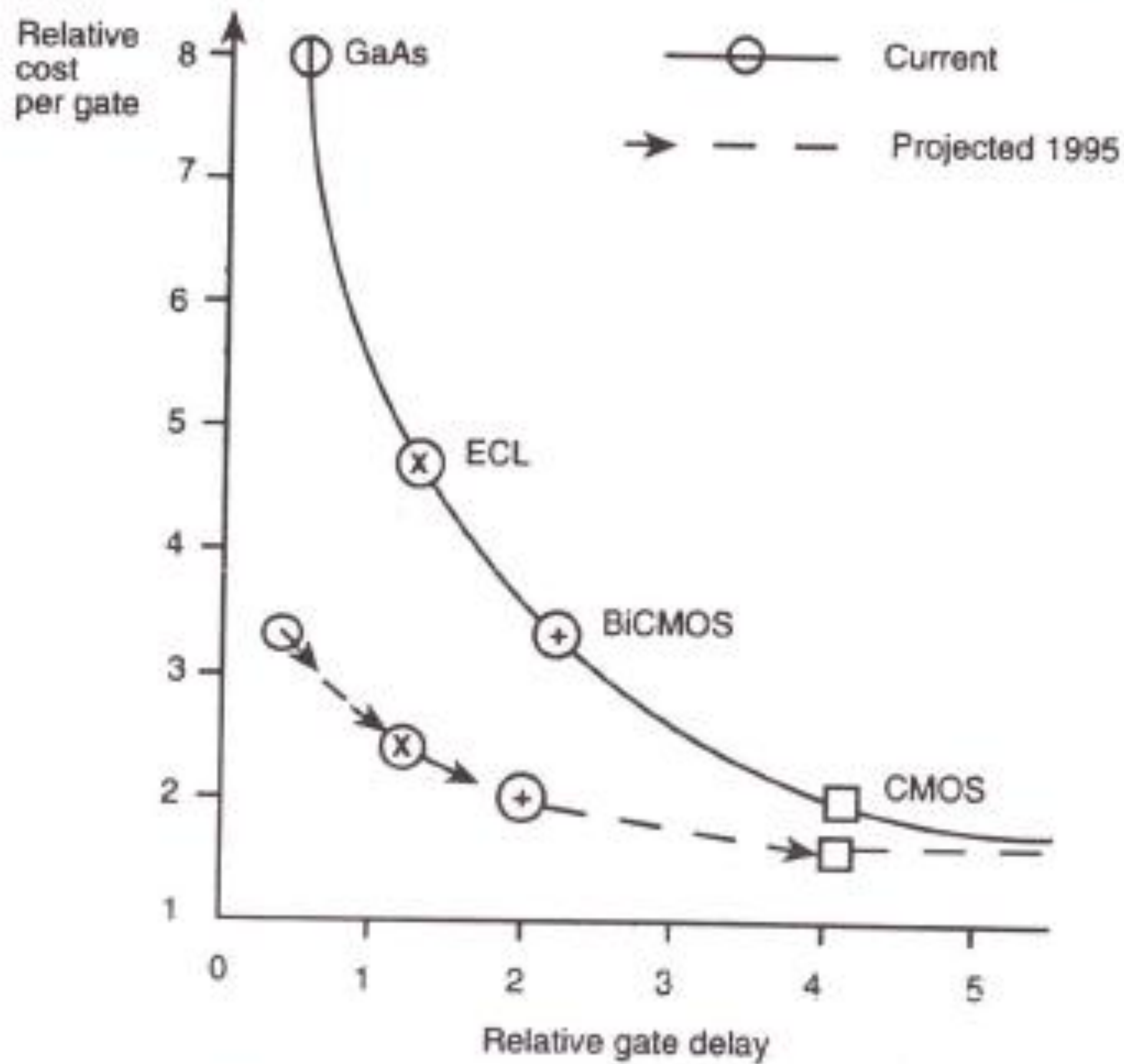


FIGURE 1.17 Cost versus delay for logic gate.

1.8.2 Advantages of BiCMOS over CMOS Technology

1. Using BiCMOS process, design of analog amplifier is possible.
2. Except input circuit, the remaining stages and output drivers are realized using bipolar transistors.
3. BiCMOS technology is used for I/O and driver circuits while CMOS technology is used for logic only.
4. BiCMOS technology is low delay sensitive to load.
5. BiCMOS has high output drive currents.

1.8.3 Comparison between CMOS, Bipolar and GaAs Technology

Sr. No.	Parameter	CMOS Technology	Bipolar Technology	GaAs Technology
1.	Static power dissipation	Low	High	Medium
2.	Input impedance	High	Low	High
3.	Noise margin	High	Medium	Low
4.	Voltage swing	High	Low	Low
5.	Operating speed	Medium	High	Very high
6.	Package density	High	Low	High
7.	Output drive current	Low	High	Low
8.	Directional capability	Bidirectional	Unidirectional	Bidirectional
9.	Suitability for switching	Ideal device	Not ideal device	Reasonable device
10.	Mask levels	12 to 16	12 to 20	6 to 10

Queries ...?