Module 2

Circuit Design Process Stick diagram and Layout

In this chapter we will be studying how to get the schematic into stick diagrams or layouts.
MOS circuits are formed on four basic layers:

N-diffusion
P-diffusion
Polysilicon
Metal

These layers are isolated by one another by thick or thin silicon dioxide insulating layers.
Thin oxide mask region includes n-diffusion / p-diffusion and transistor channel.

Stick diagrams:

Stick diagrams may be used to convey layer information through the use of a color code.
For example: n-diffusion --green
poly -- red
blue -- metal
yellow --implant
black --contact areas

Encodings for NMOS process:

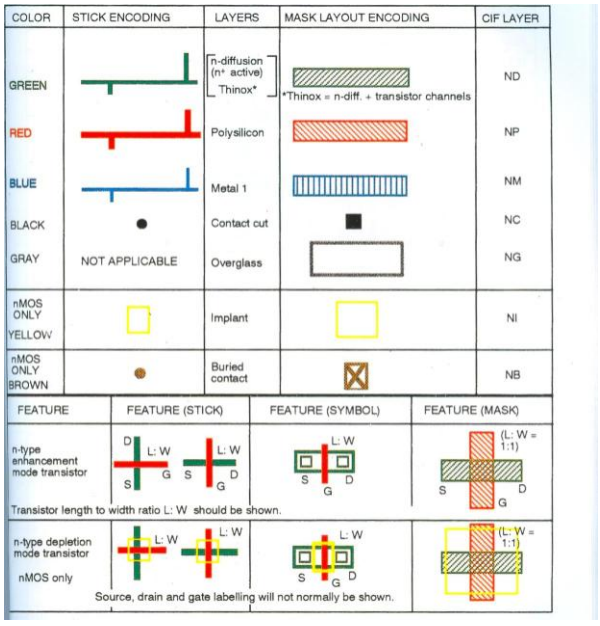

Figure 1: NMOS encodings

Figure shows the way of representing different layers in stick diagram notation and mask layout using nmos style.

Figure1 shows when a n-transistor is formed: a transistor is formed when a green line (n+ diffusion) crosses a red line (poly) completely. Figure also shows how a depletion mode transistor is represented in the stick format.

Encodings for CMOS process:

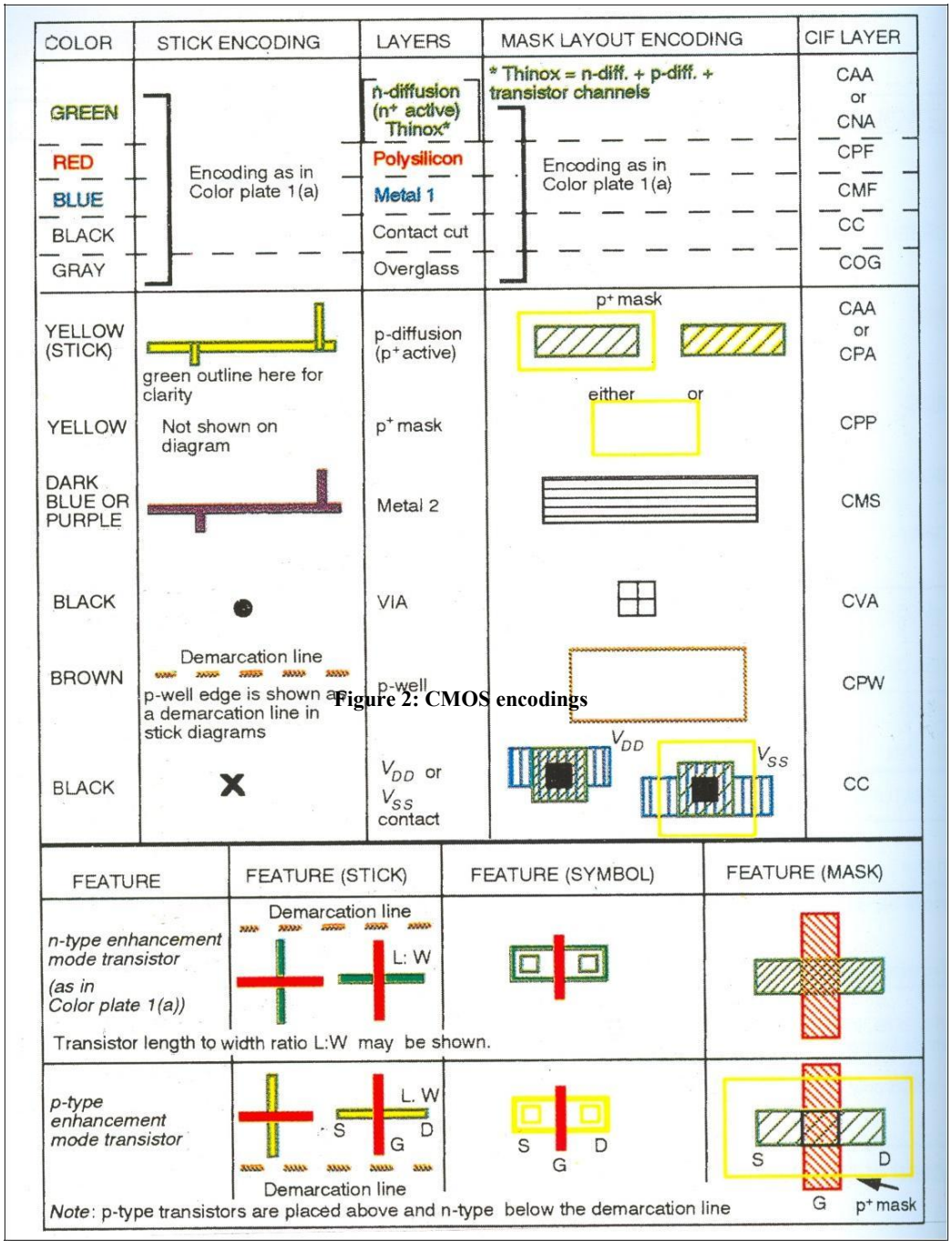

Figure 2: CMOS encodings

Figure 2 shows when a n-transistor is formed: a transistor is formed when a green line (n+ diffusion) crosses a red line (poly) completely.

Figure 2 also shows when a p-transistor is formed: a transistor is formed when a yellow line(p+ diffusion) crosses a red line (poly) completely.

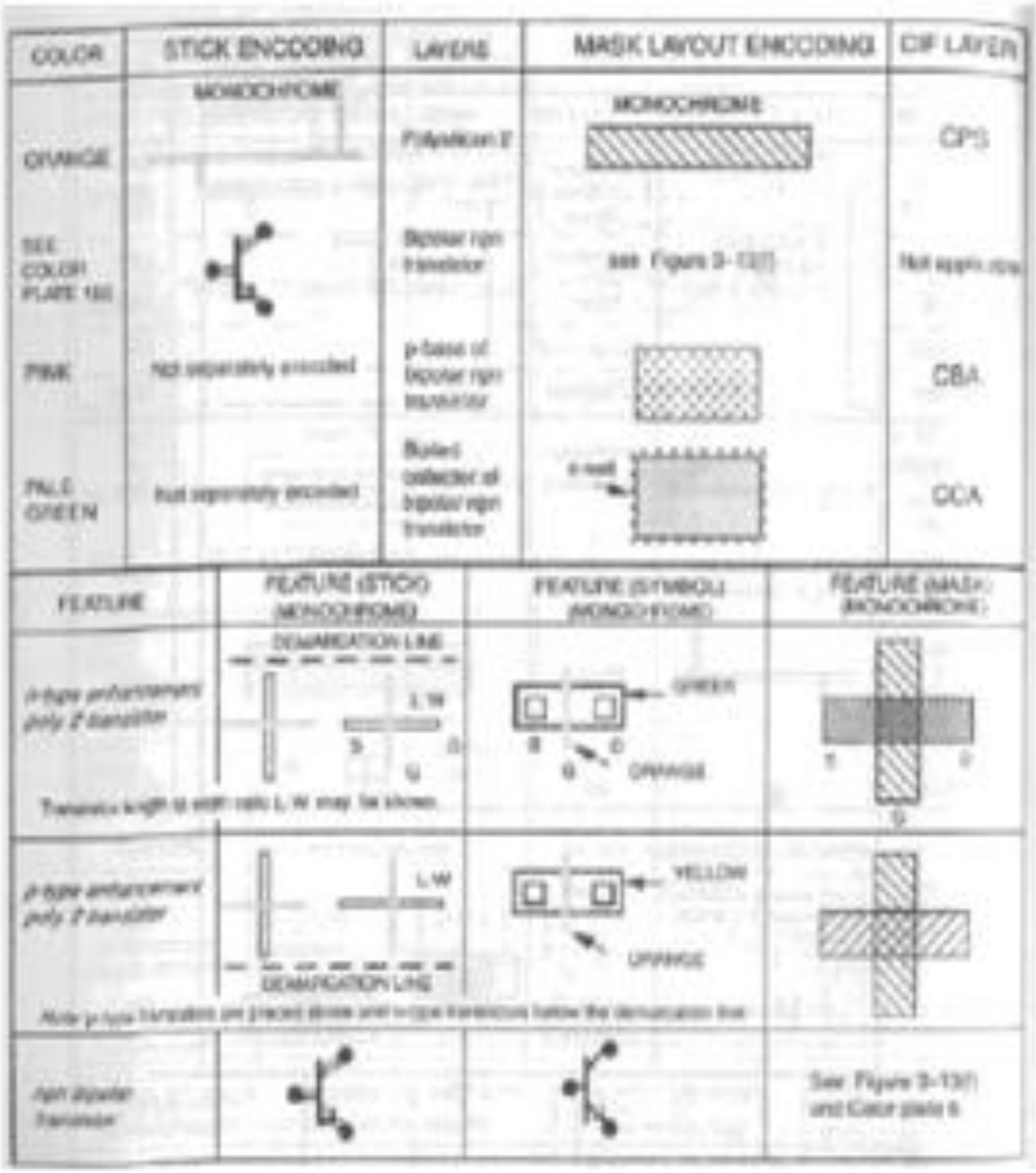

Figure 3: Bi CMOS encodings

There are several layers in an nMOS chip:

a p-type substrate
paths of n-type diffusion
a thin layer of silicon dioxide
paths of polycrystalline silicon
a thick layer of silicon dioxide
paths of metal (usually aluminium)
a further thick layer of silicon dioxide

with contact cuts through the silicon dioxide where connections are required.

The three layers carrying paths can be considered as independent conductors that only interact

where polysilicon crosses diffusion to form a transistor. These tracks can be drawn as stick

diagrams with

diffusion in green
polysilicon in red
metal in blue

using black to indicate contacts between layers and yellow to mark regions of implant in the channels of depletion mode transistors.

With CMOS there are two types of diffusion: n-type is drawn in green and p-type in brown.

These are on the same layers in the chip and must not meet. In fact, the method of fabrication required that they be kept relatively far apart.

Modern CMOS processes usually support more than one layer of metal. Two are common and three or more are often available.

Actually, these conventions for colors are not universal; in particular, industrial (rather than academic) systems tend to use red for diffusion and green for polysilicon. Moreover, a shortage of colored pens normally means that both types of diffusion in CMOS are colored green and the polarity indicated by drawing a circle round p-type transistors or simply inferred from the context. Colorings for multiple layers of metal are even less standard.

There are three ways that an nMOS inverter might be drawn:

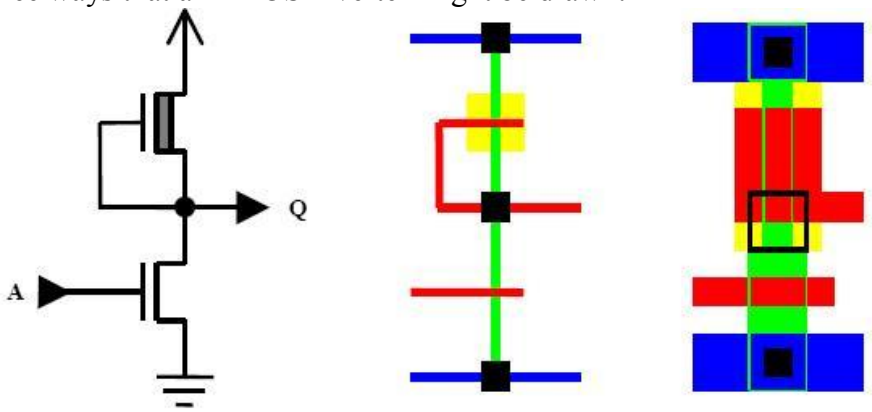

Figure 4: nMOS depletion load inverter

Figure.4 shows schematic, stick diagram and corresponding layout of nMOS depletion load inverter

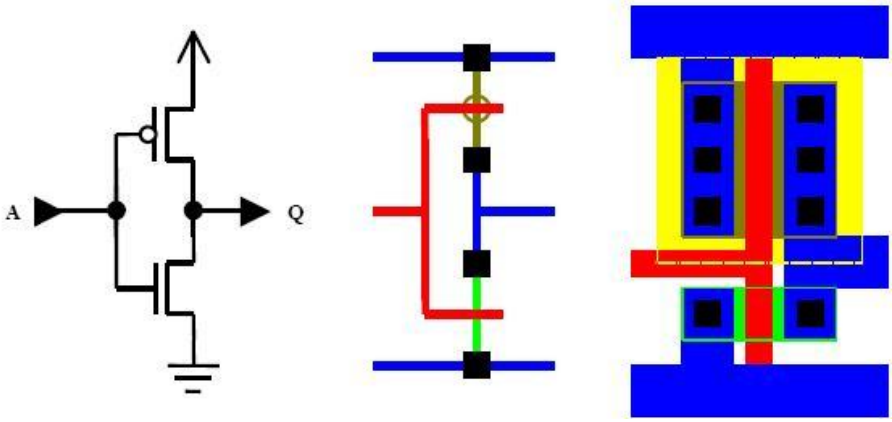

Figure 5: CMOS inverter

Figure 5 shows the schematic, stick diagram and corresponding layout of CMOS inverter

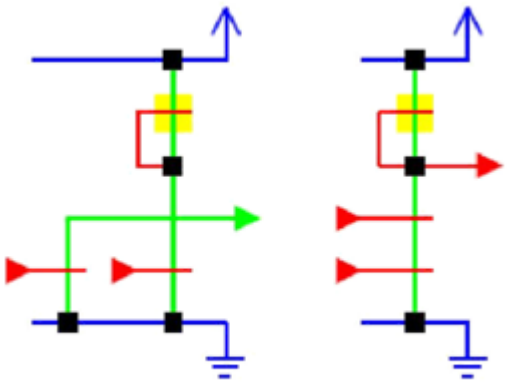

Figure 6: nMOS depletion load NAND and NOR stick diagram

Figure6 shows the stick diagrams for nMOS NOR and NAND.

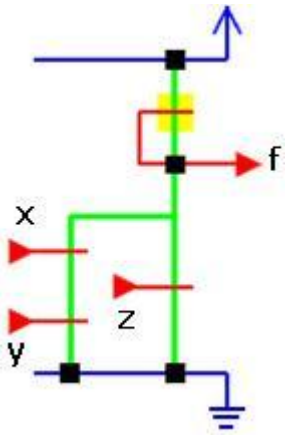

Figure 7: stick diagram of a given function f.

Figure 7 shows the stick diagram nMOS implementation of the function f=[(xy)+z]'

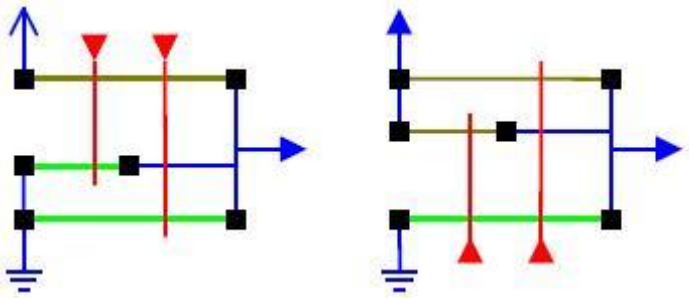

Figure 8: stick diagram of CMOS NAND and NOR

Figure 8 shows the stick diagram CMOS NOR and NAND, where we can see that the p diffusion line never touched the n diffusion directly, it is always joined using a blue color metal line.

NMOS and CMOS Design style:

In the NMOS style of representing the sticks for the circuit, we use only NMOS transistor, in CMOS we need to differentiate n and p transistor, that is usually by the color or in monochrome diagrams we will have a demarcation line. Above the demarcation line are the p transistors and below the demarcation are the n transistors

.

Following stick shows CMOS circuit example in monochrome where we utilize the demarcation line.

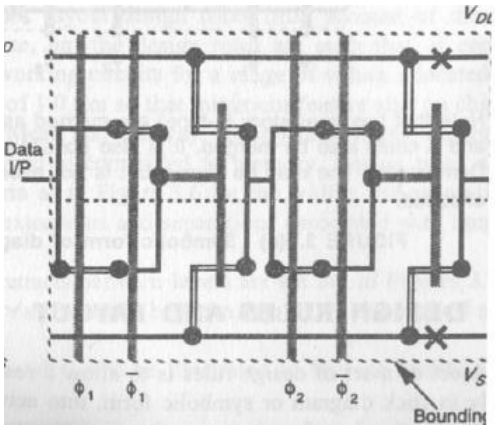

Figure 9: stick diagram of dyanmic shift register in CMOS style

Figure 9 shows the stick diagram of dynamic shift register using CMOS style. Here the output of the TG is connected as the input to the inverter and the same chain continues depending the number of bits.

Design Rules:

Design rules include width rules and spacing rules. Mead and Conway developed a set of simplified scalable λ -based design rules, which are valid for a range of fabrication technologies. In these rules, the minimum feature size of a technology is characterized as 2 λ . All width and spacing rules are specified in terms of the parameter λ . Suppose we have design rules that call for a minimum width of 2 λ , and a minimum spacing of 3 λ . If we select a 2 um technology (i.e., λ = 1 um), the above rules are translated to a minimum width of 2 um and a minimum spacing of 3 um. On the other hand, if a 1 um technology (i.e., λ = 0.5 um) is selected, then the same width and spacing rules are now specified as 1 um and 1.5 um, respectively.

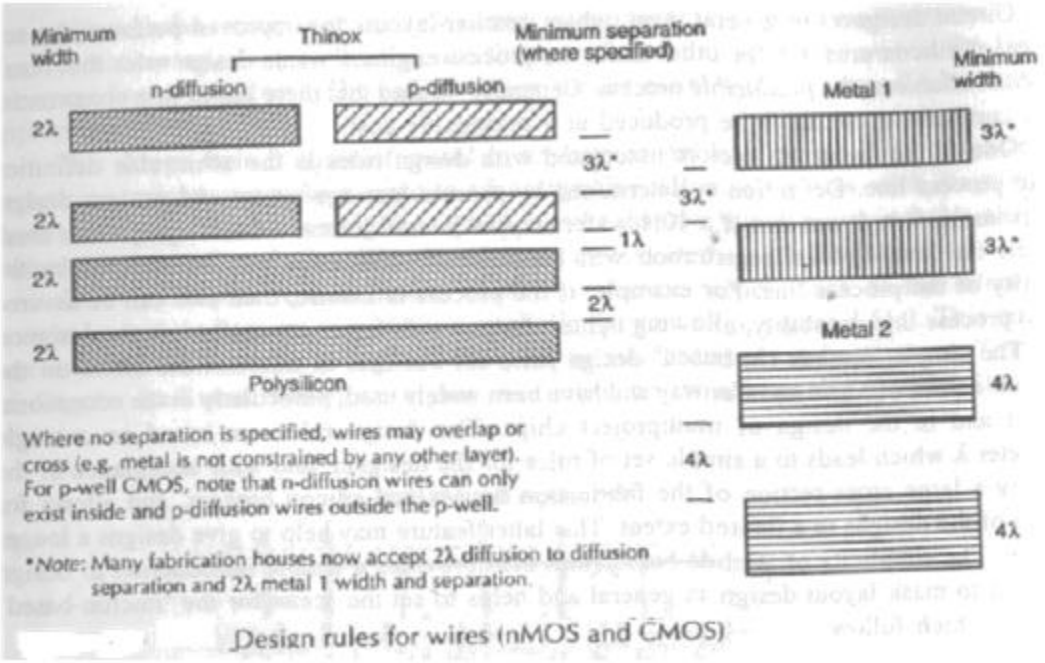

Figure 10: Design rules for the diffusion layers and metal lalyers

Figure 10 shows the design rule n diffusion, p diffusion, poly, metal1 and metal 2.

The n and p diffusion lines is having a minimum width of 2λ and a minimum spacing of 3λ. Similarly we are showing for other layers.

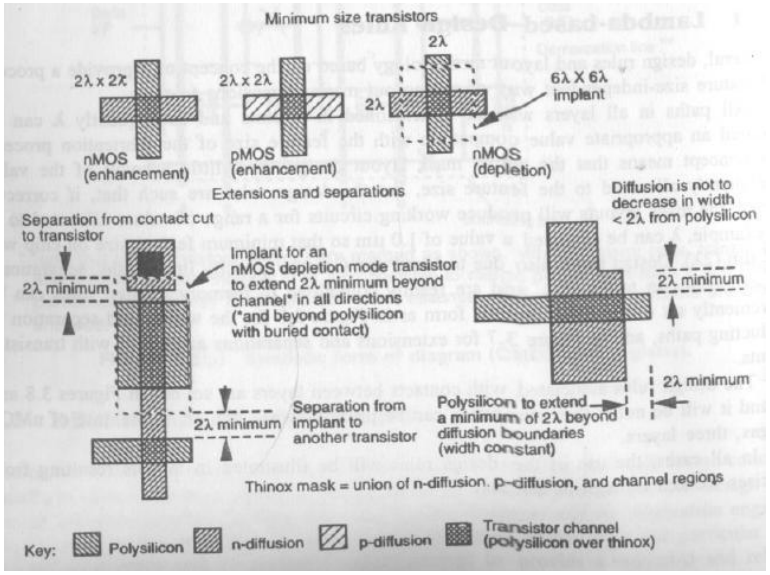

Figure 11: Design rules for transistors and gate over hang distance

Figure shows the design rule for the transistor, and it also shows that the poly should extend for a minimum of 2λ beyond the diffusion boundaries.(gate over hang distance)

What is Via?

It is used to connect higher level metals from metal1 connection. The cross section and layout view given figure 13 explain via in a better way.

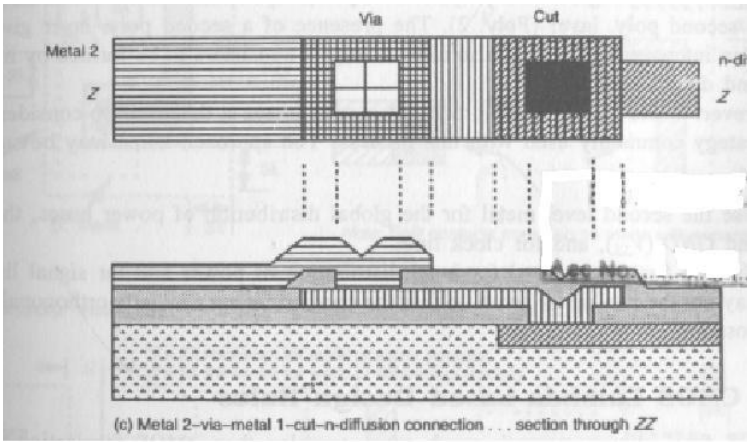

Figure 12: cross section showing the contact cut and via

Figure shows the design rules for contact cuts and Vias. The design rule for contact is minimum 2λx2λ and same is applicable for a Via.

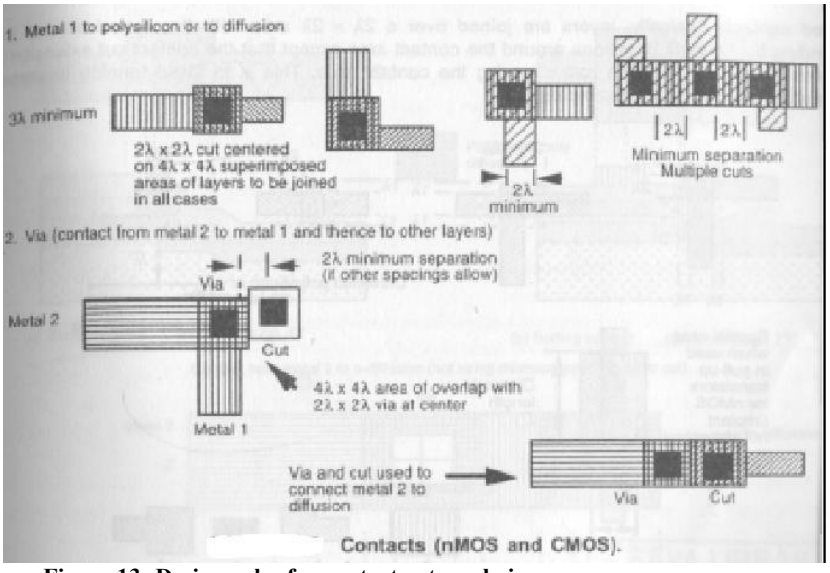

Figure 13: Design rules for contact cuts and vias

Buried contact: The contact cut is made down each layer to be joined and it is shown in figure 14.

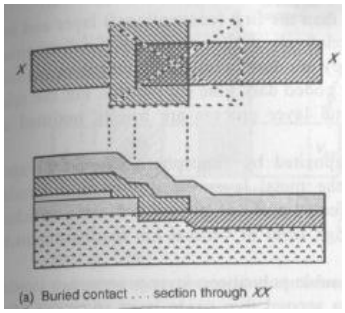

Figure 14: Buried contact

Butting contact: The layers are butted together in such a way the two contact cuts become contiguous. We can better under the butting contact from figure 15.

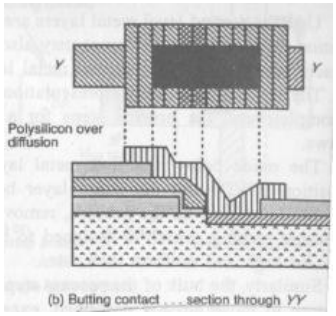

Figure 15: Butting contact

CMOS LAMBDA BASED DESIGN RULES:

Till now we have studied the design rules wrt only NMOS , what are the rules to be followed if we have the both p and n transistor on the same chip will be made clear with the diagram. Figure 16 shows the rules to be followed in CMOS well processes to accommodate both n and p transistors.

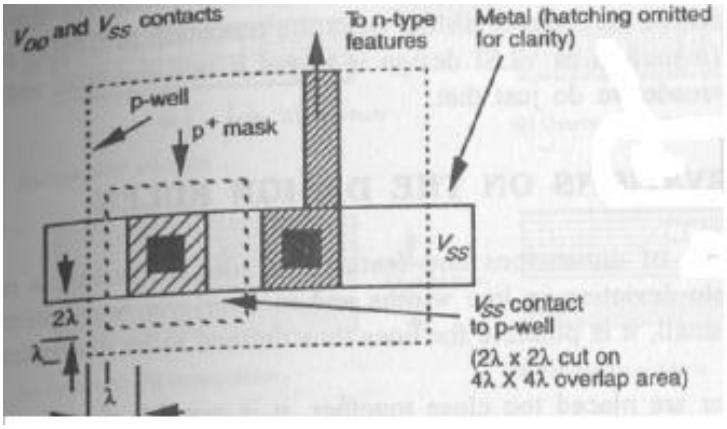

Figure 16: CMOS design rules

Orbit 2μm CMOS process:

In this process all the spacing between each layers and dimensions will be in terms micrometer. The 2μm here represents the feature size. All the design rules what ever we have seen will not have lambda instead it will have the actual dimension in micrometer.

In one way lambda based design rules are better compared micrometer based design rules, that is lambda based rules are feature size independent. Figure 17 shows the design rule for BiCMOS process using orbit 2um process.

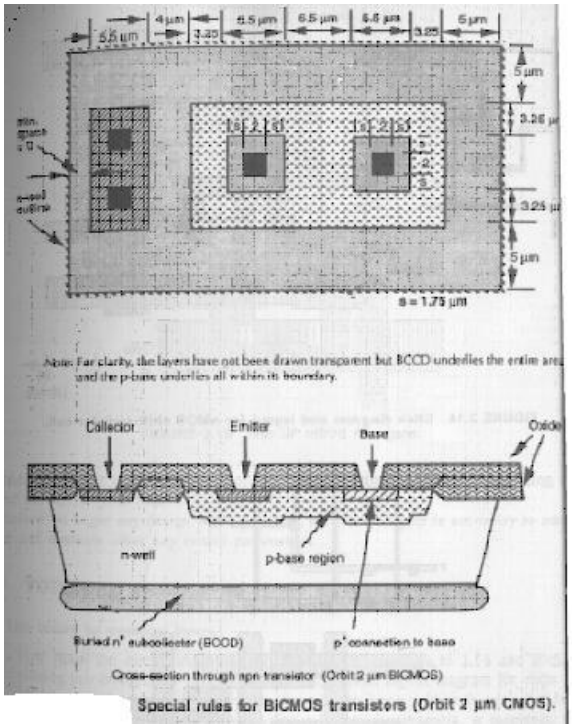

Figure 17: BiCMOS design rules

The following is the example stick and layout for 2way selector with enable(2:1 MUX).

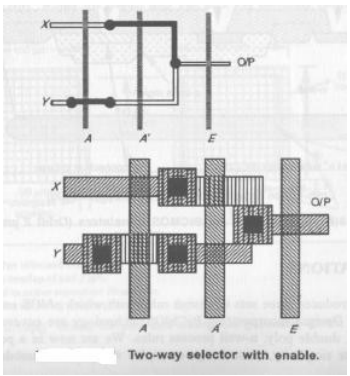

Figure 18: Two way selector stick and layout

SCHEMATIC AND LAYOUT OF BASIC GATES

1.CMOS INVERTERNOT GATE) SCHEMATIC

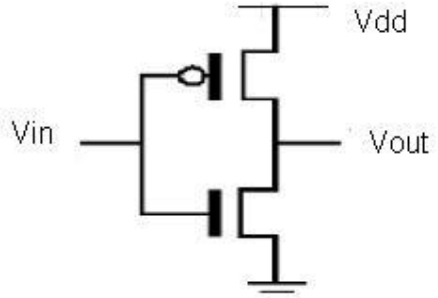

Figure 1 Inverter

TOWARDS THE LAYOUT

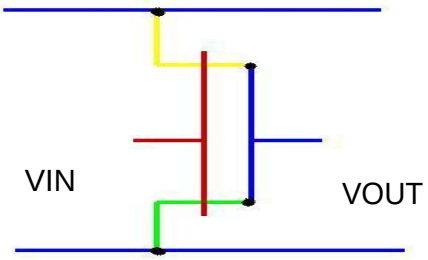

Figure2: Stick diagram of inverter

The diagram shown here is the stick diagram for the CMOS inverter. It consists of a Pmos and a Nmos connected to get the inverted output. When the input is low, Pmos (yellow)is on and pulls the output to vdd, hence it is called pull up device. When Vin =1,Nmos (green)is on it pulls Vout to Vss, hence Nmos is a pull down device. The red lines are the poly silicon lines connecting the gates and the blue lines are the metal lines for VDD(up) and VSS (down).The layout of the cmos inverter is shown below. Layout also gives the minimum dimensions of different layers, along with the logical connections and main thing about layouts is that can be simulated and checked for errors which cannot be done with only stick diagrams.

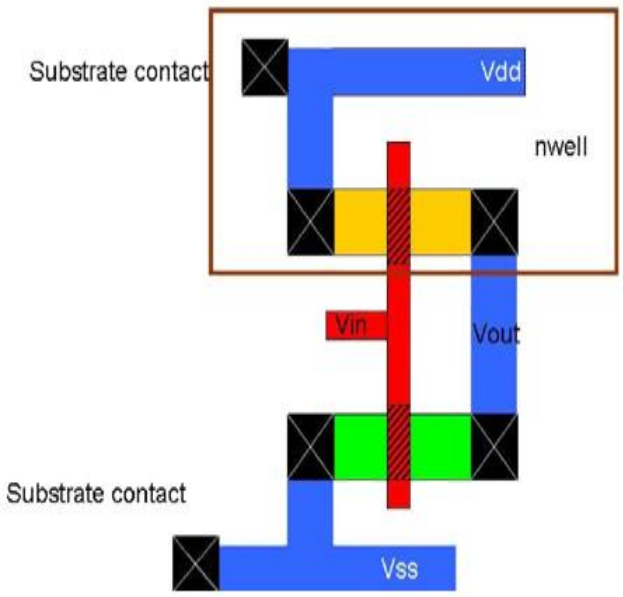

Figure 3: Layout of an inverter

The layout shown above is that of a CMOS inverter. It consists of a pdiff (yellow colour) forming the pmos at the junction of the diffusion and the polysilicon(red colour)shown hatched ndiff(green) forming the nmos(area hatched).The different layers drawn are checked for their dimensions using the DRC rule check of the tool used for drawing. Only after the DRC(design rule check) is passed the design can proceed further. Further the design undergoes Layout Vs Schematic checks and finally the parasitic can be extracted.

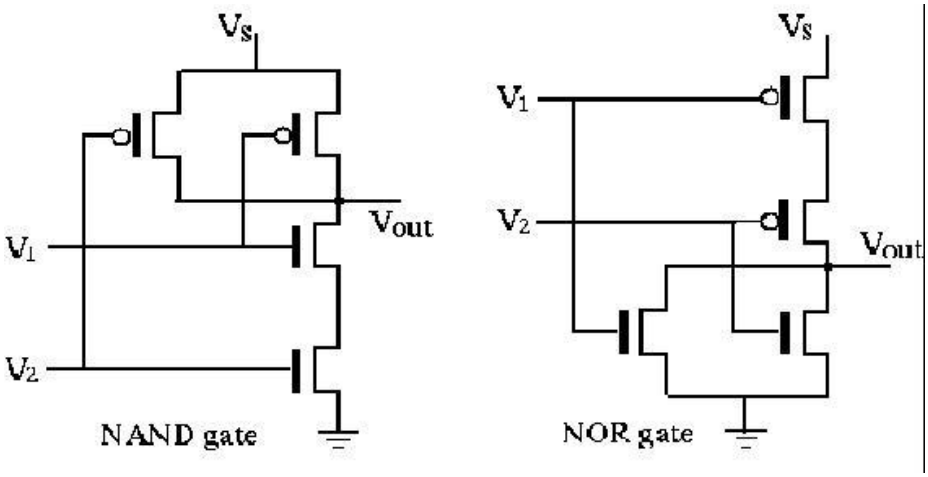

Figure 4:Schematic diagrams of nand and nor gate

We can seen that the nand gate consists of two pmos in parallel which forms the pull up logic and two nmos in series forming the pull down logic.It is the complementary for the nor gate. We get inverted logic from cmos structures. The series and parallel connections are for getting the right logic output. The pull up and the pull down devices must be placed to get high and low outsputs when required.

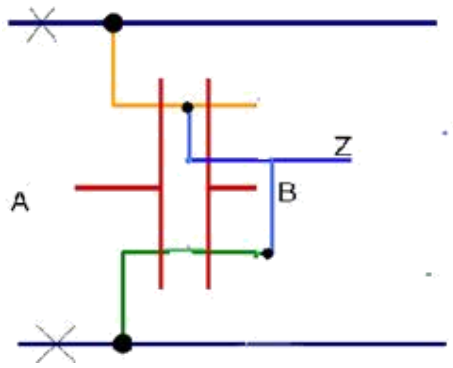

Figure 5: Stick diagram of nand gate

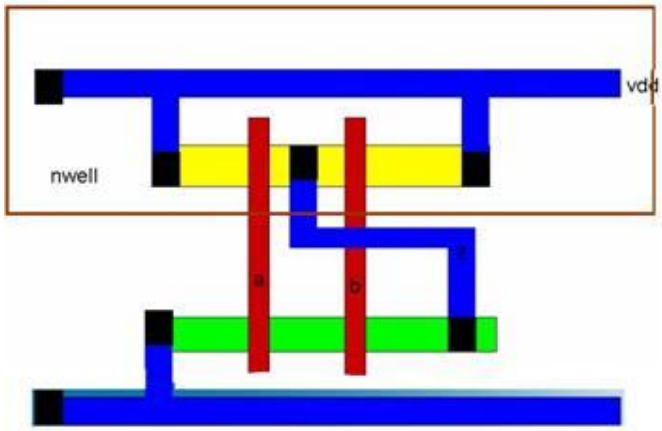

Figure 6: Layout f a nand gate

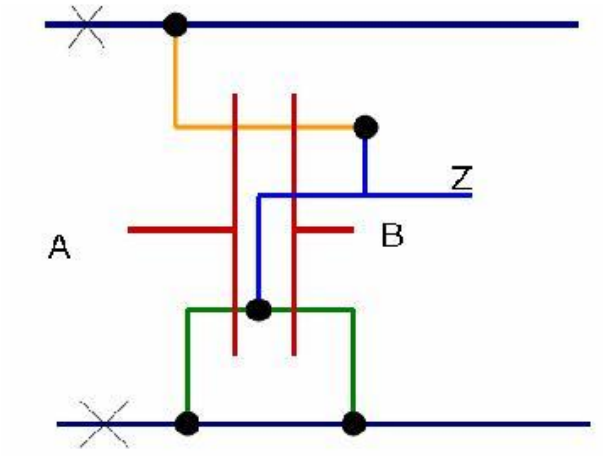

Figure 7:Stick diagram of nor gate

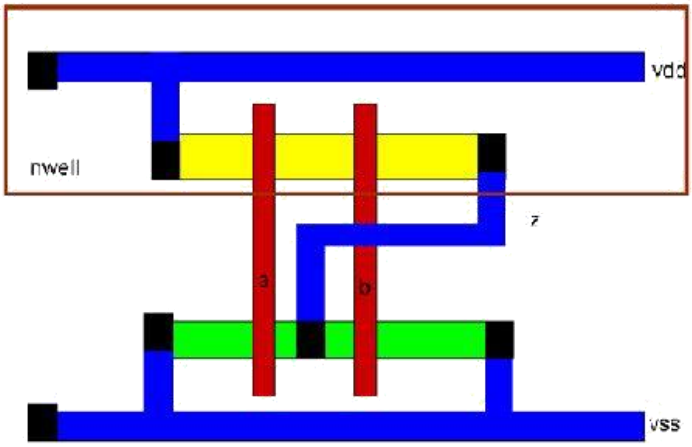

Figure 8: Layout of nor gate

TRANSMISSION GATE

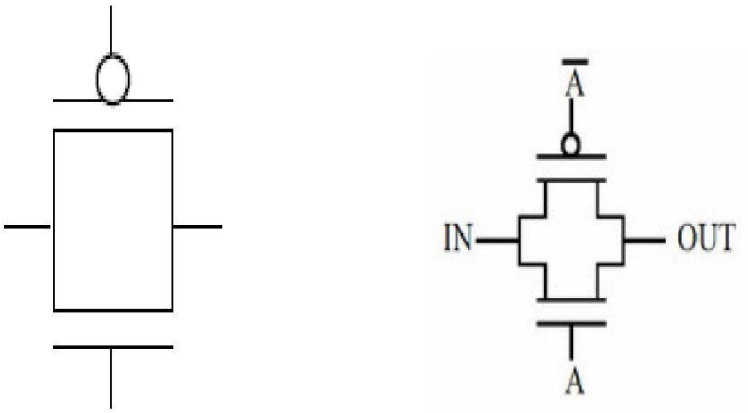

Figure 9 :Symbol and schematic of transmission gate

Layout considerations of transmission gate. It consist of drains and the sources of the P&N devices paralleled. Transmission gate can replace the pass transistors and has the advantage of giving both a good one and a good zero.

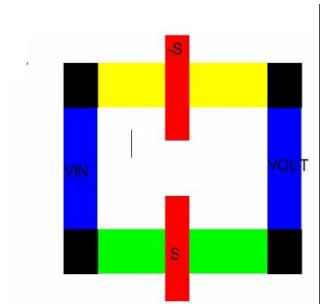

Figure 10: Layout of transmissuion gate

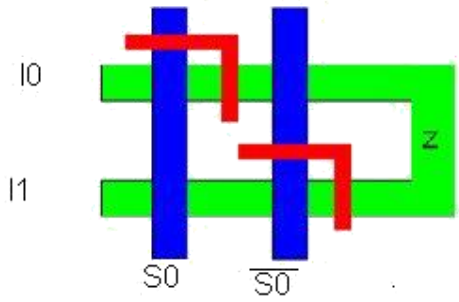

Figure 11:TG with nmos switches

CMOS STANDARD CELL DESIGN

Geometric regularity is very important to maintain some common electrical characteristics between the cells in the library. The common physical limitation is to fix the height and vary the width according to the required function. The Wp and Wn are fixed considering power dissipation, propagation delay, area and noise immunity. The best thing to do is to fix a required objective function and then fix Wn and Wp to obtain the required objective

Usually in CMOS Wn is made equal to Wp . In the process of designing these gates techniques may be employed to automatically generate the gates of common size. Later optimization can be carried out to achieve a specific feature. Gate array layout and sea of gate layout are constructed using the above techniques. The gate arrays may be customized by having routing channels in between array of gates. The gate array and the sea of gates have some special layout considerations. *The gate arrays* use fixed image of the under layers i.e the diffusion and poly are fixed and metal are programmable. The wiring layers are discretionary and providing the personalization of the array. The rows of transistors are fixed and the routing channels are provided in between them. Hence the design issues involves size of transistors, connectivity of poly and the number of routing channels required.

Sea of gates in this style continuous rows of n and p diffusion run across the master chip and are arranged without regard to the routing channel. Finally the routing is done across unused transistors saving space.

GENERAL LAYOUT GUIDELINES

1.The electrical gate design must be completed by checking the following

a.Right power and ground supplies

b.Noise at the gate input

c.Faulty connections and transistors

d.Improper ratios

c.Incorrect clocking and charge sharing

2.VDD and the VSS lines run at the top and the bottom of the design

3.Vertical poysilicon for each gate input

4.Order polysilicon gate signals for maximal connection between transistors

5.The connectivity requires to place nmos close to VSS and pmos close to VDD

6.Connection to complete the logic must be made using poly,metal and even metal2

The design must always proceeds towards optimization. Here optimization is at transistor level rather then gate level. Since the density of transistors is large ,we could obtain smaller and faster layout by designing logic blocks of 1000 transistors instead of considering a single at a time and then putting them together. Density improvement can also be made by considering optimization of the other factors in the layout

The factors are

1.Efficient routing space usage. They can be placed over the cells or even in multiple layers.

2.Source drain connections must be merged better.

3.White (blank) spaces must be minimum

4.The devices must be of optimum sizes.

5.Transperent routing can be provided for cell to cell interconnection, this reduces global wiring problems

connected in parallel ,we must try and reduce the number of drains in parallel ie wherever possible we must try and connect drains in series at least at the output.This arrangement could reduce the capacitance at the output enabling good voltage levels. One example is as shown next.

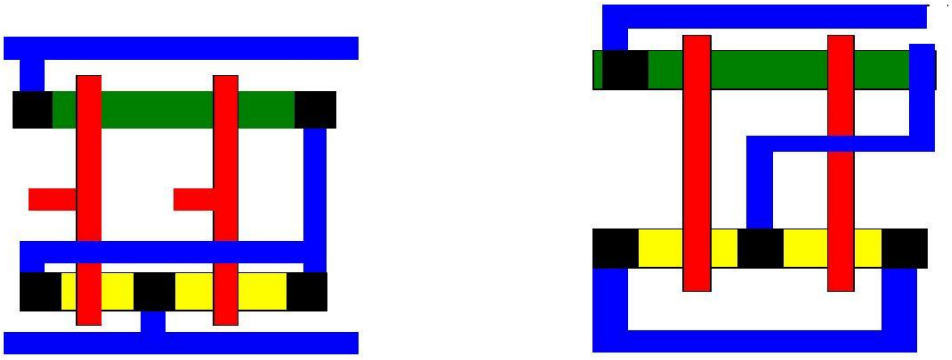

Figure 13 Layout of nor gate showing series and parallel drains.