Module 1

Basic MOS Technology

Transistor was first invented by William. B. Shockley, Walter Brattain and John Bardeen of Bell Laboratories. In 1961, first IC was introduced.

Levels of Integration:-

i) SSI:- (10-100) transistors => Example: Logic gates
ii) MSI:- (100-1000) => Example: counters
iii) LSI:- (1000-20000) => Example:8-bit chip
iv) VLSI:- (20000-1000000) => Example:16 & 32 bit up
v) ULSI:- (1000000-10000000) => Example: Special processors, virtual reality machines, smart sensors

Moore's Law:-
"The number of transistors embedded on the chip doubles after every one and a half years." The number of transistors is taken on the y-axis and the years in taken on the x-axis. The diagram also shows the speed in MHz. the graph given in figure also shows the variation of speed of the chip in MHz.

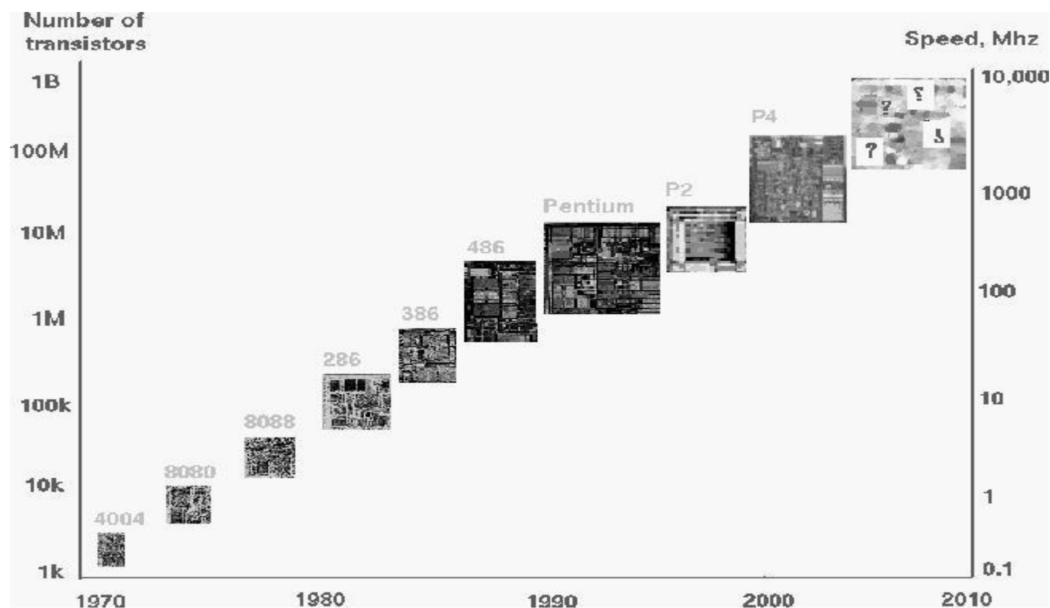


Figure 1. Moore's law

The graph in figure2 compares the various technologies available in ICs.

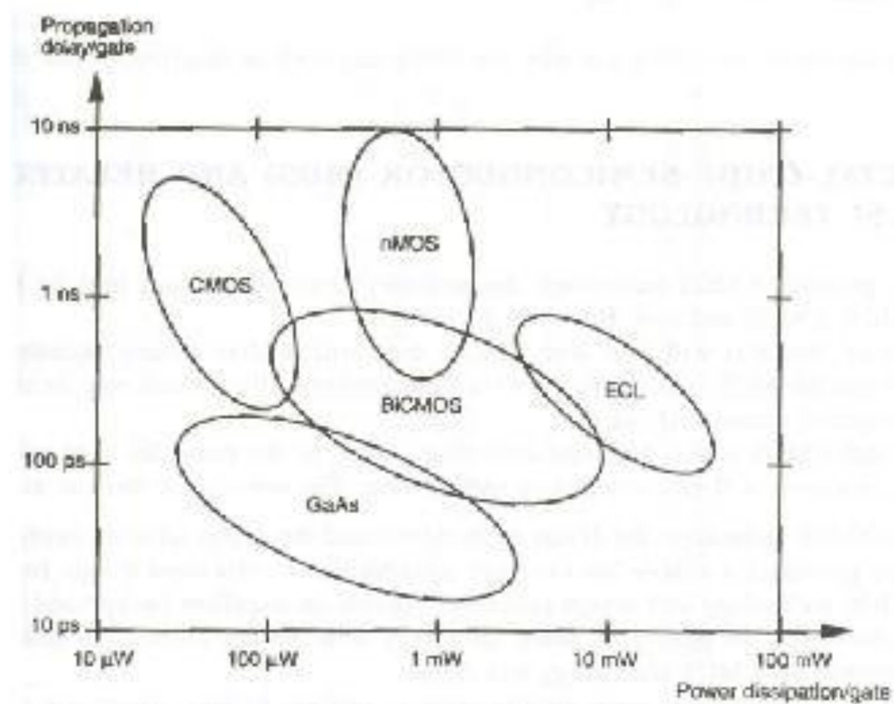


Figure 2.Comparison of available technologies

From the graph we can conclude that GaAs technology is better but still it is not used because of growing difficulties of GaAs crystal. CMOS looks to be a better option compared to nMOS since it consumes a lesser power. BiCMOS technology is also used in places where high driving capability is required and from the graph it confirms that, BiCMOS consumes more power compared to CMOS.

Levels of Integration:-

i) Small Scale Integration:- (10-100) transistors => Example: Logic gates
ii) Medium Scale Integration:- (100-1000) => Example: counters
iii) Large Scale Integration:- (1000-20000) => Example:8-bit chip
iv) Very Large Scale Integration:- (20000-1000000) => Example:16 & 32 bit up
v) Ultra Large Scale Integration:- (1000000-10000000) => Example: Special processors, virtual reality machines, smart sensors

Basic MOS Transistors:

<u>Why the name MOS?</u>

We should first understand the fact that why the name Metal Oxide Semiconductor transistor, because the structure consists of a layer of Metal (gate), a layer of oxide (Sio2) and a layer of semiconductor. Figure 3 below clearly tell why the name MOS.

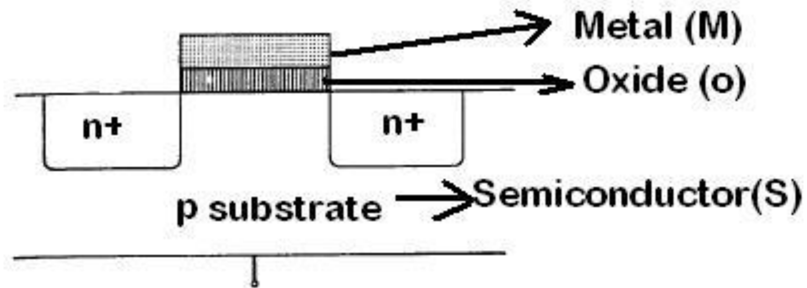


Figure 3.cross section of a MOS structure

We have two types of FETs. They are Enhancement mode and depletion mode transistor. Also we have PMOS and NMOS transistors.

In **Enhancement mode transistor** channel is going to form after giving a proper positive gate voltage. We have NMOS and PMOS enhancement transistors.

In **Depletion mode transistor** channel will be present by the implant. It can be removed by giving a proper negative gate voltage. We have NMOS and PMOS depletion mode transistors.

N-MOS enhancement mode transistor:-

This transistor is normally off. This can be made ON by giving a positive gate voltage. By giving a +ve gate voltage a channel of electrons is formed between source drain.

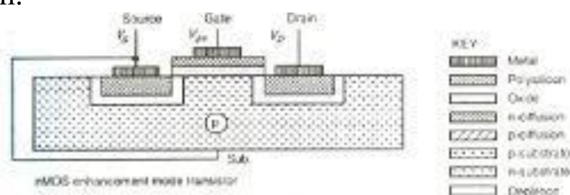


Fig 5. Nmos Enhancement transistor

P-Mos enhancement mode transistors:-

This is normally on. A Channel of Holes can be performed by giving a –ve gate voltage. In P-Mos current is carried by holes and in N-Mos its by electrons. Since the mobility is of holes less than that of electrons P-Mos is slower.

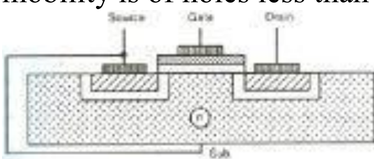


Fig 6. Pmos Enhancement transistor

N-MOS depletion mode transistor:-

This transistor is normally ON, even with Vgs=0. The channel will be implanted while fabricating, hence it is normally ON. To cause the channel to cease to exist, a –ve voltage must be applied between gate and source.

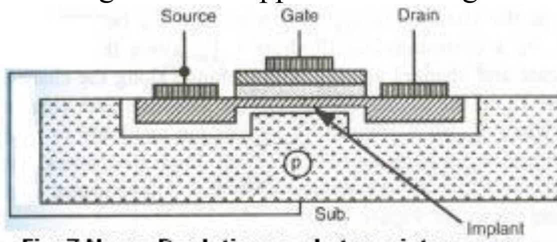
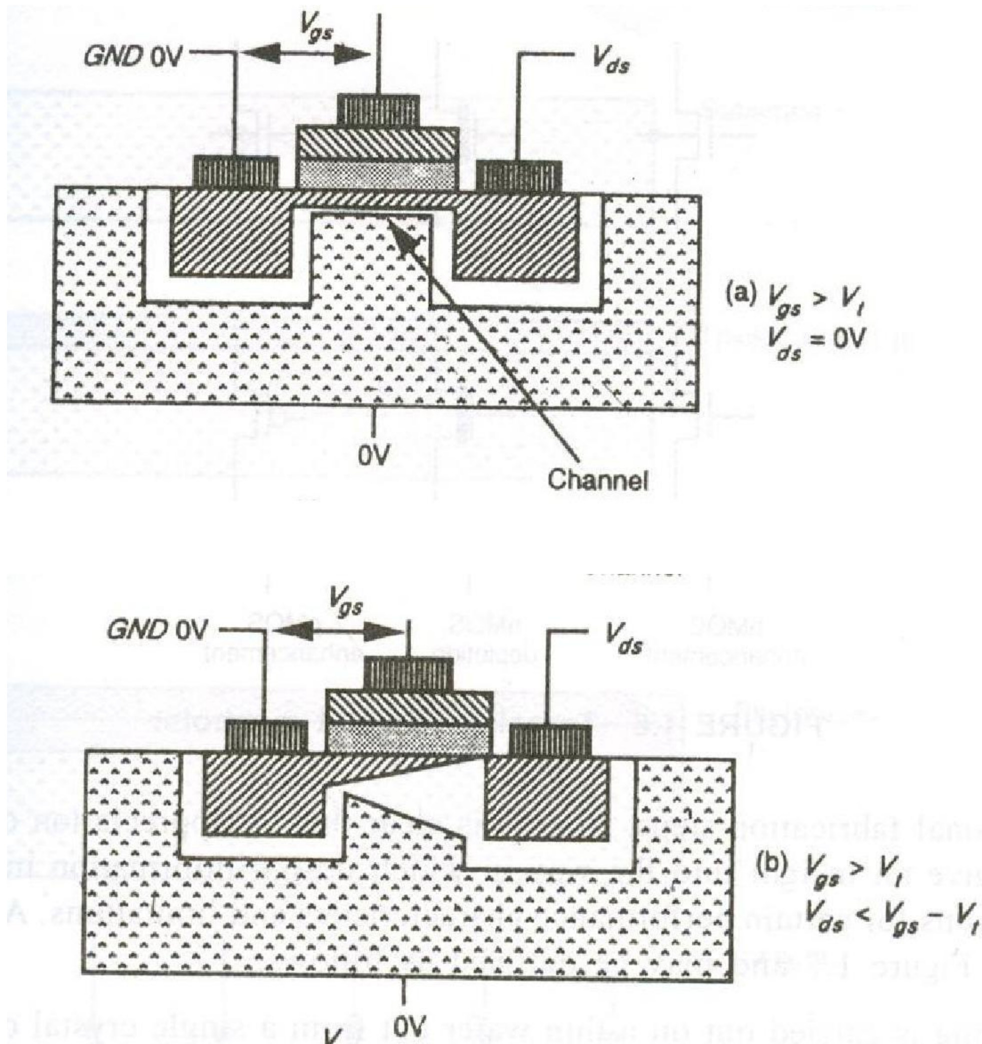


Fig. 7 Nmos Depletion mode transistor

NOTE: Mobility of electrons is 2.5 to 3 times faster than holes. Hence P-MOS devices will have more resistance compared to NMOS.

Enhancement mode Transistor action:-



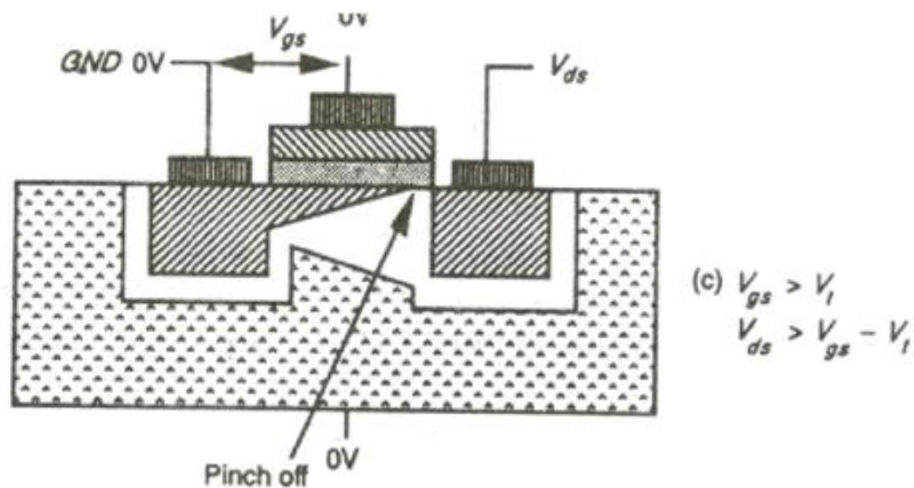


Figure 8(a)(b)(c) Enhancement mode transistor with different Vds values

To establish the channel between the source and the drain a minimum voltage (V_t) must be applied between gate and source. This minimum voltage is called as "Threshold Voltage". The complete working of enhancement mode transistor can be explained with the help of diagram a, b and c.

a) $V_{gs} > V_t$
$V_{ds} = 0$

Since $V_{gs} > V_t$ and $V_{ds} = 0$ the channel is formed but no current flows between drain and source.

b) Vgs > Vt
Vds < Vgs - Vt

This region is called the non-saturation Region or linear region where the drain current increases linearly with Vds. When Vds is increased the drain side becomes more reverse biased(hence more depletion region towards the drain end) and the channel starts to pinch. This is called as the pinch off point.

c) Vgs > Vt
Vds > Vgs - Vt

This region is called Saturation Region where the drain current remains almost constant. As the drain voltage is increased further beyond (Vgs-Vt) the pinch off point starts to move from the drain end to the source end. Even if the Vds is increased more and more, the increased voltage gets dropped in the depletion region leading to a constant current.

The typical threshold voltage for an enhancement mode transistor is given by Vt = 0.2 * Vdd.

Depletion mode Transistor action:-

We can explain the working of depletion mode transistor in the same manner, as that of the enhancement mode transistor only difference is, channel is established due to the implant even when Vgs = 0 and the channel can be cut off by applying a –ve voltage between the gate and source. Threshold voltage of depletion mode transistor is around 0.8*Vdd.

MOS TRANSISTOR THEORY

Introduction

A MOS transistor is a majority-carrier device, in which the current in a conducting channel between the source and the drain is modulated by a voltage applied to the gate.

Symbols

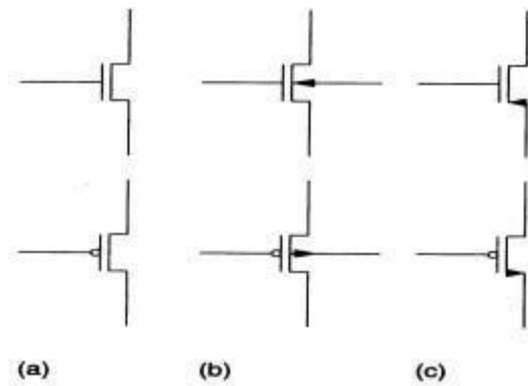


Figure 1 : symbols of various types of transistors.

NMOS (n-type MOS transistor)

vi) Majority carrier = electrons

vii) A positive voltage applied on the gate with respect to the substrate enhances the number of electrons in the channel and hence increases the conductivity of the channel.

viii) If gate voltage is less than a threshold voltage Vt , the channel is cut-off (very low current between source & drain).

PMOS (p-type MOS transistor)

vi) Majority carrier = holes

vii) Applied voltage is negative with respect to substrate.

Relationship between Vgs and Ids, for a fixed Vds:

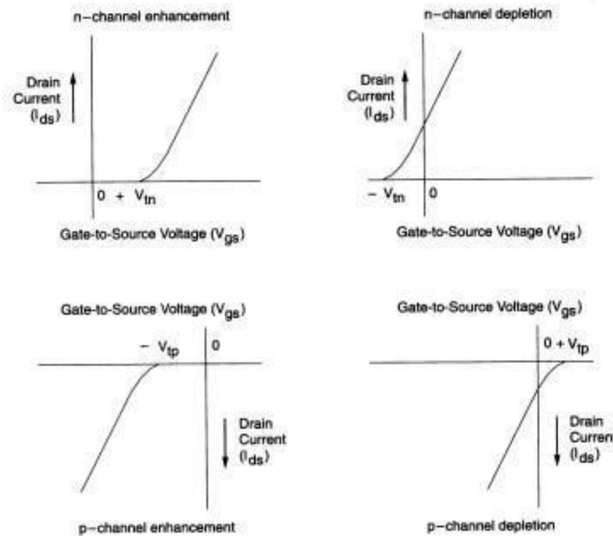


Figure 2: graph of Vgs vs Ids

Devices that are normally cut-off with zero gate bias are classified as **"enhancement-mode "**devices.

Devices that conduct with zero gate bias are called **"depletion-mode"**devices. Enhancement-mode devices are more popular in practical use.

Threshold voltage (*Vt*):

The voltage at which an MOS device begins to conduct ("turn on"). The **threshold voltage** is a function of

c) Gate conductor material
d) Gate insulator material
e) Gate insulator thickness
f) Impurity at the silicon-insulator interface
g) Voltage between the source and the substrate Vsb
h) Temperature

MOS equations (Basic DC equations):

Three MOS operating regions are :Cutoff or subthreshold region, linear region and saturation region.

The following equation describes all these three regions:

$$I_{ds} = \begin{cases} 0; & V_{gs} - V_t \leq 0 \quad \textit{cut-off} \\ \beta\left[(V_{gs} - V_t)V_{ds} - \dfrac{V_{ds}^2}{2}\right]; & 0 < V_{ds} < V_{gs} - V_t \quad \textit{linear} \\ \dfrac{\beta}{2}(V_{gs} - V_t)^2; & 0 < V_{gs} - V_t < V_{ds} \quad \textit{saturation} \end{cases}$$

where β is MOS transistor gain and it is given by $\beta = \mu\ \varepsilon / t_{ox} (W/L)$
again 'μ' is the mobility of the charge carrier

'ε' is the permittivity of the oxide layer. 't_{ox}'is
the thickness of the oxide layer.
'W' is the width of the transistor.(shown in diagram)
'L' is the channel length of the transistor.(shown in diagram)

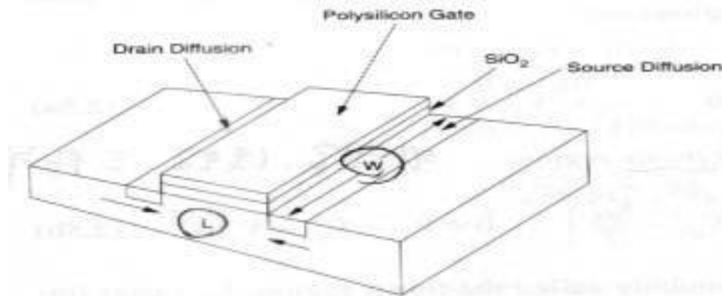


Diagram just to show the length and width of a MOSFET.

The graph of Id and Vds for a given Vgs is given below:

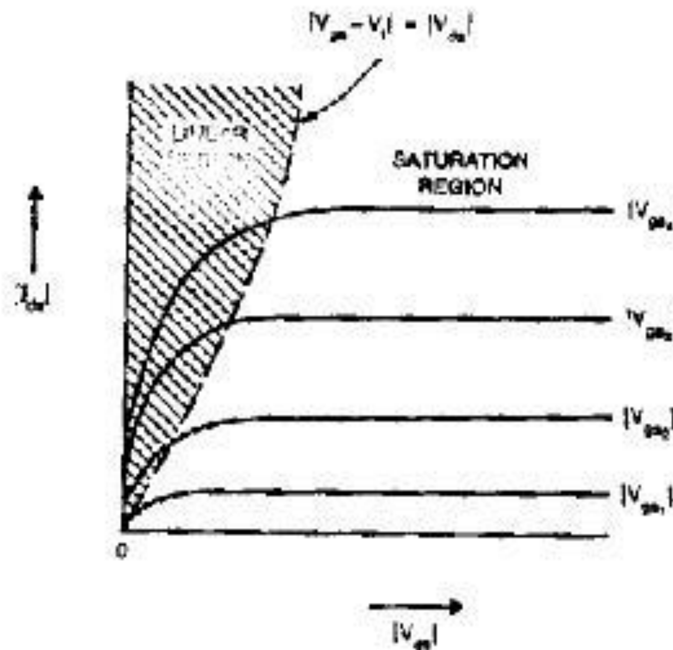


Figure 3: VI Characteristics of MOSFET

Second Order Effects:
Following are the list of second order effects of MOSFET.

Threshold voltage – Body effect
Subthreshold region
Channel length modulation
Mobility variation
Fowler_Nordheim Tunneling
Drain Punchthrough
Impact Ionization – Hot Electrons

Threshold voltage – Body effect

The change in the threshold voltage of a MOSFET, because of the voltage difference between body and source is called body effect. The expression for the threshold voltage is given by the following expression.

$$Vt=V_{t(0)}+\gamma[(V_{sb}+2\Phi_F)^{1/2}-(2\Phi_F)^{1/2}]$$

where
Vt is the threshold voltage,
$V_{t(0)}$ is the threshold voltage without body effect γ is the body coefficient factor
Φ_F is the fermi potential
V_{sb} is the potential difference between source and substarte.

If Vsb is zero, then Vt=Vt(0) that means the value of the threshold voltage will not be changed. Therefore, we short circuit the source and substrate so that, Vsb will be zero.

Subthreshold region:
For Vgs<Vt also we will get some value of Drain current this is called as Subthreshold current and the region is called as Subthreshold region.

Channel length modulation:
The channel length of the MOSFET is changed due to the change in the drain to source voltage. This effect is called as the channel length modulation. The effective channel length & the value of the drain current considering channel length modulation into effect is given by,

$$I_{ds} = \frac{\beta}{2}((V_{gs} - V_t)^2(1 + \lambda V_{ds}))$$

$$L_{eff} = L - \sqrt{2\varepsilon_o \frac{\varepsilon_{Si}}{qN}(V_{ds} - [V_{gs} - V_t])}.$$

Where λ is the channel length modulation factor.

Mobility:

Mobility is the defined as the ease with which the charge carriers drift in the substrate material. Mobility decreases with increase in doping concentration and increase in temperature. Mobility is the ratio of average carrier drift velocity and electric field. Mobility is represented by the symbol μ.

Fowler Nordhiem tunneling:

When the gate oxide is very thin there can be a current between gate and source or drain by electron tunneling through the gate oxide. This current is proportional to the area of the gate of the transistor.

Drain punchthough:

When the drain is a high voltage, the depletion region around the drain may extend to the source, causing the current to flow even it gate voltage is zero. This is known as Punchthrough condition.

Impact Ionization-hot electrons:

When the length of the transistor is reduced, the electric field at the drain increases. The field can be come so high that electrons are imparted with enough energy we can term them as hot. These hot electrons impact the drain, dislodging holes that are then swept toward the negatively charged substrate and appear as a substrate current. This effect is known as Impact Ionization.

MOS Models

MOS model includes the Ideal Equations, Second-order Effects plus the additional Curve-fitting parameters. Many semiconductor vendors expend a lot of effects to model the devices they manufacture.(Standard : Level 3 SPICE) . Main SPICE DC parameters in level 1,2,3 in 1μn-well CMOS process.

CMOS INVETER CHARACTERISTICS

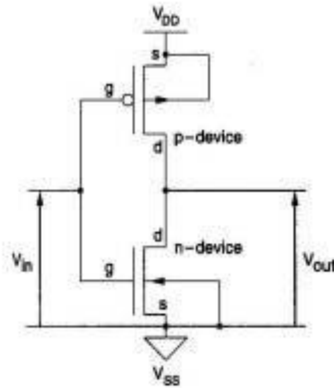


Figure 4: CMOS Inverter

CMOS inverters (Complementary NOSFET Inverters) are some of the most widely used and adaptable MOSFET inverters used in chip design. They operate with very little power loss and at relatively high speed. Furthermore, the CMOS inverter has good logic buffer characteristics, in that, its noise margins in both low and high states are large.

A CMOS inverter contains a PMOS and a NMOS transistor connected at the drain and gate terminals, a supply voltage VDD at the PMOS source terminal, and a ground connected at the NMOS source terminal, were VIN is connected to the gate terminals and VOUT is connected to the drain terminals.(given in diagram). It is important to notice that the CMOS does not contain any resistors, which makes it more power efficient that a regular resistor-MOSFET inverter. As the voltage at the input of the CMOS device varies between 0 and VDD, the state of the NMOS and PMOS varies accordingly. If we model each transistor as a simple switch activated by VIN, the inverter’s operations can be seen very easily:

MOSFET	Condition on MOSFET	State of MOSFET
NMOS	Vgs<Vtn	OFF
NMOS	Vgs>Vtn	ON
PMOS	Vsg<Vtp	OFF
PMOS	Vsg>Vtp	ON

The table given, explains when the each transistor is turning on and off. When VIN is low, the NMOS is "off", while the PMOS stays "on": instantly charging VOUT to

logic high. When Vin is high, the NMOS is "on and the PMOS is "off": taking the voltage at VOUT to logic low.

Inverter DC Characteristics:

Before we study the DC characteristics of the inverter we should examine the ideal characteristics of inverter which is shown below. The characteristic shows that when input is zero output will high and vice versa.

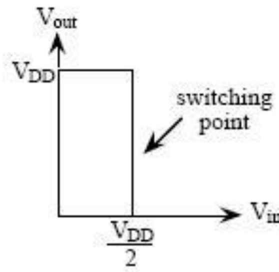


Figure 5: Ideal Characteristics of an Inverter

The actual characteristics is also given here for the reference. Here we have shown the status of both NMOS and PMOS transistor in all the regions of the characteristics.

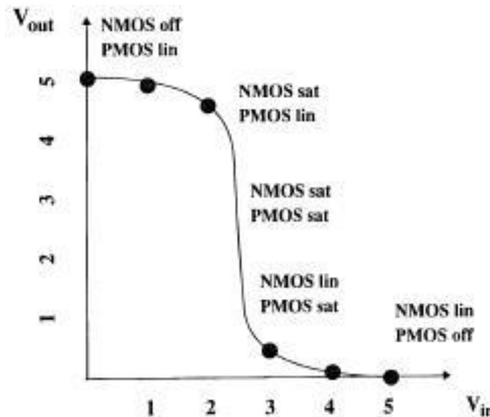


Figure 6: Actual Characteristics of an Inverter

Graphical Derivation of Inverter DC Characteristics:

The actual characteristics is drawn by plotting the values of output voltage for different values of the input voltage. We can also draw the characteristics, starting with the VI characteristics of PMOS and NMOS characteristics.

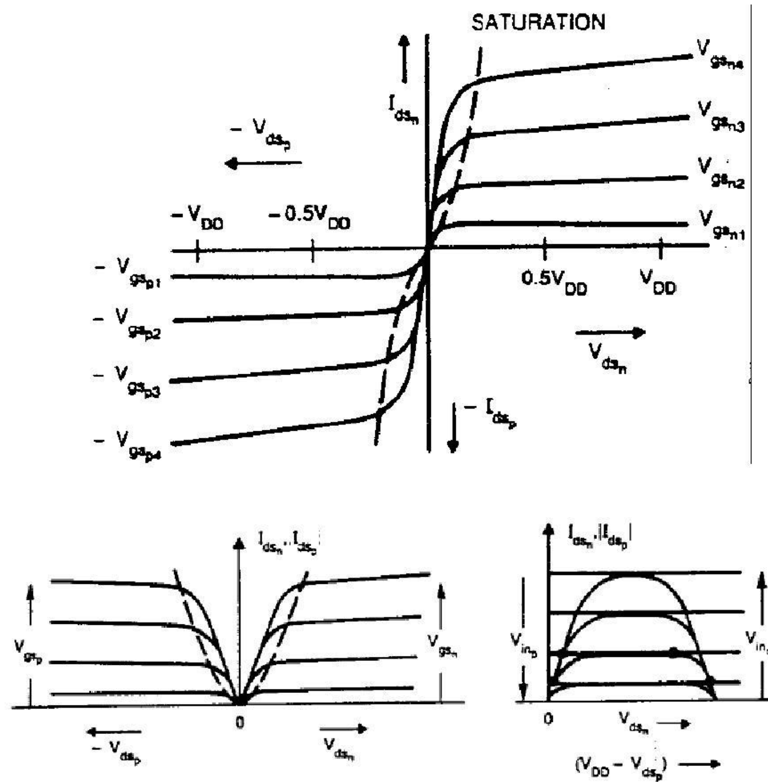
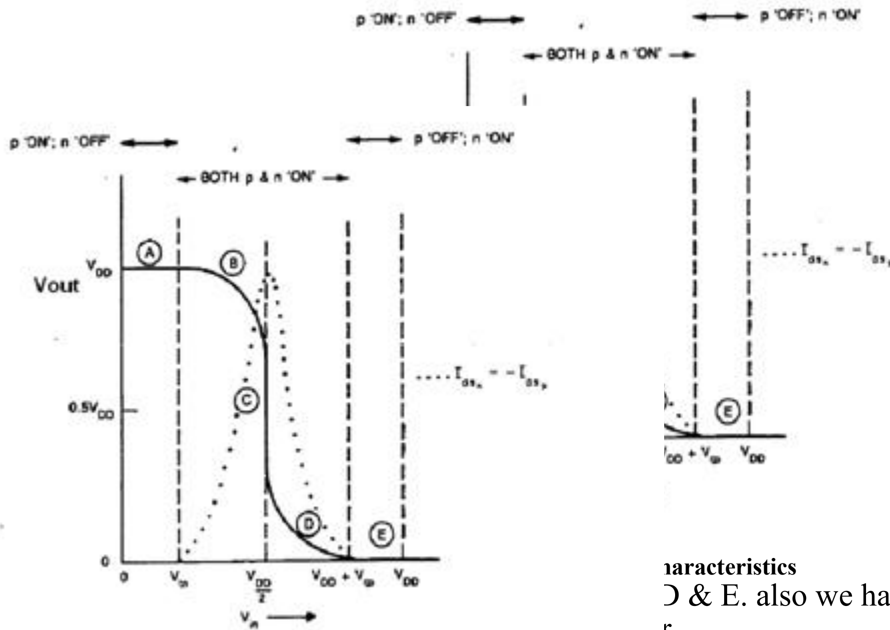


Figure 7a,b,c: Graphical Derivation of DC Characteristics

The characteristics given in figure 7a is the vi characteristics of the NMOS and PMOS characteristics (plot of Id vs. Vds). The figure 7b shows the values of drain current of PMOS transistor is taken to the positive side the current axis. This is done by taking the absolute value of the current. By superimposing both characteristics it leads to figure 7c. the actual characteristics may be now determined by the points of common Vgs intersection as shown in figure 7d.



haracteristics
D & E. also we have shown a dotted
r.

Region A:

The output in this region is High because the P device is OFF and n device is ON. In region A, NMOS is cutoff region and PMOS is on, therefore output is logic high. We can analyze the inverter when it is in region B. the analysis is given below:

Region B:

The equivalent circuit of the inverter when it is region B is given below.

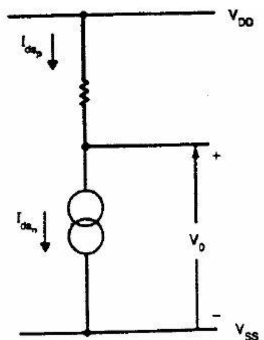


Figure 8: Equivalent circuit in Region B

In this region PMOS will be in linear region and NMOS is in saturation region.

The expression for the NMOS current is $I_{ds_n} = \beta_n \frac{(V_{in} - V_{t_n})^2}{2}$,

The expression for the PMOS current is $I_{ds_p} = -\beta_p\left[(V_{in} - V_{DD} - V_{t_p})(V_O - V_{DD}) - \frac{1}{2}(V_O - V_{DD})^2\right]$

The expression for the voltage Vo can be written as

$$V_O = (V_{in} - V_{t_p}) + \left[(V_{in} - V_{t_p})^2 - 2\left(V_{in} - \frac{V_{DD}}{2} - V_{t_p} \right) V_{DD} - \frac{\beta_n}{\beta_p}(V_{in} - V_{t_n})^2 \right]^{1/2}.$$

Region C:

The equivalent circuit of CMOS inverter when it is in region C is given here. Both n and p transistors are in saturation region, we can equate both the currents and we can obain the expression for the mid point voltage or switching point voltage of a inverter. The corresponding equations are as follows:

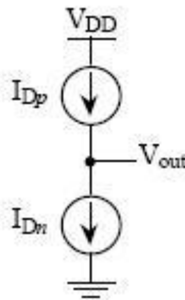


Figure 9: Equivalent circuit in Region C

The corresponding equations are as follows:

$$I_{dsp} = \frac{1}{2}\beta_p (V_{in} - V_{DD} - V_{t_p})^2$$

$$I_{dsn} = \frac{1}{2}\beta_n (V_{in} - V_{t_n})^2$$

By equating both the currents, we can obtain the expression for the switching point voltage as,

$$V_{in} = \frac{V_{DD} + V_{t_p} + V_{t_n}\sqrt{\frac{\beta_n}{\beta_p}}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}}.$$

Region D: the equivalent circuit for region D is given in the figure below.

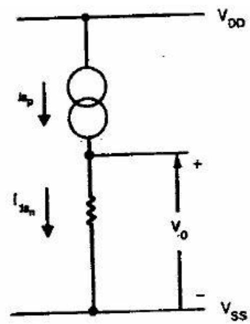


Figure 10: equivalent circuit in region D

We can apply the same analysis what we did for region B and C and we can obtain the expression for output voltage.

Region E:
The output in this region is zero because the P device is OFF and n device is ON.

Influence of βn/βp on the VTC characteristics:

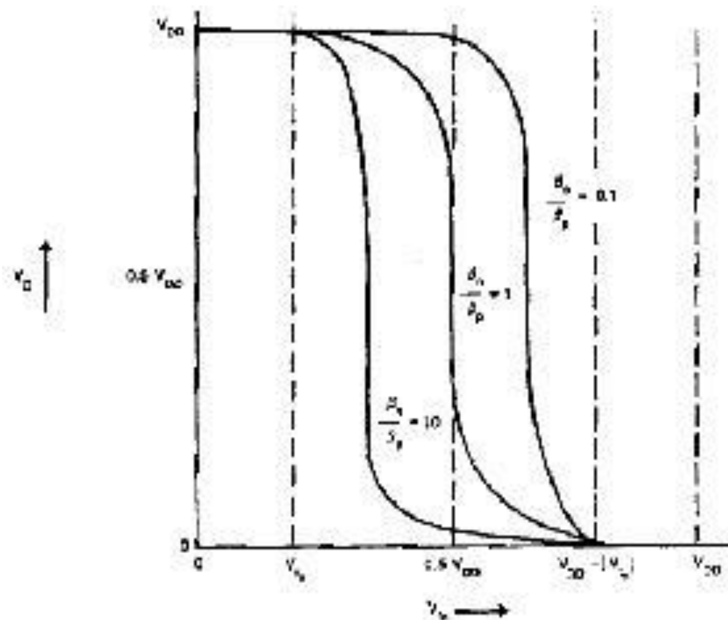


Figure 11: Effect of βn/βp ratio change on the DC characteristics of CMOS inverter

The characteristics shifts left if the ratio of βn/βp is greater than 1(say 10). The curve shifts right if the ratio of βn/βp is lesser than 1(say 0.1). this is decided by the switching point equation of region C. the equation is repeated here the reference again.

$Vm=Vsp=V_{DD}+Vtp+Vtn(\beta n/\beta p)1/2 \,/\, 1+(\beta n/\beta p)1/2$

Noise Margin:

Noise margin is a parameter related to input output characteristics. It determines the allowable noise voltage on the input so that the output is not affected.

We will specify it in terms of two things:

LOW noise margin
HIGH noise margin

LOW noise margin: is defined as the difference in magnitude between the maximum Low output voltage of the driving gate and the maximum input Low voltage recognized by the driven gate.

$NM_L=|V_{ILmax} – V_{OLmax}|$

HIGH noise margin: is defined difference in magnitude between minimum High output voltage of the driving gate and minimum input High voltage recognized by the receiving gate.

$NM_H=|Voh_{min} – V_{IHmin}|$

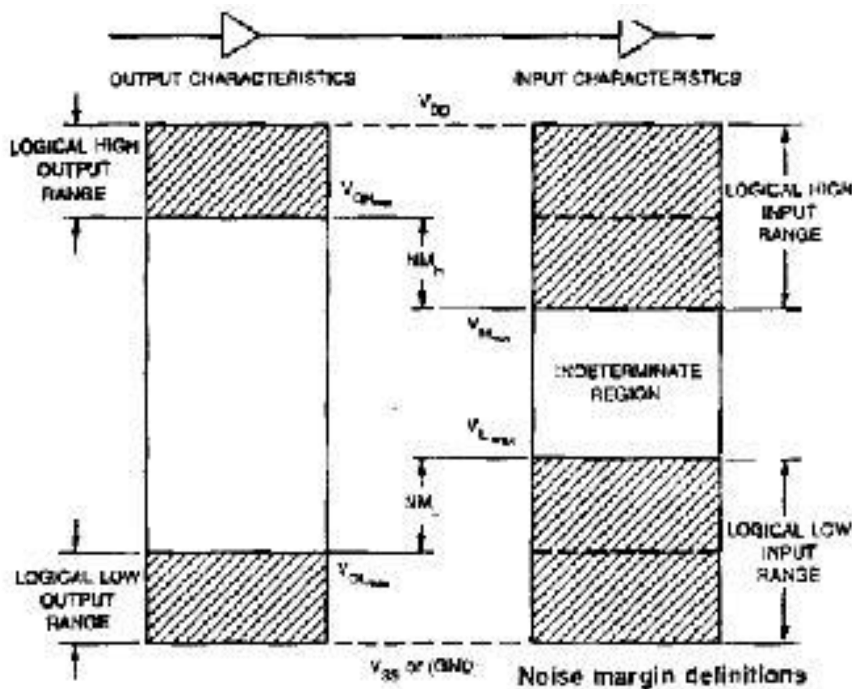


Figure 12: noise margin definitions

Figure shows how exactly we can find the noise margin for the input and output.

We can also find the noise margin of a CMOS inverter. The following figure gives the idea of calculating the noise margin.

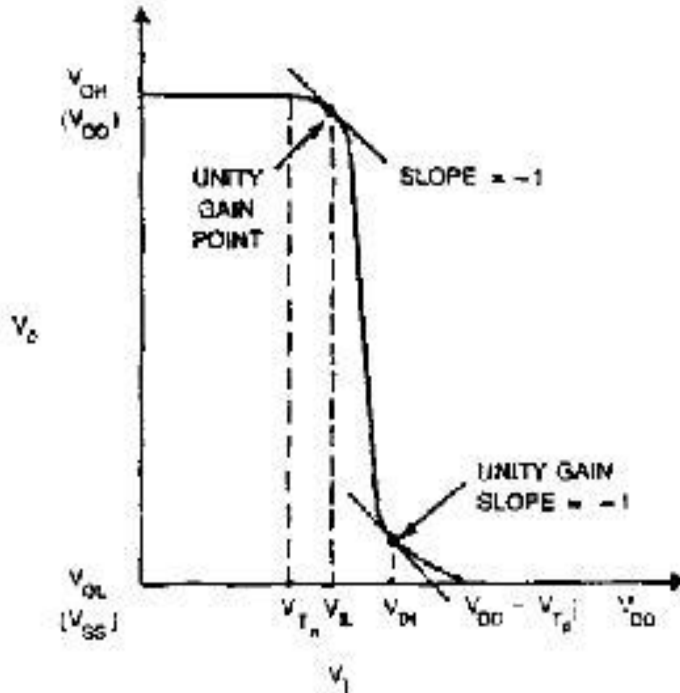


Figure 13: CMOS inverter noise margins

Static Load MOS inverters:

In the figure given below we have shown a resistive load and current source load inverter. Usually resistive load inverters are not preferred because of the power consumption and area issues.

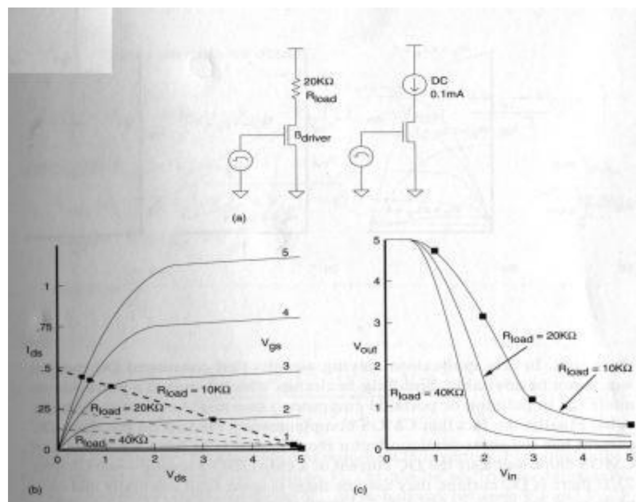


Figure 14: static load inverter

Pseudo-NMOS inverter:

This circuit uses the load device which is p device and is made to turn on always by connecting the gate terminal to the ground.

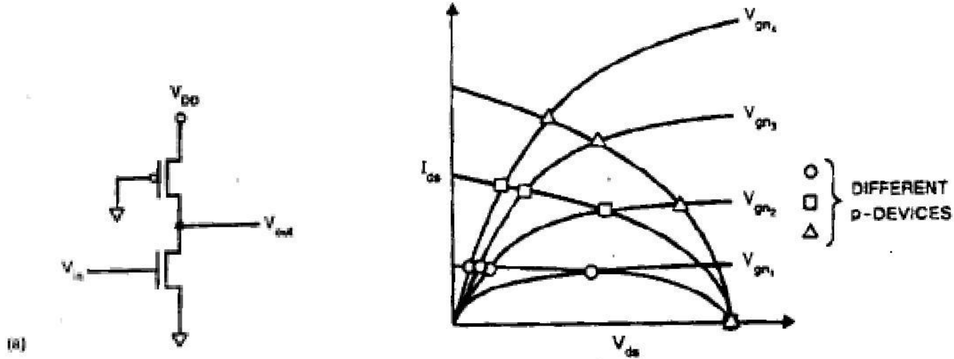


Figure 15: Pseudo-NMOS inverter

Power consumption is High compared to CMOS inverter particularly when NMOS device is ON because the p load device is always ON.

Saturated load inverter:

The load device is an nMOS transistor in the saturated load inverter. This type of inverter was used in nMOS technologies prior to the availability of nMOS depletion loads.

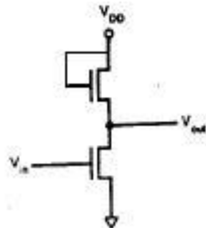


Figure 16: Saturated load inverter

Transmission gates:

It's a parallel combination of pmos and nmos transistor with the gates connected to a complementary input. After looking into various issues of pass transistors we will come back to the TGs again.

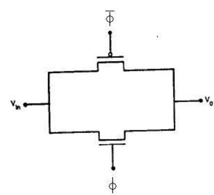


Figure 17: Transmission gate

Pass transistors:
We have n and p pass transistors.

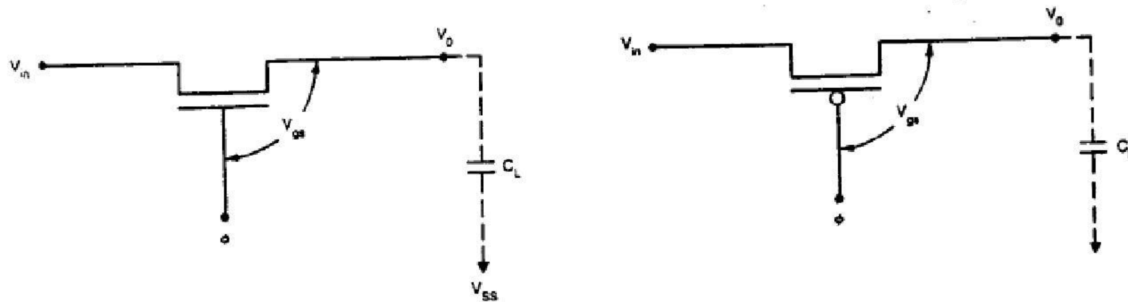


Figure 18: n and p pass transistors

The disadvantage with the pass transistors is that, they will not be able to transfer the logic levels properly. The following table gives that explanation in detail.

Transmission characteristics of *n*-channel and *p*-channel pass transistors

DEVICE	TRANSMISSION OF '1'	TRANSMISSION OF '0'
n	poor	good
p	good	poor

If Vdd (5 volts) is to be transferred using nMOS the output will be (Vdd-Vtn). **POOR 1 or Weak Logic 1**
If Gnd(0 volts) is to be transferred using nMOS the output will be Gnd. **GOOD 0 or Strong Logic 0**
If Vdd (5 volts) is to be transferred using pMOS the output will be Vdd. **GOOD 1 or Strong Logic 1**
If Gnd(0 volts) is to be transferred using pMOS the output will be Vtp. **POOR 0 or Weak Logic 0.**

Transmission gates(TGs):
It's a parallel combination of pmos and nmos transistor with the gates connected to a complementary input. The disadvantages weak 0 and weak 1 can be overcome by using a TG instead of pass transistors.

Working of transmission gate can be explained better with the following equation.

When Φ='0' n and p device off, Vin=0 or 1, Vo='Z'
When Φ='1' n and p device on, Vin=0 or 1, Vo=0 or 1 , where 'Z' is high impedance.

One more important advantage of TGs is that the reduction in the resistance because two transistors will come in parallel and it is shown in the graph. The graph shows the

resistance of n and p pass transistors, and resistance of TG which is lesser than the other two.

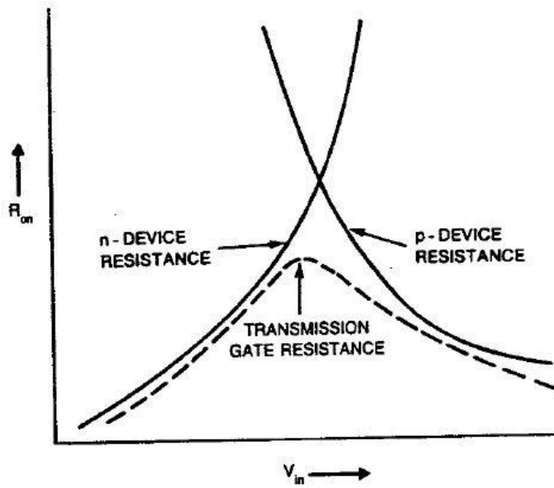


Figure 19: Graph of resistance vs. input for pass transistors and TG

Tristate Inverter:

By cascading a transmission gate with an inverter the tristate inverter circuit can be obtained. The working can be explained with the help of the circuit.

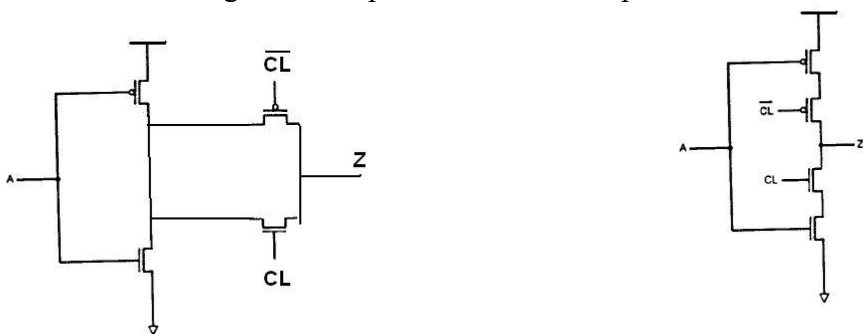
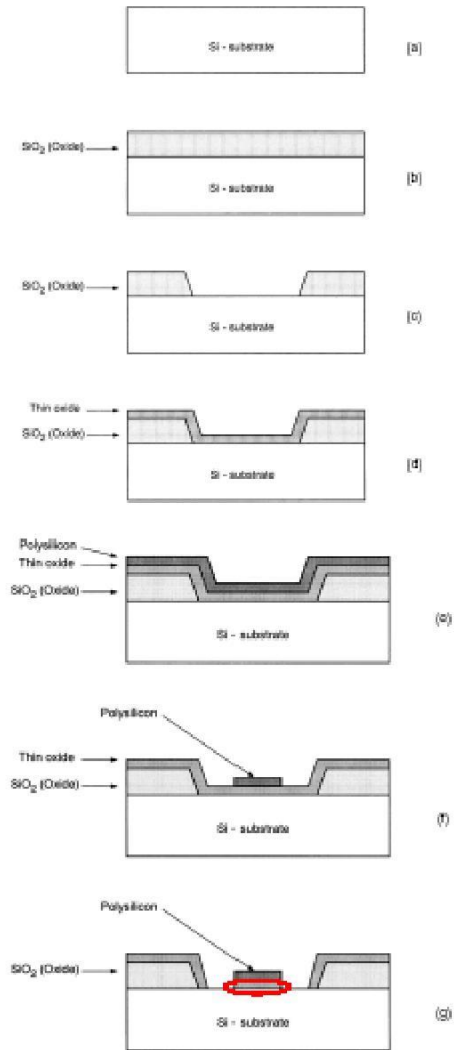


Figure 20: Tristate Inverter

The two circuits are the same only difference is the way they are written. When CL is zero the output of the inverter is in tristate condition. When CL is high the output is Z is the inversion of the input A

NMOS Fabrication:



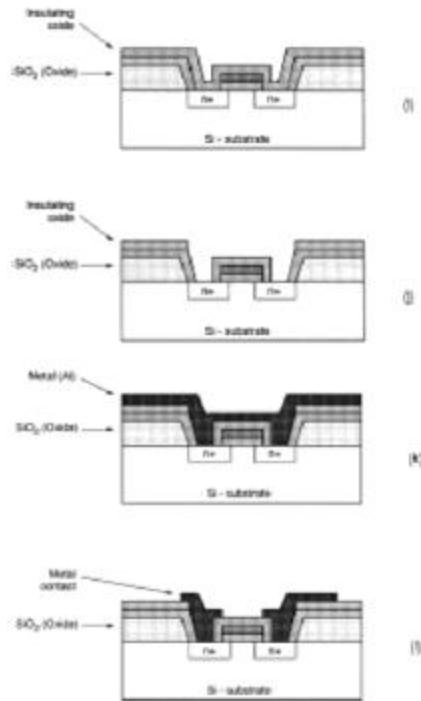


Figure 9 NMOS Fabrication process steps

The process starts with the oxidation of the silicon substrate (Fig. 9(a)), in which a relatively thick silicon dioxide layer, also called field oxide, is created on the surface (Fig. 9(b)). Then, the field oxide is selectively etched to expose the silicon surface on which the MOS transistor will be created (Fig. 9(c)). Following this step, the surface is covered with a thin, high-quality oxide layer, which will eventually form the gate oxide of the MOS transistor (Fig. 9(d)). On top of the thin oxide, a layer of polysilicon (polycrystalline silicon) is deposited (Fig. 9(e)). Polysilicon is used both as gate electrode material for MOS transistors and also as an interconnect medium in silicon integrated circuits. Undoped polysilicon has relatively high resistivity. The resistivity of polysilicon can be reduced, however, by doping it with impurity atoms.

After deposition, the polysilicon layer is patterned and etched to form the interconnects and the MOS transistor gates (Fig. 9(f)). The thin gate oxide not covered by polysilicon is also etched away, which exposes the bare silicon surface on which the source and drain junctions are to be formed (Fig. 9(g)). The entire silicon surface is then doped with a high concentration of impurities, either through diffusion or ion implantation (in this case with donor atoms to produce n-type doping). Figure 9(h) shows that the doping penetrates the exposed areas on the silicon surface, ultimately creating two n-type regions (source and drain junctions) in the p-type substrate. The impurity doping also penetrates the polysilicon on the surface, reducing its resistivity. Note that the polysilicon gate, which is patterned before doping actually defines the precise location of the channel region and, hence, the location of the source and the drain regions. Since this procedure allows very precise positioning of the two regions relative to the gate, it is also called the self-aligned

process. Once the source and drain regions are completed, the entire surface is again covered with an insulating layer of silicon dioxide (Fig. 9 (i)). The insulating oxide layer is then patterned in order to provide contact windows for the drain and source junctions (Fig. 9 (j)). The surface is covered with evaporated aluminum which will form the interconnects (Fig. 9 (k)). Finally, the metal layer is patterned and etched, completing the interconnection of the MOS transistors on the surface (Fig. 9 (l)). Usually, a second (and third) layer of metallic interconnect can also be added on top of this structure by creating another insulating oxide layer, cutting contact (via) holes, depositing, and patterning the metal.

CMOS fabrication: When we need to fabricate both nMOS and pMOS transistors on the same substrate we need to follow different processes. The three different processes are,P-well process ,N-well process and Twin tub process.

P-WELL PROCESS:

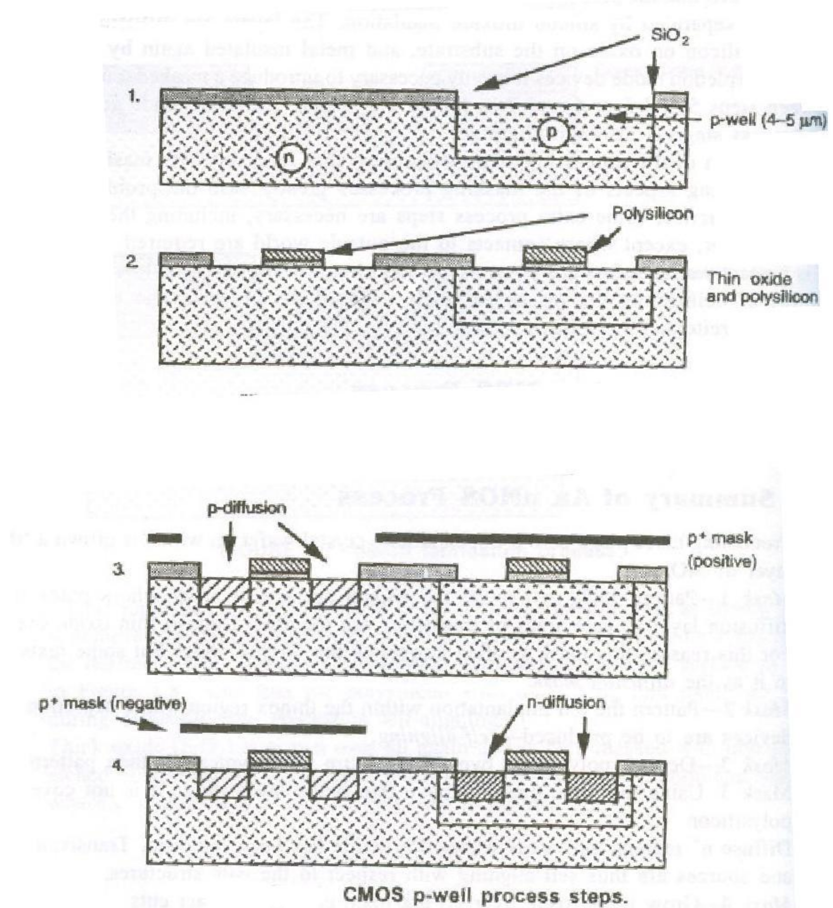


Figure 10 CMOS Fabrication (P-WELL) process steps

The p-well process starts with a n type substrate. The n type substrate can be used to implement the pMOS transistor, but to implement the nMOS transistor we need to provide a p-well, hence we have provided he place for both n and pMOS transistor on the same n-type substrate.

Mask sequence.
Mask 1:

Mask 1 defines the areas in which the deep p-well diffusion takes place.

Mask 2:

It defines the thin oxide region (where the thick oxide is to be removed or stripped and thin oxide grown)

Mask 3:

It's used to pattern the polysilicon layer which is deposited after thin oxide. Mask 4:

A p+ mask (anded with mask 2) to define areas where p-diffusion is to take place.

Mask 5:

We are using the –ve form of mask 4 (p+ mask) It defines where n-diffusion is to take place.

Mask 6:

Contact cuts are defined using this mask.

Mask 7:

The metal layer pattern is defined by this mask. Mask 8:

An overall passivation (overglass) is now applied and it also defines openings for accessing pads.

The cross section below shows the CMOS pwell inverter.

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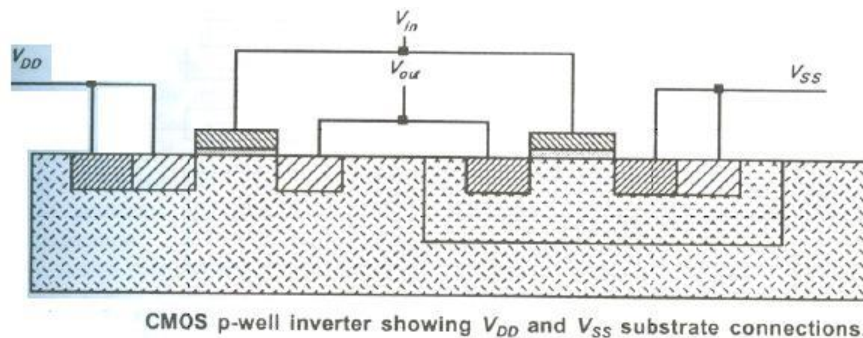


CMOS p-well inverter showing V_{DD} and V_{SS} substrate connections.

Figure 11 CMOS inverter (P-WELL)

N-WELL PROCESS:

In the following figures, some of the important process steps involved in the fabrication of a CMOS inverter will be shown by a top view of the lithographic masks and a cross-sectional view of the relevant areas.

The n-well CMOS process starts with a moderately doped (with impurity concentration typically less than 10^{15} cm-3) p-type silicon substrate. Then, an initial oxide layer is grown on the entire surface. The first lithographic mask defines the n-well region. Donor atoms, usually phosphorus, are implanted through this window in the oxide. Once the n-well is created, the active areas of the nMOS and pMOS transistors can be defined. Figures 12.1 through 12.6 illustrate the significant milestones that occur during the fabrication process of a CMOS inverter.

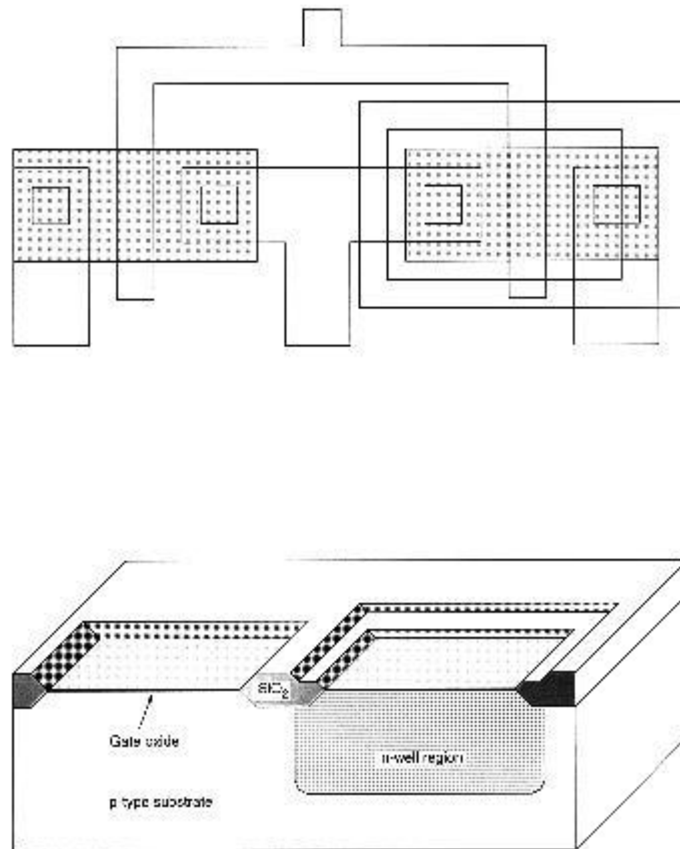


Figure-12.1: Following the creation of the n-well region, a thick field oxide is grown in the areas surrounding the transistor active regions, and a thin gate oxide is grown on top of the active regions. The thickness and the quality of the gate oxide are two of the most critical fabrication parameters, since they strongly affect the operational characteristics of the MOS transistor, as well as its long-term reliability.

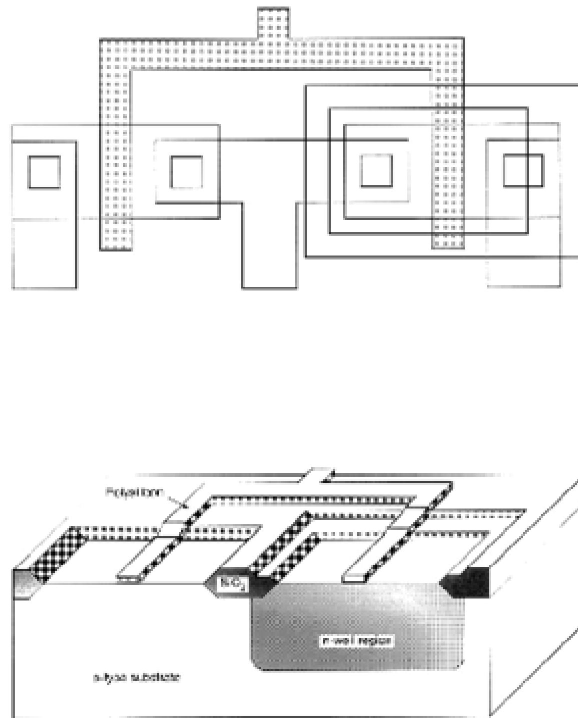
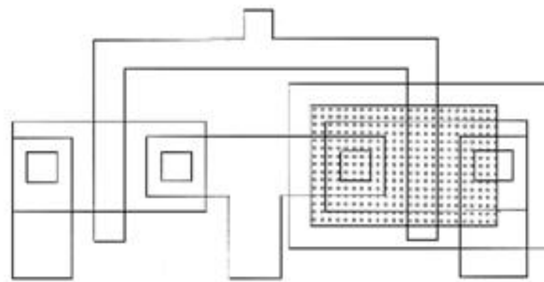


Figure-12.2: The polysilicon layer is deposited using chemical vapor deposition (CVD) and patterned by dry (plasma) etching. The created polysilicon lines will function as the gate electrodes of the nMOS and the pMOS transistors and their interconnects. Also, the polysilicon gates act as self-aligned masks for the source and drain implantations that follow this step.



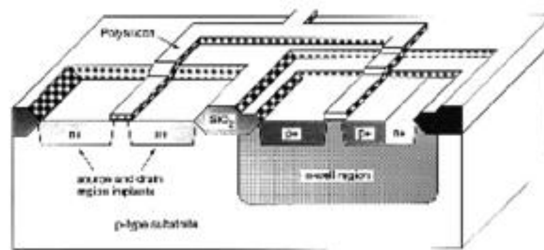
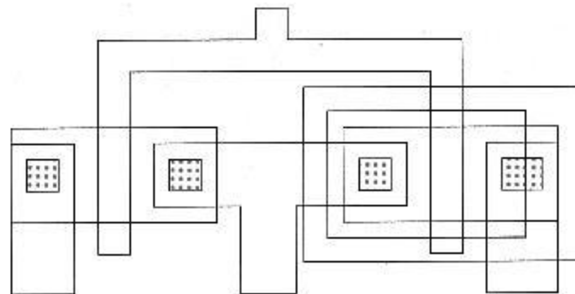


Figure-12.3: Using a set of two masks, the n+ and p+ regions are implanted into the substrate and into the n- well, respectively. Also, the ohmic contacts to the substrate and to the n-well are implanted in this process step.



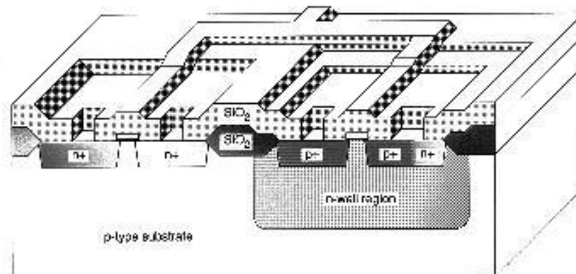
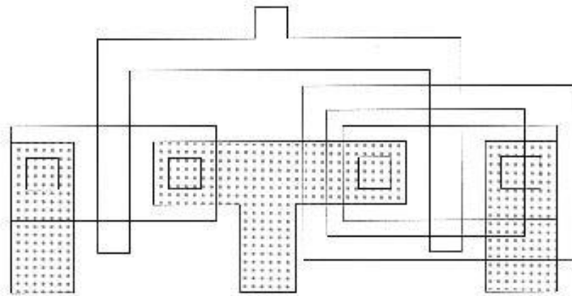


Figure-12.4: An insulating silicon dioxide layer is deposited over the entire wafer using CVD. Then, the contacts are defined and etched away to expose the silicon or polysilicon contact windows. These contact windows are necessary to complete the circuit interconnections using the metal layer, which is patterned in the next step.



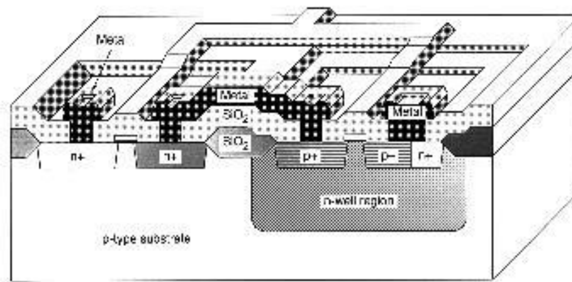


Figure-12.5: Metal (aluminum) is deposited over the entire chip surface using metal evaporation, and the metal lines are patterned through etching. Since the wafer surface is non-planar, the quality and the integrity of the metal lines created in this step are very critical and are ultimately essential for circuit reliability.

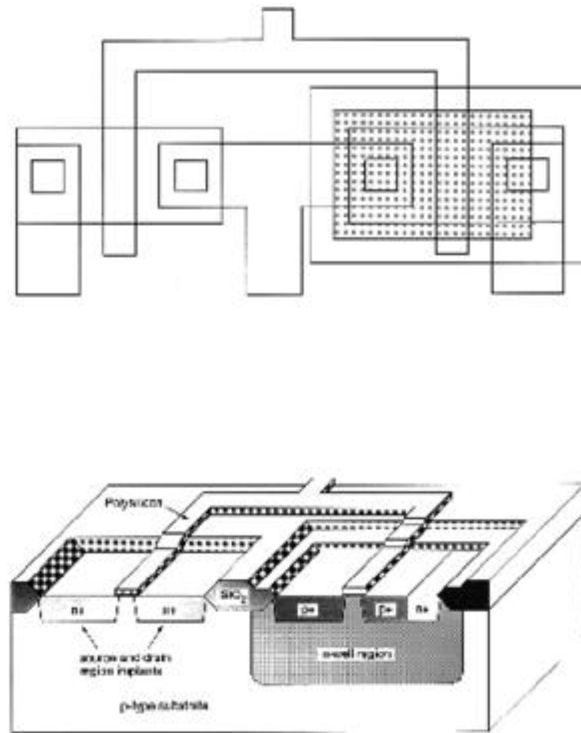


Figure-12.6: The composite layout and the resulting cross-sectional view of the chip, showing one nMOS and one pMOS transistor (built-in n-well), the polysilicon and metal interconnections. The final step is to deposit the passivation layer (for protection) over the chip, except for wire-bonding pad areas.

Twin-tub process:

Here we will be using both p-well and n-well approach. The starting point is a n-type material and then we create both n-well and p-well region. To create the both well we first go for the epitaxial process and then we will create both wells on the same substrate.

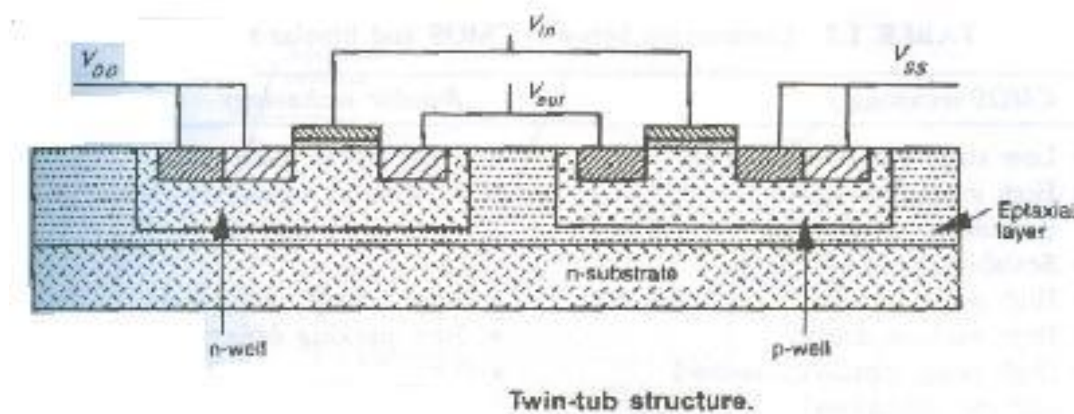


Figure 13 CMOS twin-tub inverter

NOTE: Twin tub process is one of the solutions for latch-up problem.

Bi-CMOS technology: - (Bipolar CMOS)

The driving capability of MOS transistors is less because of limited current sourcing and sinking capabilities of the transistors. To drive large capacitive loads we can think of Bi-Cmos technology.

This technology combines Bipolar and CMOS transistors in a single integrated circuit, by retaining benefits of bipolar and CMOS, BiCMOS is able to achieve VLSI circuits with speed-power-density performance previously unattainable with either technology individually.

Characteristics of CMOS Technology

- Lower static power dissipation
- Higher noise margins
- Higher packing density – lower manufacturing cost per device
- High yield with large integrated complex functions
- High input impedance (low drive current)
- Scaleable threshold voltage
- High delay sensitivity to load (fan-out limitations)
- Low output drive current (issue when driving large capacitive loads)
- Low transconductance, where transconductance, gm α Vin
- Bi-directional capability (drain & source are interchangeable)
- A near ideal switching device

Characteristics of Bipolar Technology

- Higher switching speed
- Higher current drive per unit area, higher gain
- Generally better noise performance and better high frequency characteristics
- Better analogue capability
- Improved I/O speed (particularly significant with the growing importance of package limitations in high speed systems).
- high power dissipation
- lower input impedance (high drive current)
- low voltage swing logic
- low packing density
- low delay sensitivity to load
- high gm (gm α Vin)
- high unity gain band width (ft) at low currents
- essentially unidirectional

From the two previous paragraphs we can get a comparison between bipolar and CMOS technology.

The diagram given below shows the cross section of the BiCMOS process which uses an npn transistor.

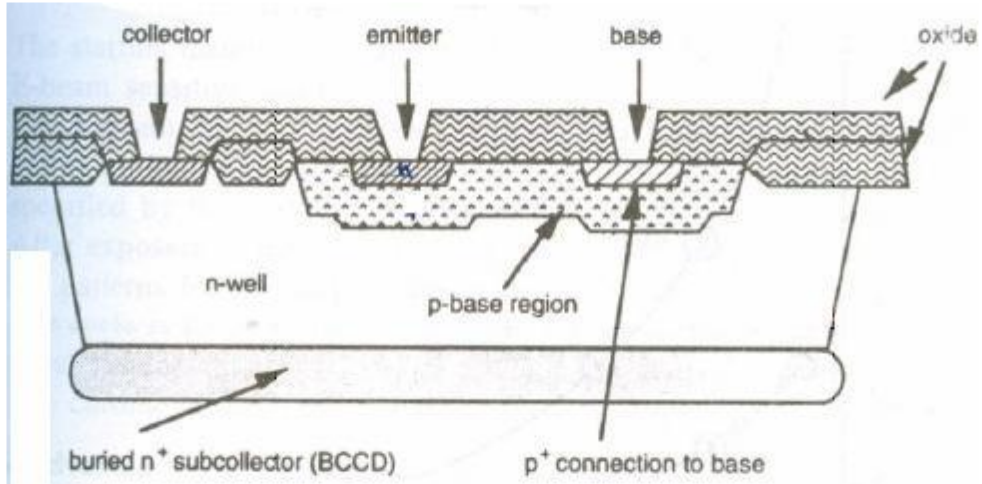


Figure 14 Cross section of BiCMOS process

The figure below shows the layout view of the BiCMOS process.

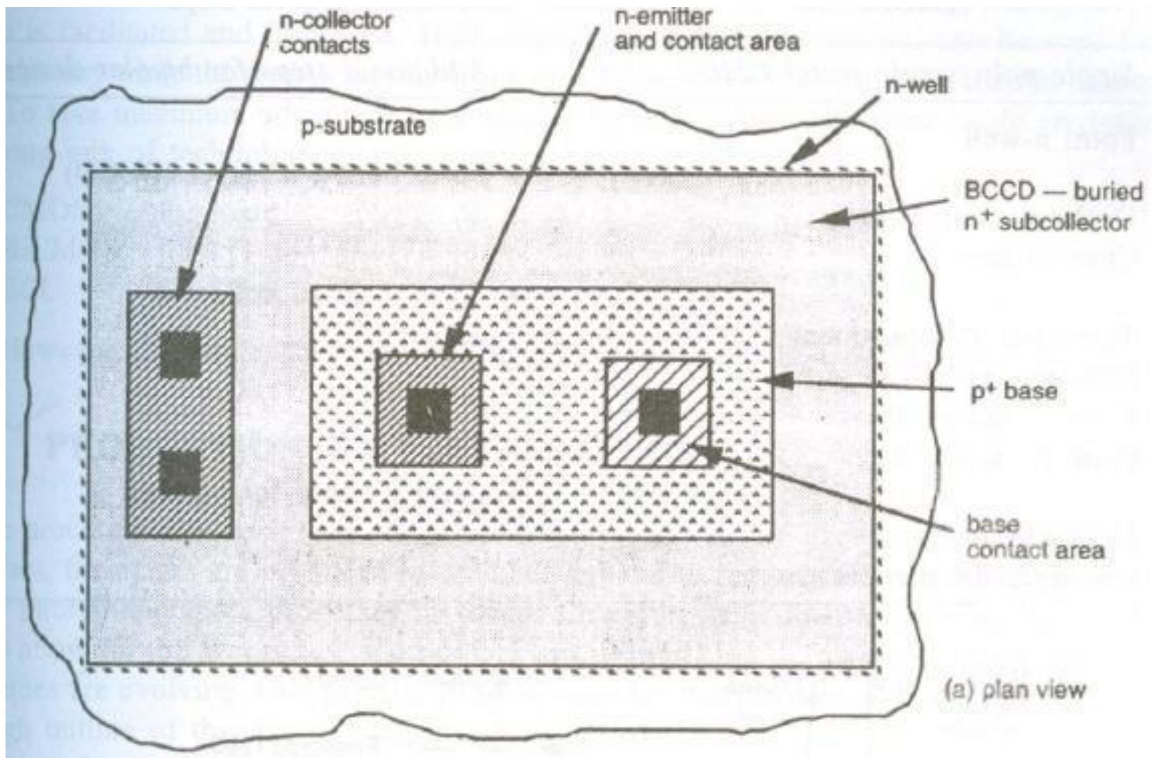


Fig.15. Layout view of BiCMOS process

The graph below shows the relative cost vs. gate delay.

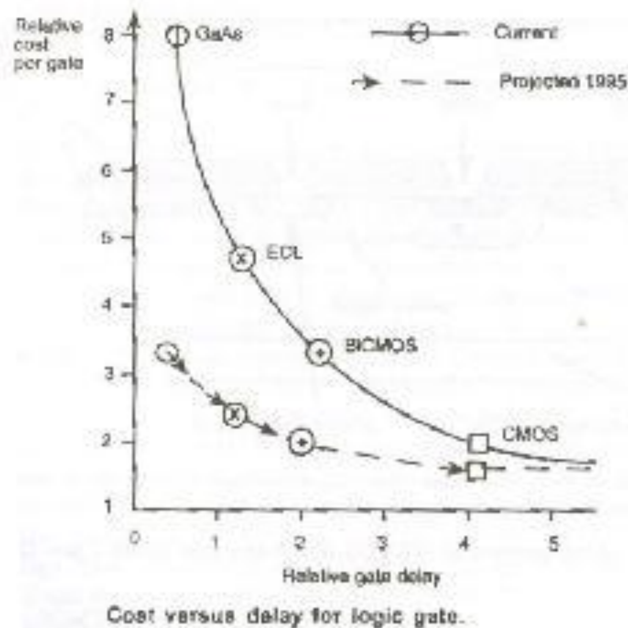


Fig.16. cost versus delay graph

Production of e-beam masks:

In this topic we will understand how we are preparing the masks using e-beam technology. The following are the steps in production of e-beam masks.

- Starting materials is chromium coated glass plates which are coated with e-beam sensitive resist.
- E-beam machine is loaded with the mask description data.
- Plates are loaded into e-beam machine, where they are exposed with the patterns specified by mask description data.
- After exposure to e-beam, plates are introduced into developer to bring out patterns.
- The cycle is followed by a bake cycle which removes resist residue.
- The chrome is then etched and plate is stripped of the remaining e-beam resist.

We use two types of scanning, Raster scanning and vector scanning to map the pattern on to the mask.

In raster type, e-beam scans all possible locations and a bit map is used to turn the e-beam on and off, depending on whether the particular location being scanned is to be exposed or not.

In vector type, beam is directed only to those location which are to be exposed.

Advantages e-beam masks:

Tighter layer to layer registration;
Small feature sizes