



S J P N Trust's

Hirasugar Institute of Technology, Nidasoshi.*Inculcating Values, Promoting Prosperity*

Approved by AICTE, Recognized by Govt. of Karnataka and Affiliated to VTU Belagavi.

ECE Dept.

Exam.

Internal Assessment

Even Sem(2017-18)

THIRD INTERNAL ASSESSMENT

Sem :VI	Sub: VLSI DESIGN	Sub. Code: 15EC63
Date:19/05/2018	Time: 11:00AM-12.00N	Max. Marks: 25

Note: Answer two full questions, draw sketches wherever necessary.

Q. No	Discription of Question	Marks	CO	RBT LEVEL
1.	a. Define scaling and find the scaling factors for: i) Saturation current ii) Current density iii) Gate capacitance iv) Powerdissipation/unit area v) Maximum operating frequency	6	CO311.3	L2
	b. With a neat diagram, explain 4x4 barrel shifter.	6	CO311.3	L3
OR				
2.	a. Explain Pseudo nMOS logic for NAND gate and Inverter	6	CO311.6	L2
	b. Explain Parity generator with basic block diagram and stick diagram.	6	CO311.6	L3
3.	a. Explain 3 transistor dynamic RAM cell with stick diagram	6	CO311.3	L2
	b. Explain switch logic implementation of a 4x4 four way multiplexer	7	CO311.3	L3
OR				
4.	a. Explain in detail the Generic Structure of an FPGA fabric.	6	CO311.4	L2
	b. Explain any two fault models in combinational circuits.	7	CO311.5	L2


Course Coordinator
Module Coordinator
HOD

SCHEME OF EVALUATION

Sem : G.		Subject : VLSI Design	Sub Code : 15EC63	Date : 19-05-18		
Q. No.	Bit	Description	Marks	CO's	RBT LEVEL	
1	a.	<p>The process of reducing vertical and horizontal size or dimensions of the MOSFET is referred to as scaling.</p> <p>Scaling factors for:</p> <p>i) Saturation current : $I_{DSS} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{gs} - V_t)^2$</p> $= \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{gs} - V_t)^2$ $= \beta \frac{1}{\beta^2} = \frac{1}{\beta}$ <p>ii) Current density $J = \frac{I_{DSS}}{A} = \frac{1}{\beta} \frac{\alpha^2}{1/\alpha^2 \beta^2}$</p> <p>iii) Gate Capacitance $C_g = C_{ox} L W = \frac{\beta}{\alpha^2}$</p> <p>iv) power dissipation/unit area = $P_a = \frac{P_g}{A_g}$</p> $P_a = \frac{1/\beta^2}{1/\alpha^2} = \frac{\alpha^2}{\beta^2}$ <p>v) Max. operating frequency f_o</p> $f_o = \frac{W}{L} \frac{\mu_n C_{ox} V_{DD}}{C_g} = \frac{\alpha^2}{\beta}$	6	CO311, 3	L2	
	b.	<p>4x4 barrel shifter.</p> <p>The barrel shifter; interbus switches have their gate s/ps connected in a stair-case fashion in groups of four and there four shift control s/ps which must be mutually exclusive in the active state. ②</p> <p>CMOS, transmission gate may be used in place of pass transistor. + diagram ④.</p>	6	CO313	L3	



SCHEME OF EVALUATION

Sem : 6		Subject : VLSI Design	Sub Code : 15EC63	Date : 19-05-18		
Q. No.	Bit	Description	Marks	CO's	RBT LEVEL	
2.	a.	<p>Pseudo nMOS logic factor in explanation</p> <p>Pseudo nMOS NAND gate</p> <p>Pseudo inverter</p>	6	CO3, CO6	L2	
		$V_{inv} = V_{tn} + \frac{(2.5 \mu p / \mu n)^{1/2} [(5V - V_{tn}) V_{dsp} - V_{dsp}^2]}{(Z_{P,u} / Z_{P,d})^{1/2}}$ <p>for $V_{inv} = 0.5V_{DD}$, $V_{tn} = V_{tp} = 0.2V_{DD}$ $V_{DD} = 5V$ $\mu_n = 2.5 \mu_p$ $\frac{Z_{P,u}}{Z_{P,d}} = \frac{3}{1}$</p> <ol style="list-style-type: none"> power dissipation is reduced by 60% than in 4:1 inverter (nMOS) The higher pull-up resistance leads to more delay. (larger by 8.5:5 than nMOS 4:1) 				
	b.	<p>Parity Generator</p>	6	CO3, CO6	L3	
		$P = 1 - \text{even no. of } 1's$ $P = 0 - \text{odd no. of } 1's$ <p>As no. of bits is undefined, the general solution on a cascaded bit-wise basis so that we can have any value.</p>				



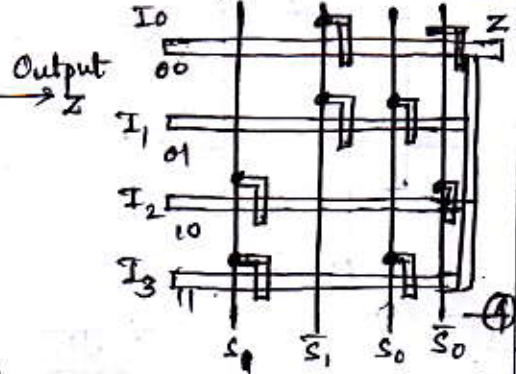
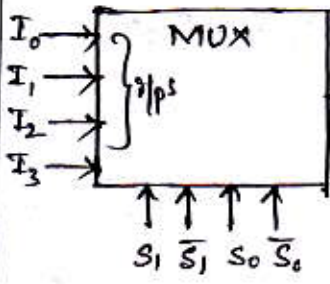
SCHEME OF EVALUATION

Sem : 6		Subject : VLSI Design	Sub Code : 15EC63	Date : 19/05/18		
Q. No.	Bit	Description	Marks	CO's	RBT LEVEL	
2.	b.	<p> $P_i = \bar{P}_{i-1} A_i + P_{i-1} \bar{A}_i$ </p>	6	CO 311.6	L3	
3.	a.	<p>Three-transistor SRAM cell</p>	3	CO 311.6	L2	
		<p>explanation req. RD & WR. & general.</p>	3			
	b.	<p>Implementation of 4x4 way multiplexer</p> <p>Multiplexer eqn is,</p> $Z = I_0 \bar{S}_1 \bar{S}_0 + I_1 \bar{S}_1 S_0 + I_2 S_1 \bar{S}_0 + I_3 S_1 S_0$	6	CO 311.3	L3	



SCHEME OF EVALUATION

Sem : 6		Subject : VLSI Design	Sub Code : 15EC69	Date : 19-05-18	
Q. No.	Bit	Description		Marks	CO's
					RBT LEVEL

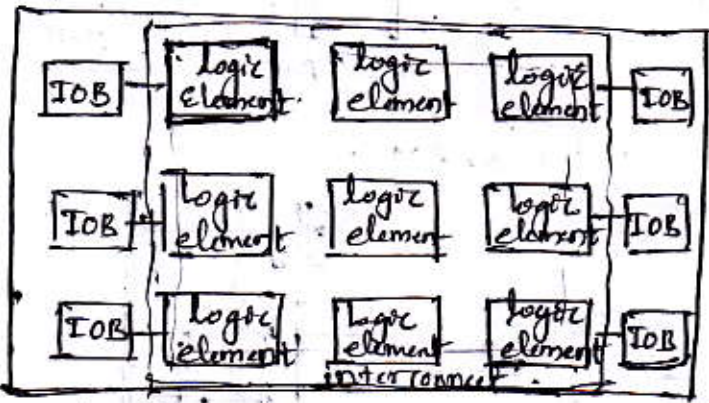


factor → ③

7 CO 3113 L3

4

- a. Generic structure of FPEFA fabric.
 FPEFAs require three major types of elements
- combinatorial logic
 - interconnect
 - I/O pins



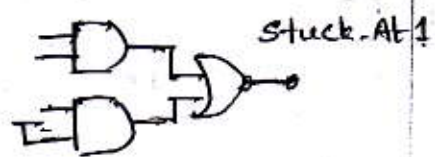
explanation + diagrams → 3+3

6 CO 3112 L2

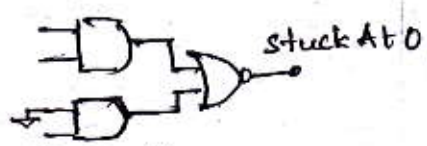
- b. Any two fault models.

stuck-at Faults

stuck-at-1



stuck-at-0



7 CO 3115 L2

Short circuit & Open circuit faults
 any of the short ckt and open ckt examples.