	S J P N Trust's HirasugarInstitute of Technology, Nidasoshi. *Inculcating Values, Promoting Prosperity* Approved by AICTE, Recognized by Govt. of Karnataka and Affiliated to VTU Belagavi.	ECE Dept. Exam. Internal Assessment Even Sem(2017-18)

SECOND INTERNAL ASSESSMENT		
Sem :VI	Sub: VLSI DESIGN	Sub. Code: 15EC63
Date:12/04/2018	Time: 11:00AM-12.00PM	Max. Marks: 25

Note: Answer two full questions, draw sketches wherever necessary.

Q. No		Discription of Question	Marks	CO	RBT LEVEL
1.	a.	With neat diagram, explain λ based rules for (NMOS and CMOS) and transistor design rules (nMOS, pMOS and CMOS)	12	CO311. 2	L2
		OR			
2.	a.	What is a stick diagram? Draw schematic and stick diagram for nMOS and CMOS style (step by step) for the Boolean expression $Y = \overline{AB + CD}$	12	CO311. 2	L3
3.	a.	Draw the circuit diagram, monochrome stick diagram and mask layout of p-well CMOS inverter.	8	CO311. 2	L2
	b.	What is a contact? Explain the design rules related to contacts	5	CO311. 2	L2
		OR			
4.	a.	Explain and distinguish buried and butting contacts with suitable diagrams	8	CO311. 2	L2
	b.	Explain the following i) sheet resistance ii) standard unit capacitance	5	CO311. 2	L2

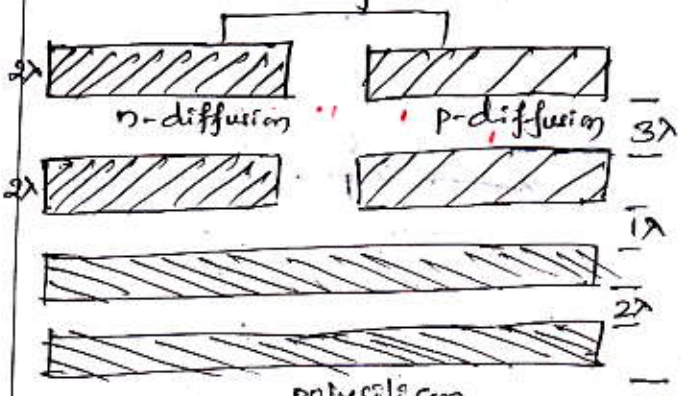
Course Coordinator **Module Coordinator** **HOD**

SCHEME OF EVALUATION IA- II

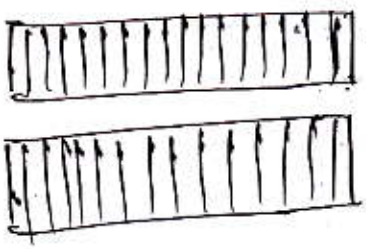
Sem : VI | Subject : VLSI Design | Sub Code : 15EC63 | Date : 12-02-18

Q. No.	Bit	Description	Marks	CO's	RBT LEVEL
1.	a.	Lambda-based Design Rules. Design rules and Layout methodology based on the concept of λ provide a process and feature size-independent way of setting mask dimensions scale. – 2M. All paths in all layers are dimensioned in λ units and subsequently, λ value is compatible with feature size.	12	CO311.2	L2

Minimum feature size on the chip = 2λ



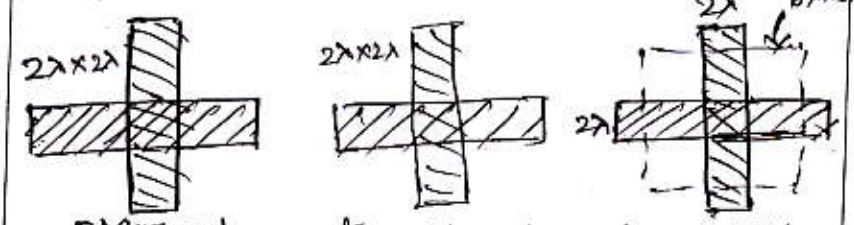
– 3M.



for metal 2, 4λ

– 2M.

5M



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Module Coordinator

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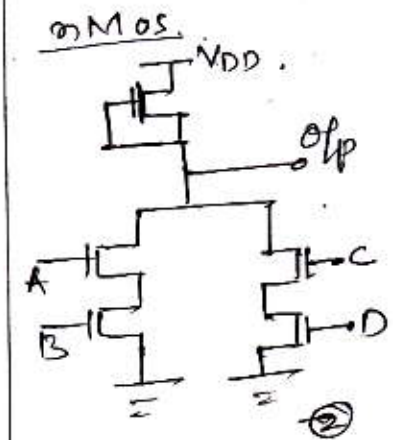
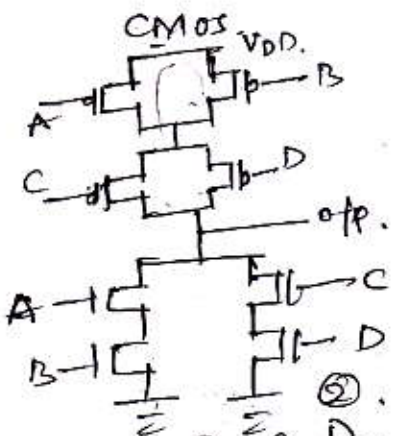
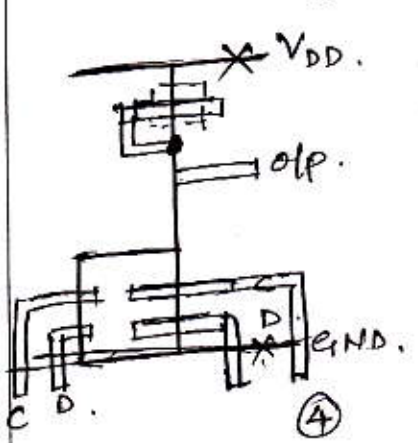
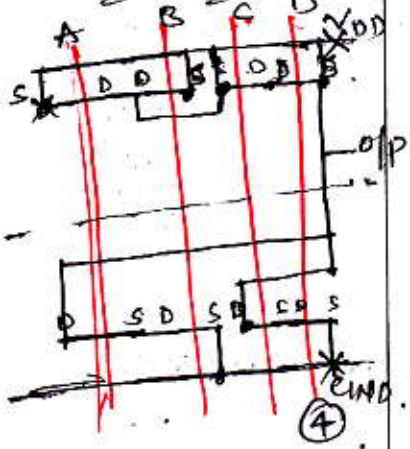
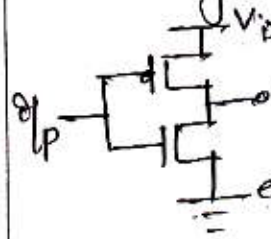
SCHEME OF EVALUATION IA-II

Sem : VI | Subject : VLSI Design | Sub Code : 15ECE63 | Date : 13-04-18

Q. No.	Bit	Description	Marks	CO's	RBT LEVEL
2.	a.	λ based design rules The schematic nMOS.  CMOS   	12	CO3 L2	L3
3	a.	Circuit diagram and and monochrome stick diagram of p-well CMOS inverter.  —2M.			

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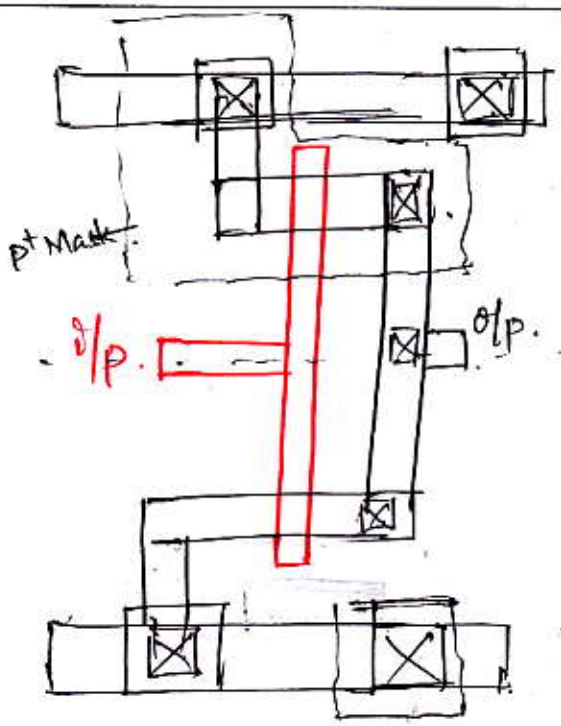
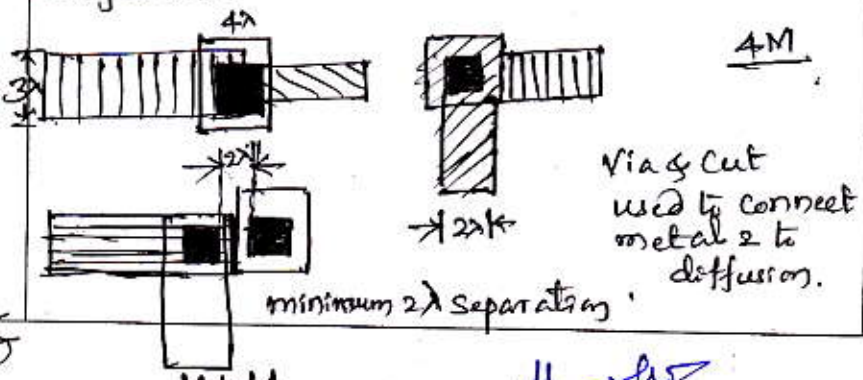
SCHEME OF EVALUATION IA-II

Sem : VI | Subject : VLSI Design | Sub Code : 15EC63 | Date : 13/04/18.

Q. No.	Bit	Description	Marks	CO's	RBT LEVEL
3.	a.	 — 6M.	8	CO311.2	L2
	b.	Contact – When making contacts between polysilicon and diffusion, in nMos circuits. There are three possible approaches Design rules related to Contacts — 1M. Minimum 2λ×2λ cut centered on 4λ×4λ superimposed areas of layers to be joined.  4M.	5	CO311.2	L2

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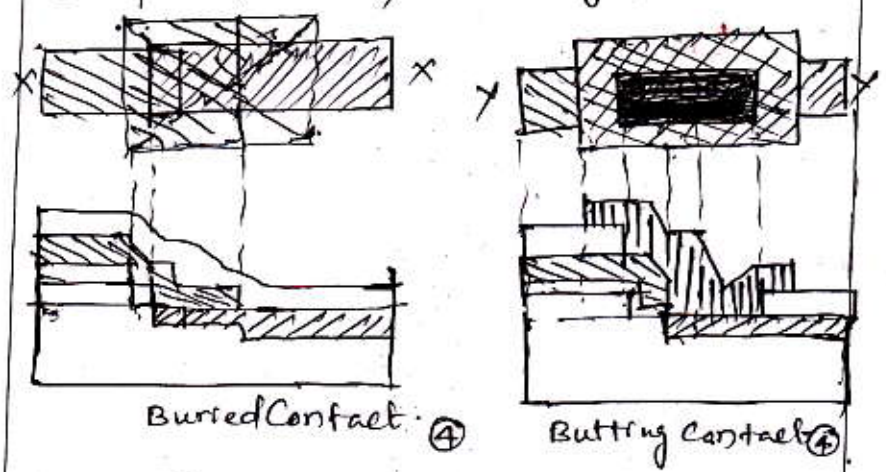
SCHEME OF EVALUATION IA-II

Sem : VI | Subject : VLSI Design | Sub Code : 15EC63 | Date : 12-04-18

Q. No.	Bit	Description	Marks	CO's	RBT LEVEL
4.	a.	Distinguish between buried and butting contact. Butting Contact: 2λ×2λ contact cut is made down to each of the layers to be joined. The layers are butted together in such a way that these two contact cuts become contiguous Buried Contact: Thin oxide is to be removed to reveal the surface of the silicon wafer before polysilicon is deposited. The polysilicon is deposited directly on the crystalline wafer.  Buried Contact ④ Butting Contact ④	8	CO3 Lt. 2	L2
	b.	Sheet Resistance (R_s). R_s – ohm per square or sheet resistance. $R_s = \rho/t$ ohm per square. 2.5M Standard Unit of Capacitance □C_g □C_g is gate channel capacitance of a MOS transistor having W = L = 2λ. i.e min. feature size. 2.5M	5	CO3 11.2	L2

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