FIRST INTERNAL ASSESSMENT

Sem :VI
Date:06/03/2018

Sub: VLSI DESIGN
Time: 11:00AM-12.00N

Sub. Code: 15EC63
Max. Marks: 25

Note: Answer two full questions, draw sketches wherever necessary.

Q. No.		Discription of Question	Marks	CO	RBT LEVEL
1.	a.	Explain nMOS enhancement mode MOSFET operation for different values of Vgs and Vds with relevant equations and necessary graphs.	6	C311. 1	L2
	b.	Derive an expression for current in n-type enhancement mode transistor in triode and saturation regions.	6	C311. 1	L3
		OR			
2.	a.	Explain the following terms briefly i)Threshold Voltage ii) Body effect	6	C311. 1	L2
	b.	Find the value of body effect parameter and threshold voltage, when the applied substrate bias is 3V. Given V_{tho} = 0.4V, NA = $10^{16}/cm^3$, thermal voltage is 26mV, $n_i = 1.5x10^{10}/cm^3$, t_{ox} = 40nm, εr (si) =11.9, εr(ox) = 3.9.	6	C311. 1	L3
3.	a.	Explain CMOS inverter transfer characteristics highlighting the regions of the operation.	8	C311. 1	L2
	b.	Explain the influence of βp /βn on the DC transfer characteristics of an Inverter.	5	C311. 1	L3
		OR			
4.	a.	What is noise margin? explain and obtain noise margin values of typical inverter.	5	C311. 1	L2
	b.	Briefly explain the steps involved in nMOS fabrication process with neat sketches.	8	C311. 1	L2

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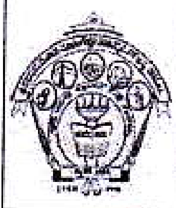
Q. No.	Bit	Description		Marks	CO's	RBT LEVEL
1	a.	nMOS enhancement mode MOSFET Structure (S, G, D; n+, n+; p-sub) — Symbol. When $V_{gs} < 0$ Accumulation mode. D no voltage. (p-sub)		1	CO311.1	L2
		$V_{gs} < V_t$ Depletion mode. (p-sub)		1		
		$V_{gs} > V_t$ Inversion mode (p-sub)		1		
		When $V_{gs} < V_t \rightarrow$ cut-off region & $V_{gs} > V_t \rightarrow$ operation region. (S, G, V_{gs}, V_{ds}, n+, n+, p-Sub) When V_{ds} is small & $V_{ds} < V_{gs} - V_t$ linear region $i_{ds} = \beta\left(V_{gs} - V_t - \frac{V_{DS}}{2}\right)V_{DS}$		1		



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Q. No.	Bit	Description		Marks	CO's	RBT LEVEL
		& when $V_{gs} > V_t$ & V_{ds} is sufficiently more $V_{ds} > V_{gs} - V_t$ — Saturation region		1		
		& current is $i_{ds} = \frac{\beta}{2}\{V_{gs} - V_t\}^2$				
		[graph: I_{ds} (uA) vs V_{ds}; linear region, saturation region; curves $V_{gs} = V_{in4}$, $V_{gs} = 2V$, $V_{gs} = 1V$, $V_{gs} = 0.8$, $V_{gs} \le V_t$; y-axis 50, 100, 150, 200, 250; x-axis 0, 0.5, 1, 1.5, 2, 2.5, 3]		1		
1	b.	Current expression. Let the nMOSFET is in linear region			CO3114	L3
		[diagram: MOSFET structure with S, D, L, W]		1		
		The current through the device is $i = \frac{dQ}{dt} \Rightarrow \frac{Q}{t}$.				
		$Q = CV$ here $C = C_g$ & $V = V_{ge} - V_t$				

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Q. No.	Bit	Description		Marks	CO's	RBT LEVEL
		$Q = C_{ox}WL.\{V_{gs} - \frac{V_{ds}}{2} - V_t\}$		1		
		& t – time related to velocity of charges				
		$v = \frac{d}{t} \Rightarrow t = \frac{d}{v}$ here $d = L$				
		$= \frac{L}{v}$.		1		
		& $v = \mu E$ & $E = \frac{V_{ds}}{L}$				
		$\Rightarrow i_{ds} = \frac{Q}{t} = \frac{C_{ox}WL\left(V_{gs} - V_t - \frac{V_{ds}}{2}\right)}{L/\mu\frac{V_{ds}}{L}}$		1		
		$= \mu C_{ox}\frac{W}{L}\left(V_{gs} - V_t - \frac{V_{ds}}{2}\right)V_{ds}$			CO311.1	
		in triode region.		1		
		$i_{ds} = \beta\left(V_{gs} - V_t - \frac{V_{ds}}{2}\right)V_{ds}$.				
		& when $V_{ds} = V_{gs} - V_t$ → we get saturation region current		1		
		$i_{ds} = \frac{\beta}{2}(V_{gs} - V_t)^2$				
2	a.	Threshold Voltage (V_t).				
		The voltage above which channel is formed.				
		$V_{gs} > V_{tn}$. V_{tn} – nMOS threshold voltage (+)ve.				L2
		$V_{gs} < V_t$ – Cut-off region.		1		
		V_{gs} i/p, as source is grounded.			CO311.1	
		PMOSFET: V_{tp} – threshold voltage (-)ve.		1		
		$V_{gs} < V_t$ for 'ON or channel formation or V_g or $V_{in} < V_{DD} - \lvert V_{tp}\rvert$.		1		
		$V_{in} > V_{DD} - \lvert V_{tp}\rvert$ ie $V_{gs} > V_{tp}$ OFF.				

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Sem :		Subject :	Sub Code :	Date :		
Q. No.	Bit	Description		Marks	CO's	RBT LEVEL
		& When $V_{gs} > V_t$ & V_{ds} is sufficiently more $V_{ds} > V_{gs} - V_t$ — Saturation region & current is $i_{ds} = \frac{\beta}{2}\{V_{gs} - V_t\}^2$		1		
		[Graph: I_{ds} (uA) vs V_{ds}; linear region; saturation region; $V_{gs} = V_{in4}$; $V_{gs} = 2V$; $V_{gs} = 1V$; $V_{gs} = 0.8$; $V_{gs} \leq V_t$; y-axis 50, 100, 150, 200, 250; x-axis 0, 0.5, 1, 1.5, 2, 2.5, 3]		1		
1	b.	Current expression. Let the nMOSFET is in linear region			CO311.1	
		[Diagram: S, L, D, W]		1		L3
		The current through the device is $i = \frac{dQ}{dt} \Rightarrow \frac{Q}{t}$. $Q = CV$ here $C = C_g$ & $V = V_{gs} - V_t$				

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Q. No.	Bit	Description		Marks	CO's	RBT LEVEL

$Q = C_{ox}WL \cdot \{V_{gs} - \frac{V_{ds}}{2} - V_t\}$ — 1

& t - time related to velocity of charges

$v = \frac{d}{t} \Rightarrow t = \frac{d}{v}$ here $d = L$

$= \frac{L}{v}$ — 1

& $v = \mu E$ & $E = \frac{V_{ds}}{L}$

$\Rightarrow i_{ds} = \frac{Q}{t} = \frac{C_{ox}WL\left(V_{gs} - V_t - \frac{V_{ds}}{2}\right)}{L / \frac{\mu V_{ds}}{L}}$ — 1

$= \mu C_{ox}\frac{W}{L}\left(V_{gs} - V_t - \frac{V_{ds}}{2}\right)V_{ds}$ (CO311.1)

in triode region. — 1

$i_{ds} = \beta\left(V_{gs} - V_t - \frac{V_{ds}}{2}\right)V_{ds}$.

& when $V_{ds} = V_{gs} - V_t \rightarrow$ we get saturation region current — 1

$i_{ds} = \frac{\beta}{2}(V_{gs} - V_t)^2$

Q. 2 a. Threshold Voltage (V_t).

The voltage above which channel is formed.

$V_{gs} > V_{tn}$. V_{tn} - nMOS threshold voltage. (+)ve.

$V_{gs} < V_t$ - cut-off region. — 1 (RBT: L2)

V_{gs} i/p, as source is grounded. (CO311.1)

PMOSFET: V_{tp} - threshold voltage (-)ve. — 1

$V_{gs} < V_t$ for 'ON or channel formation

or V_g or $V_{in} < V_{DD} - |V_{tp}|$. — 1

$V_{in} > V_{DD} - |V_{tp}|$ ie $V_{gs} > V_{tp}$ OFF.

SCHEME OF EVALUATION

Sem :		Subject :	Sub Code :	Date :		
Q. No.	Bit	Description		Marks	CO's	RBT LEVEL
2.	b	Body Effect: The potential difference between the body & Source V_{sb} affects threshold voltage $V_t = V_{to} + \gamma\{\sqrt{\phi_s + V_{sb}} - \sqrt{\phi_s}\}$ ϕ_s – surface potential γ – body effect parameter (0.4 to $1\ V^{1/2}$) $N_A \rightarrow$ doping level $\phi_s = 2v_T \ln N_A/n_i$ $\gamma = \frac{t_{ox}}{\varepsilon_{ox}}\sqrt{2q\varepsilon_{si}N_A}$		1 1 1	CO311.1	
2	b.	$\gamma = ?$ $V_t = ?$ $V_{sb} = 3V$, $V_{to} = 0.4V$, $N_A = 10^{18}/cm^3$ $v_T = 0.026$, $n_i = 1.5\times10^{10}/cm^3$ $t_{ox} = 40nm$, $\varepsilon_r = 11.9$ $\varepsilon_{rox} = 3.9$ $\gamma = \sqrt{2q\varepsilon_{si}N_A}/C_{ox}$ $\{C_{ox} = \frac{t_{ox}}{\varepsilon_{ox}}$ $= \frac{40\times10^{-7}\sqrt{2\times1.6\times10^{-19}\times11.9\times8.854\times10^{-12}\times10^{18}}}{3.9\times8.854\times10^{-12}}$ $= 0.672$ $V_t = V_{to} + \gamma(\sqrt{\phi_s + V_{sb}} - \sqrt{\phi_s})$. $\phi_s = 2V_T \ln\frac{N_A}{n_i} = 2\times0.026 \ln\frac{10^{18}}{1.5\times10^{10}}$ $= 0.936$ $V_t = 0.4 + 0.672(\sqrt{0.936+3} - \sqrt{0.936})$ $1.984 - 0.967$ $= 0.4 + 0.459 = 0.859V$.		2 2 2	CO311.1	L3

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Sem :		Subject :	Sub Code :	Date :		
Q. No.	Bit	Description		Marks	CO's	RBT LEVEL
3.	a	CMOS inverter transfer characteristics [CMOS inverter circuit: V_{DD}, i/p, o/p] — ① [Transfer characteristic: V_{out} vs V_{in}, regions A, B, C, D, E, V_{DD}, 0] — ② Cut-off / linear / Saturation: nMOS: $V_{gs}<V_{tn}$ / $V_{gs}>V_t$, $V_{ds}<V_{gs}-V_t$ / $V_{gs}>V_t$, $V_{ds}>V_{gs}-V_t$ pMOS: $V_{gs}>V_t$ / $V_{gs}<V_t$, $V_{ds}>V_{gs}-V_t$ / $V_{gs}<V_t$, $V_{ds}<V_{gs}-V_t$ — 2 i/p — o/p — Region — nMOS — pMOS $V_{in}\approx 0<V_{tn}$ — $\approx V_{DD}$ — A — Cut-off — linear $V_{tn}<V_{in}<\frac{V_{DD}}{2}$ — $>\frac{V_{DD}}{2}$ — B — Saturation — linear $\frac{V_{DD}}{2}$ — $\frac{V_{DD}}{2}$ — C — Saturation — Saturation $\frac{V_{DD}}{2}<V_{in}<V_{DD}-\lvert V_{tp}\rvert$ — $<\frac{V_{DD}}{2}$ — D — linear — Saturation $V_{in}>V_{DD}-\lvert V_{tp}\rvert$ — ≈ 0 — E — linear — cut off — 2 explanation — ①			CO311.1	L2
3.	b.					

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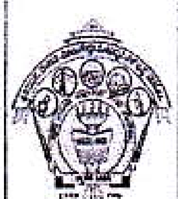

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Q. No.	Bit	Description		Marks	CO's	RBT LEVEL
3.	b.	β_p/β_n ratio. [VTC plot: V_{out} vs V_{in} for $\beta_p/\beta_n = 0.1, 1, 2, 10$]. $\frac{\beta_p}{\beta_n} = 1$ unskewed; >1 HI skewed; <1 LO skewed.		1, 3	CO311.1	L3
		$\beta_p = \mu_p C_{ox}\left(\frac{W}{L}\right)_p$, $\beta_n = \mu_n C_{ox}\left(\frac{W}{L}\right)_n$; $\beta_p = \beta_n \Rightarrow \left(W/L\right)_p = \frac{\mu_n}{\mu_p}\left(\frac{W}{L}\right)_n$.		2		
4.	a.	Noise Margin: $NM_H = V_{OH} - V_{IH}$, $NM_L = V_{IL}$		1		
		[Diagram: two cascaded inverters, o/p and i/p; level bars showing V_{OH}, NMH, V_{IH}, NML, V_{IL}, V_{OL}]		1+1	CO311.1	L2
		explanation & values of typical inverter. $NM_H = NM_L \approx \frac{V_{DD}}{2}$. [VTC plot: V_{out} vs V_{in}, with V_{OH}, V_{OL}, slope -1 points, 0, V_{IL}, V_{IH}]		2		

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Sem :		Subject :	Sub Code :	Date :		
Q. No.	Bit	Description		Marks	CO's	RBT LEVEL
4.	b.	nMos fabrication Process.				
		① p-sub. 75-150mm, 0.4mm thick, $10^{15}-10^{16}/cm^3$, $R \rightarrow 2-25\Omega/cm$. substrate.		1		
		② p-sub. 1μm SiO2. oxide layer			CO311.1	
		③ p-sub. photoresistive layer. oxide layer		1		L2
		④ Mask-1. p-sub. photoresistive layer. SiO2		1		
		⑤ p-sub. window in oxide.		1		
		⑥ poly. 1-2 μm. 100Å-1000Å thin oxide. by CVD. p-sub. oxide & poly pattern.		1		

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4	b.	(7). poly, 1um deep, n+, n+, p-sub. n+ diffusion; heating & passing phosphorous ions		1	CO311.1	L2
		(8) 1um SiO2, n+, n+, p-sub. Contact holes.		1		
		(9). 1um aluminum, n+, n+, p-sub. patterned metalization		1		
		with explanation stepwise.				

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