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*Inculcating Values, Promoting Prosperity*

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| ECE Dept. |
| DSDV |
| VI Sem |
| 2017-18 |

## Department of Electronics & Communication Engg.

**Course : Digital System Design using Verilog.** **Sem.: 6th (2017-18)**

## Course Coordinator:

## Prof. D. M. Kumbhar

# Digital System Design Using Verilog

## Module 5

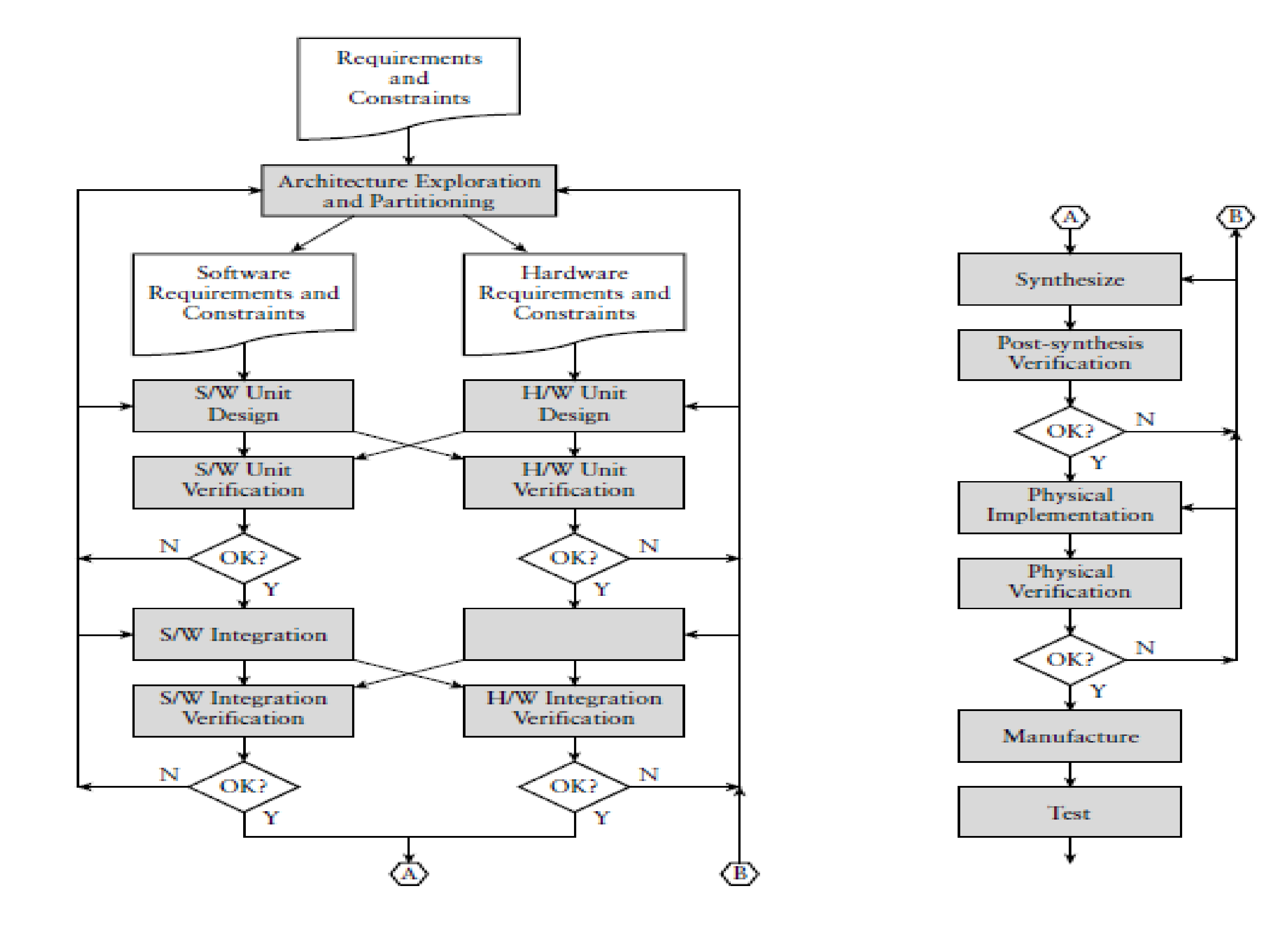
## Design Methodology

Portions of this work are from the book, *Digital Design: An Embedded Systems Approach Using Verilog,* by Peter J. Ashenden, published by Morgan Kaufmann Publishers, Copyright 2007 Elsevier Inc. All rights reserved.

# DESIGN FLOW

- Digital system design
  - Complex – expert team
  - Systematic design approach – manage complexity and interconnection between components
- Design methodology
  - Systematic approach of design, verification and preparation for implementation
- Many projects fail lack of control
- Standard design methodology
- Prototype design methodology

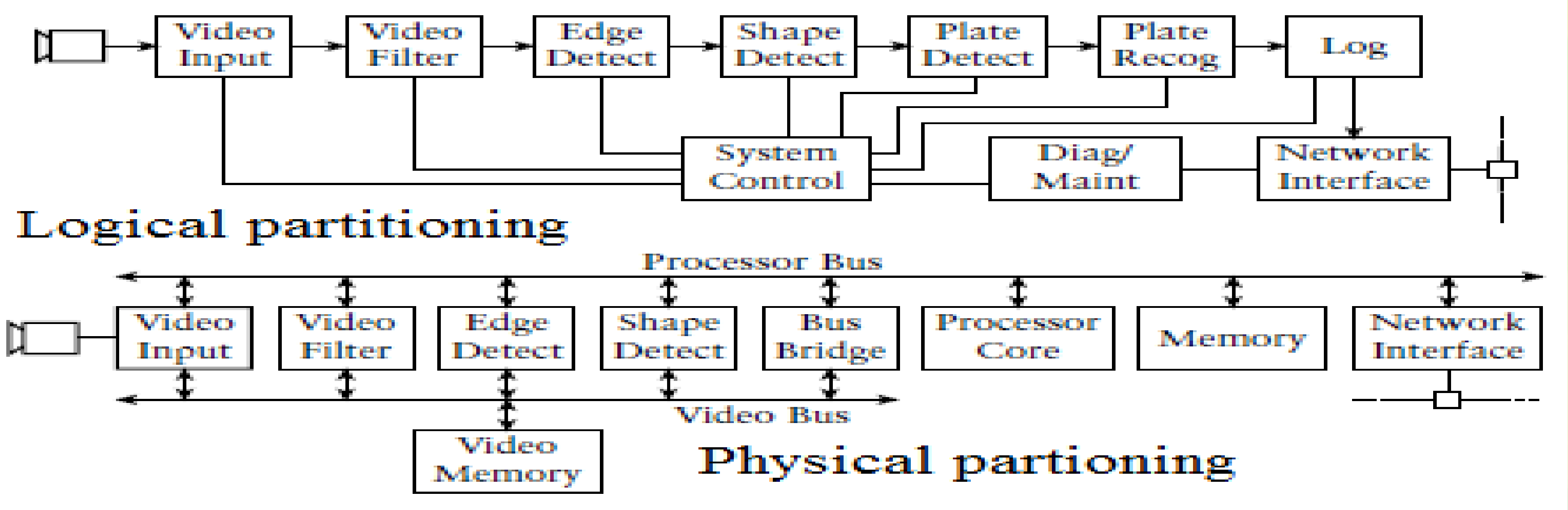
# PROTOTYPE DESIGN METHODOLOGY


Requirements and Constraints
Architecture Exploration and Partitioning
Software Requirements and Constraints
Hardware Requirements and Constraints
S/W Unit Design
H/W Unit Design
S/W Unit Verification
H/W Unit Verification
N
OK?
Y
OK?
N
Y
S/W Integration
S/W Integration Verification
H/W Integration Verification
N
OK?
Y
OK?
N
Y
A
B
A
B
Synthesize
Post-synthesis Verification
OK?
N
Y
Physical Implementation
Physical Verification
OK?
N
Y
Manufacture
Test

# Architecture exploration

- Functional requirements and constraints
- Small modifications / new requirement
  - Violet/satisfy constraints – cost, performance, power consumption, reliability
  - Candidate – various design approaches
- Architecture exploration refers to the task of abstract modeling and analysis of candidate design
- Partitioning – divide problem to sole complexity
  - Logical partitioning
  - Physical partitioning
  - Hardware software partitioning

# Example of Partitioning



- Road transport monitoring system
- Logical and *physical components* – *video from camera, filtering to remove noise, edge detection, shape detection*, license plate detection, character recognition for number, logging, n/w interface, control, diagnostic & maintenance task.

# Floor planning

- Physical design types – ASISs & FPGA
- ASIC – floor planning, placement, routing
  - 1. Placement – cell & sub cell, closer, external connection
  - 2. Routing – wire length, conjunction of wiring
  - DIP, QFP, PGA, BGA
  - 3 Arrangement of power supply, ground & internal connection
  - Clock pin & distribution of clock
- FPGA – same physical design steps but good planning for interconnections
- Good floor planning – reducing interconnections, it’s length, faster design, good I/O block connection

# Functional Design

- Architectural Design - top level
  - Each block/ component – sub component unless complexity manageable
  - Develop behavioral model – expressing functionality, functional verification, test bench
- Implement given component several approaches
  - Reuse components from previous system – intellectual property (IP) – less effort, reduced time & verification.
  - No reusable IP – component from scratch – extra efforts, verify functionality
  - Core generator EDA tool – common functions available such as memories, ALUs, bus interfaces, FSM e.g. Xilinx core gene
- Revision management – source code control

Multiple design engineers revise code called repository version

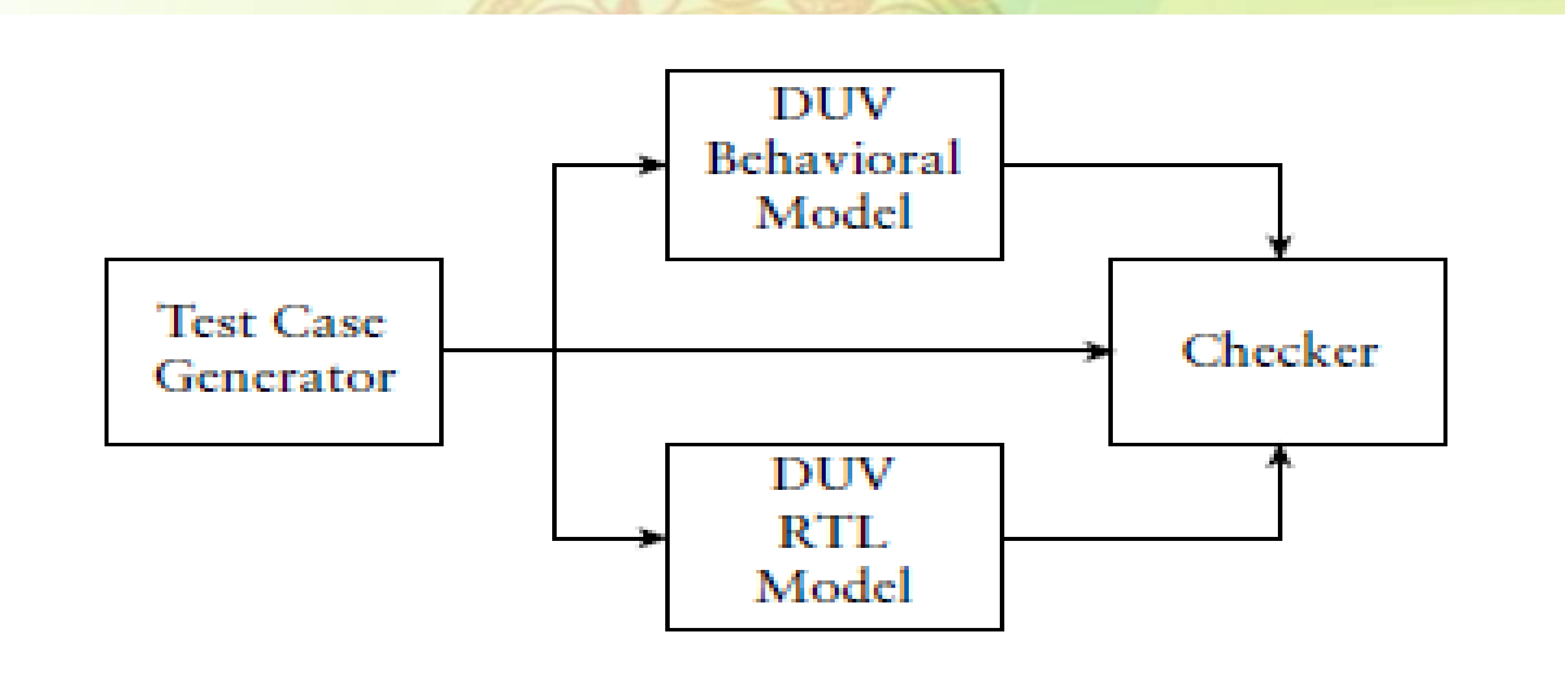
Completed change  affects various parts of code – EDA Verification.

# Functional Verification

- Simulation based verification
  - Code Generator and checker
  - First question, what parts to verify – subsystem, top up process
  - Second question, what functionality to verify – each component
  - Coverage - functional coverage
  - The third question in the verification plan is how to verify. – Directed testing – DUV (simpler components), constrained random testing (complex components)
  - Verification language - Vera & e

# Functional Verification

- Both Directed testing, constrained random testing
- Checker



# Functional Verification

- Coverage – less
- Formal verification 100% coverage
- Property specification language
- State-space exploration
- Hardware/Software Co-Verification

# Scan Chain

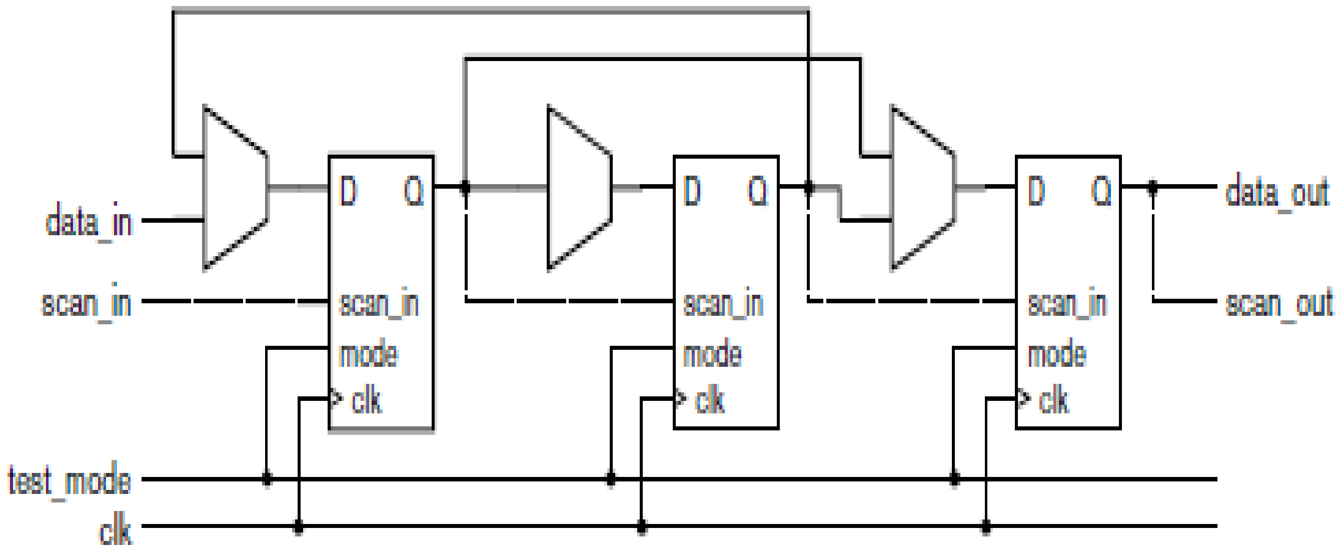


FIGURE 10.12 Connection of modified registers in a scan chain.

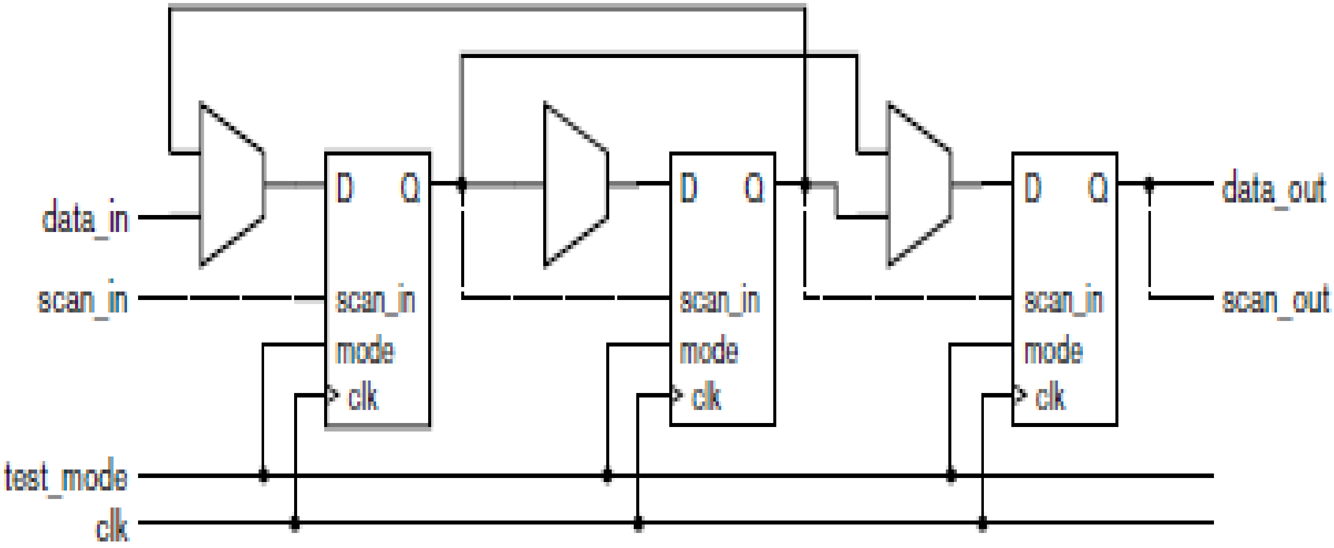
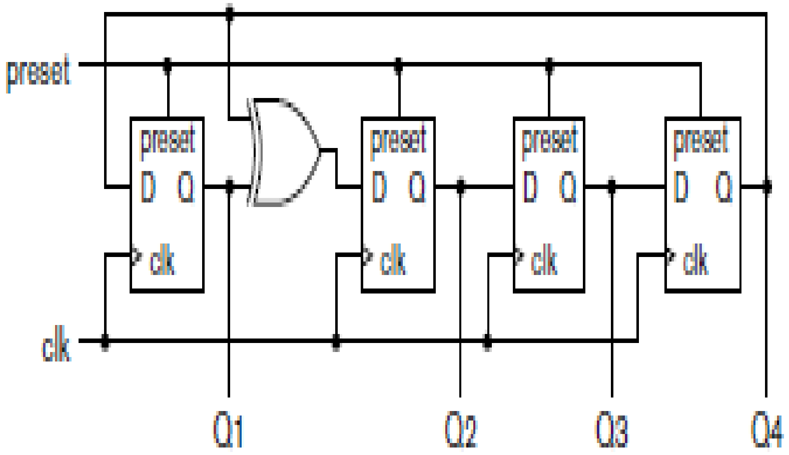


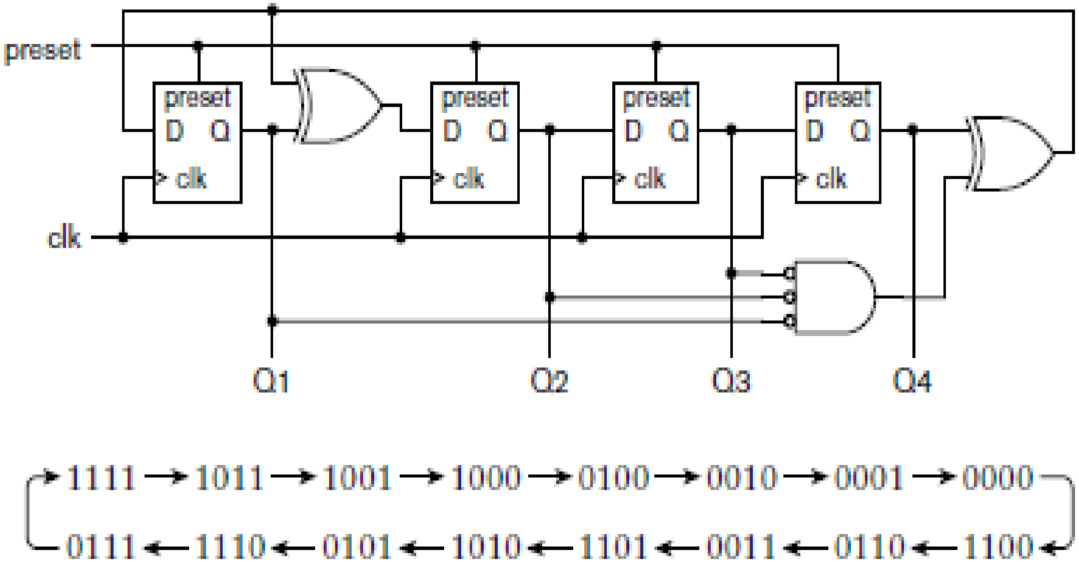
FIGURE 10.12 Connection of modified registers in a scan chain.



1111 → 1011 → 1001 → 1000 → 0100 → 0010 → 0001 → 1100

0111 ← 1110 ← 0101 ← 1010 ← 1101 ← 0011 ← 0110

FIGURE 10.17 A 4-bit LFSR for generating pseudo-random test vectors.

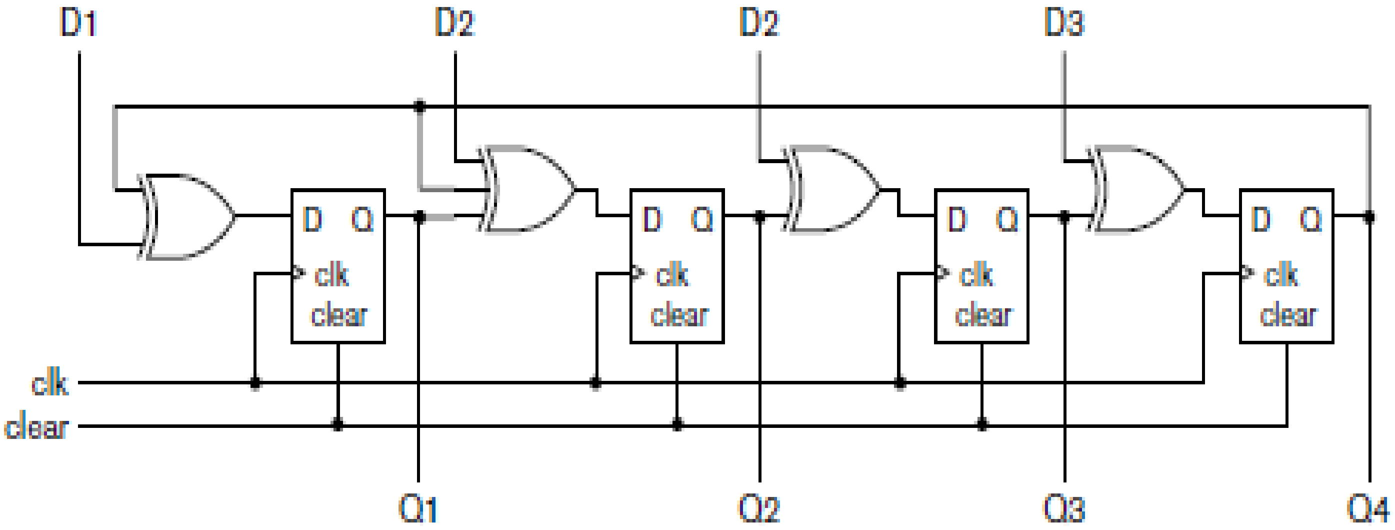


1111 → 1011 → 1001 → 1000 → 0100 → 0010 → 0001 → 0000

0111 ← 1110 ← 0101 ← 1010 ← 1101 ← 0011 ← 0110 ← 1100

FIGURE 10.18 A 4-bit CFSR for generating pseudo-random test vectors.

FIGURE 10.19 A 4-bit MISR with four inputs from a circuit under test.



# Queries ….?