Department of Electronics & Communication Engg.

Course : Digital System Design using Verilog. **Sem.: 6th (2017-18)**

Course Coordinator:

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Digital System Design Using Verilog

Module 3

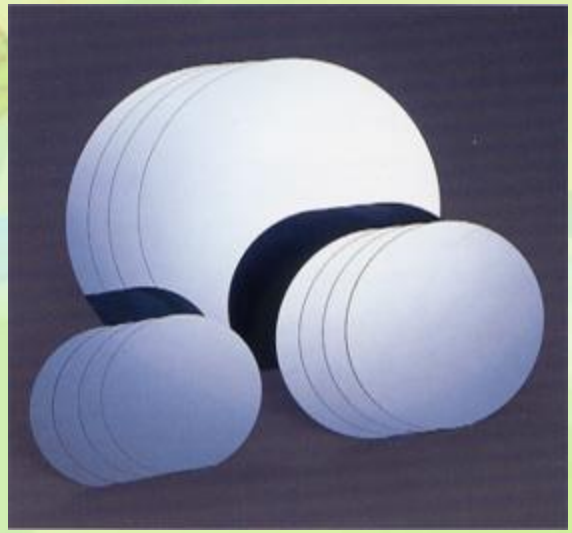
Implementation Fabrics

Integrated Circuits

- Early digital circuits
  - Relays, vacuum tubes, discrete transistors
- Integrated circuits (ICs, or “chips”)
  - Manufacture of multiple transistors and connections on surface of silicon wafer
  - Invented in 1958: Jack Kilby at Texas Instruments (TI)
  - Rapid growth since then, and ongoing

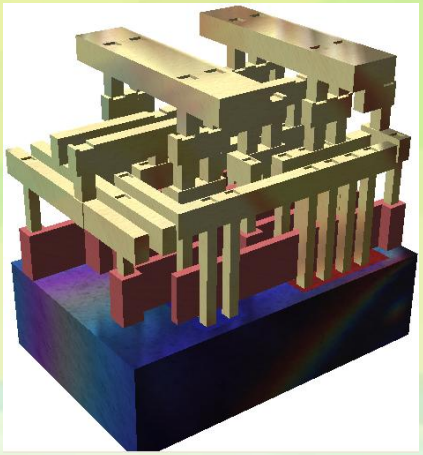
IC Manufacture: Wafers

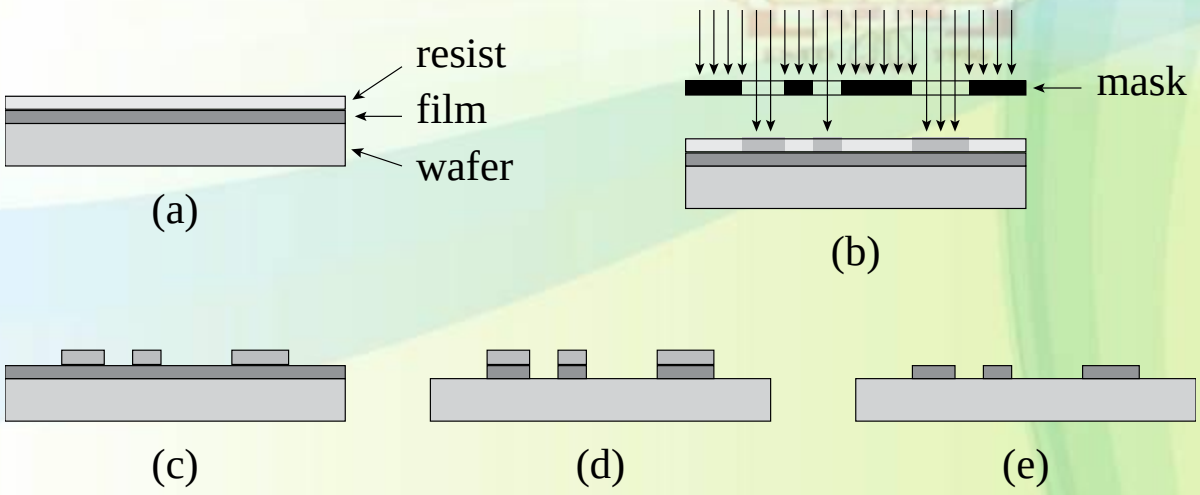
- Start with ingot of pure silicon
- Saw into wafers & polish
  - Early wafers: 50mm
  - Now 300mm

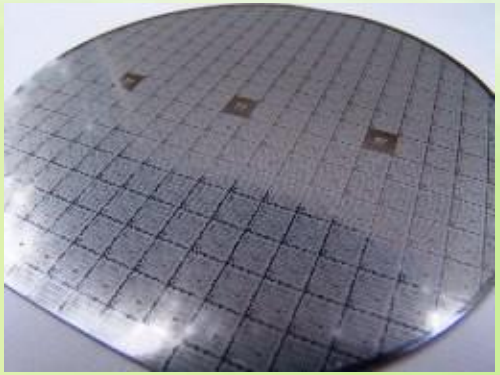


IC manufacture: Processing

- Chemical processing steps based on photolithography
  - Ion implantation
  - Etching a deposited film
    - SiO_2, polysilicon, metal







IC Manufacture: Test & Packaging

- Defects cause some ICs to fail
  - Test to identify which ICs don't work
  - Discard them when wafer is broken into chips
    - Their cost is amortized over working chips
  - Yield depends (in part) on IC area
    - Constrain area to reduce final IC cost
- Working chips are packaged and tested further

Exponential Trends

- Circuit size and complexity depends on minimum feature size
  - Which depends on manufacturing process
    - Mask resolution, wavelength of light
- Process nodes (ITRS Roadmap)
  - 350nm (1995), 250nm (1998), 180nm (2000), 130nm (2002), 90nm (2004), 65nm (2007), 45nm (2010), 32nm (2013), 22nm (2016), 16nm (2019)
  - Smaller feature size $\Rightarrow$ denser, faster

SSI and MSI

- In 1964, TI introduced 5400/7400 family of TTL ICs
  - Other manufacturers followed, making 7400 family a de facto standard
  - Small-scale integrated (SSI)
    - 7400: 4 × NAND gate
    - 7427: 4 × NOR gate
    - 7474: 2 × D flip-flop
    - …
  - Medium-scale integrated (MSI)
    - 7490: 4-bit counter
    - 7494: 4-bit shift reg
    - …

Other Logic Families

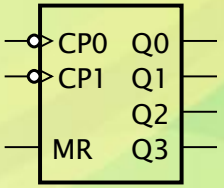
- Variations on electrical characteristics
  - 74L… : low power
  - 74S… : Schottky diodes ⇒ fast switching
  - 74LS… : compromise between speed and power
  - 74ALS… : advances low-power Schottky
  - 74F… : fast
- CMOS families
  - 4000 family: very low power, 3–15V
  - 74HC…, 74AHC… : TTL compatible

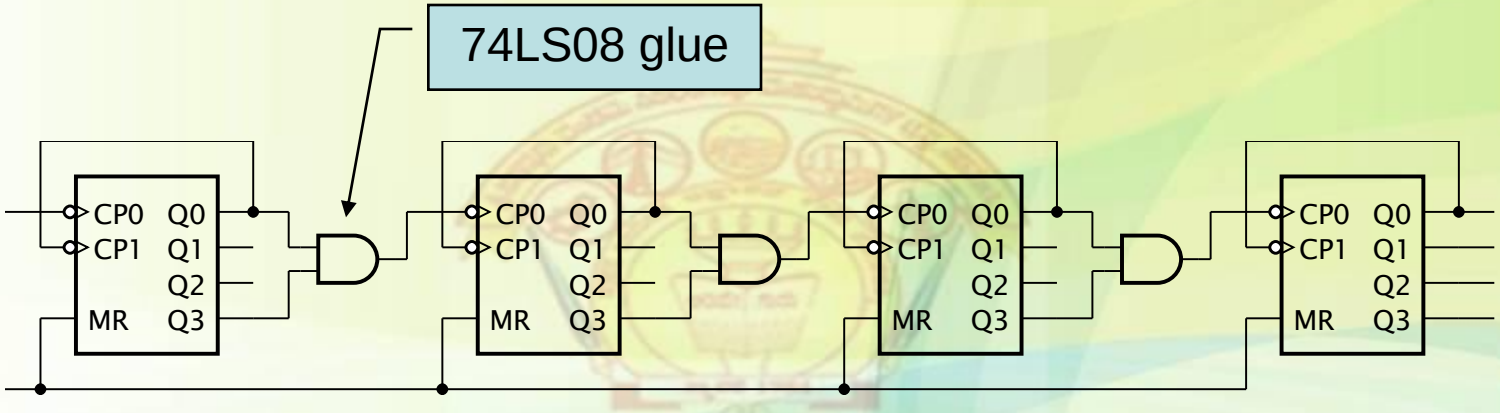
Large Scale Integration

- 1970s: LSI (thousands of transistors)
  - Small microprocessors became feasible
  - Custom LSI chips for high-volume applications
- SSI/MSI mainly used for glue logic
- Later additions to 74xx… families oriented toward glue-logic and interfacing
  - E.g., multibit tristate drivers, registers
  - Other functions supplanted by PLDs

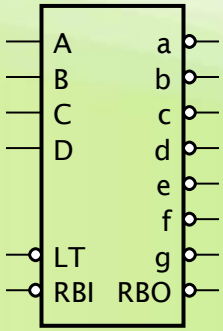
MSI Example: Counter/Display

- 74LS390: dual decade counter

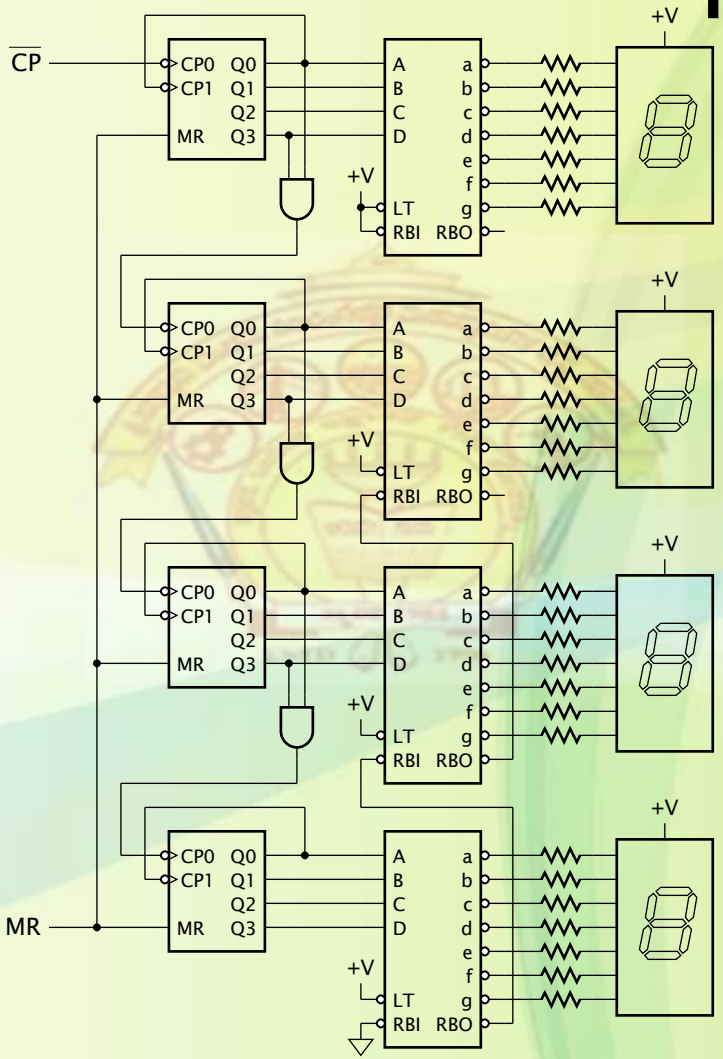




- 74LS47: 7-segment decoder



MSI Example: Counter/Display



VLSI and ASICs

- 1980s: Very Large Scale Integration
  - Then ULSI, then what?
  - VLSI now just means IC design
- Application-specific ICs (ASICs)
  - Enabled by CAD tools, foundry services
  - Often designed for a range of related products in a market segment
    - Application-specific standard products (ASSPs)
    - E.g., cell phone ICs

ASIC Economics

- ASIC has lower unit cost than an FPGA
  - But more design/verification effort
  - Higher non-recurring engineering (NRE) cost
    - Amortized over production run
  - ASICs make sense for high volumes
  - Performance of ASIC & FPGA
- Full custom
  - Design each transistor and wire
  - High NRE, but best performance & least area
  - Design expertise team
- Standard cell
  - Use basic components from a foundry's library
  - Previous designs / ASIC Venders design

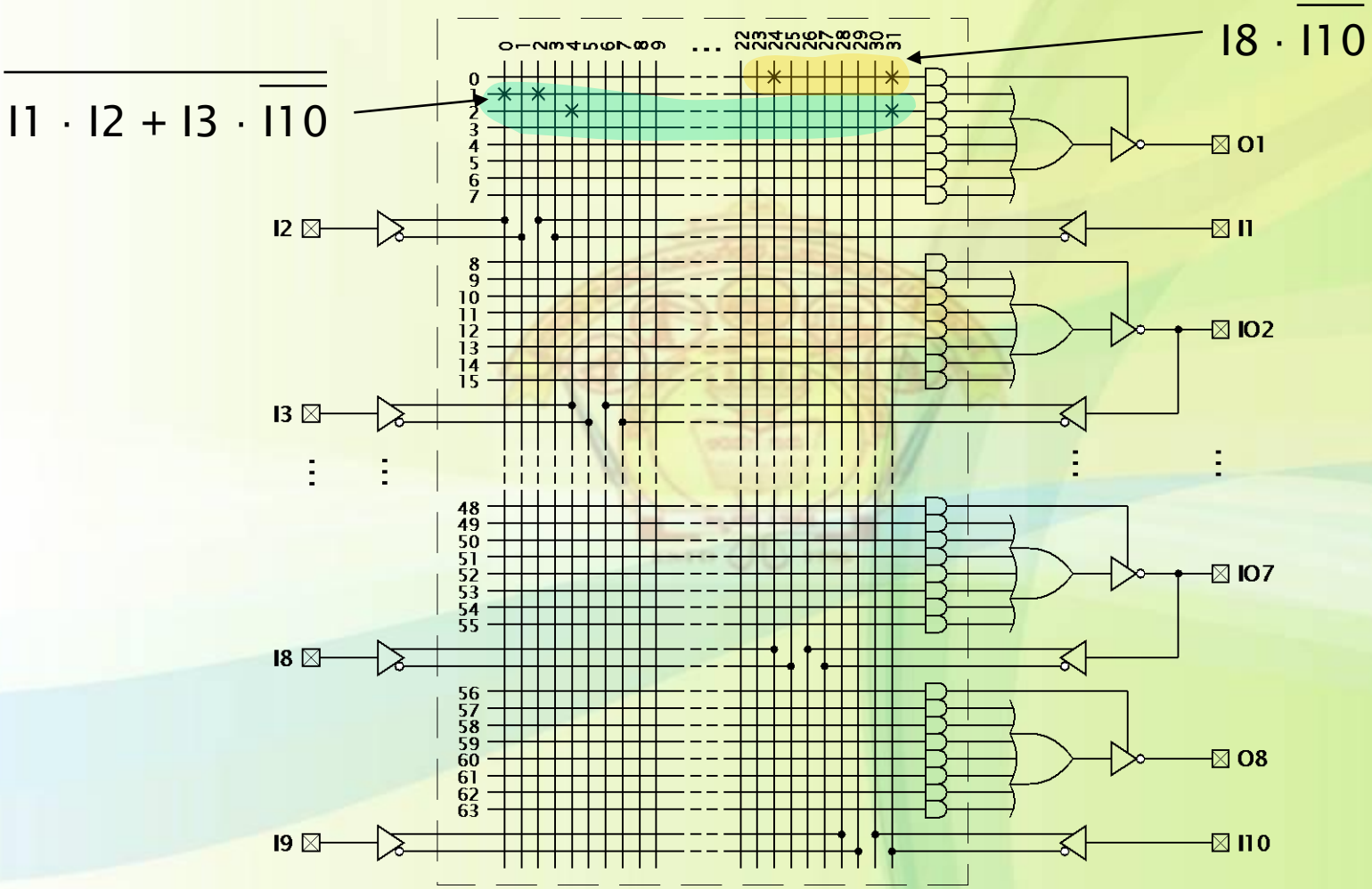
Programmable Logic Devices (PLDs)

- PLDs can be programmed after manufacture to vary their function
  - C.f. fixed-function SSI/MSI ICs and ASICs
- Higher unit cost than ASIC
  - But lower NRE
  - Ideal for low to medium product volumes

Programmable Array Logic (PALs)

- Introduced by Monolithic Memories Inc in 1970s
  - First widely-used PLDs
  - Programmed by blowing fusible links in the circuit
    - Use a special programming instrument
- PAL16L8
  - 16 inputs, 8 active-low outputs
  - 10-I/P, 2-O/P, 6-both I/O
- PAL16R8
  - 16 inputs, 8 registered outputs

PAL16L8


$\overline{I1 \cdot I2 + I3 \cdot \overline{I10}}$
$I8 \cdot \overline{I10}$
0 1 2 3 4 5 6 7 8 9 ... 22 23 24 25 26 27 28 29 30 31
0
2
3
4
5
6
7
8
9
10
11
12
13
14
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48
49
50
51
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57
58
59
60
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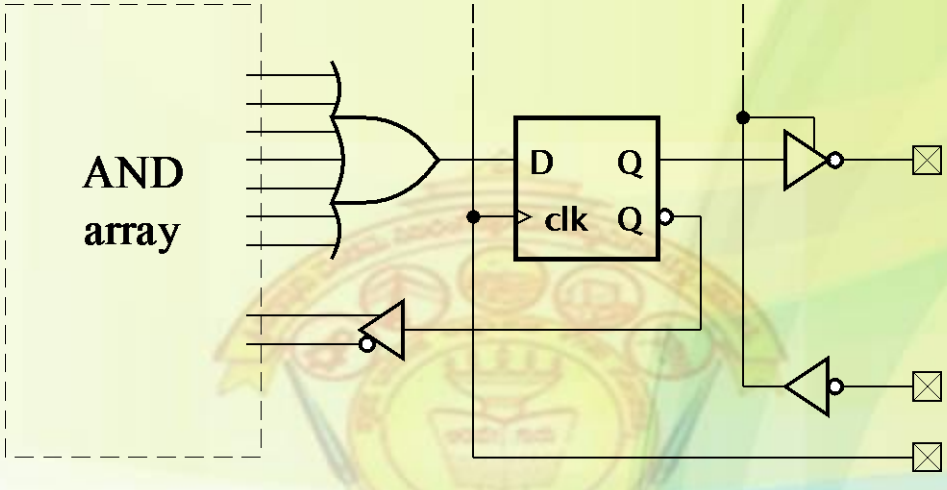
62
63
I2
I3
I8
I9
O1
I1
IO2
IO7
O8
I10

PAL16R8 Output Circuit

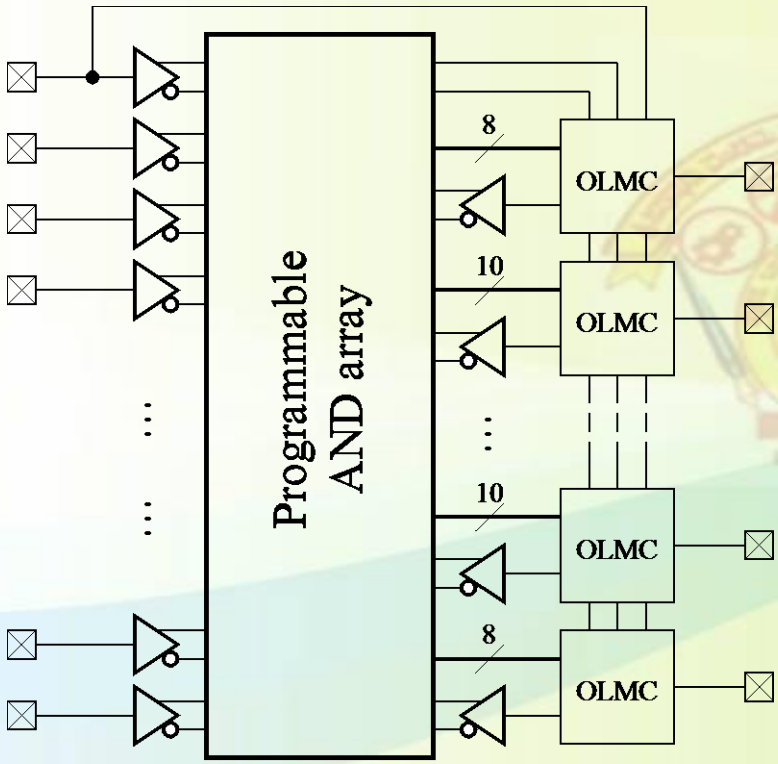


- Feedback path is useful for implementing FSMs

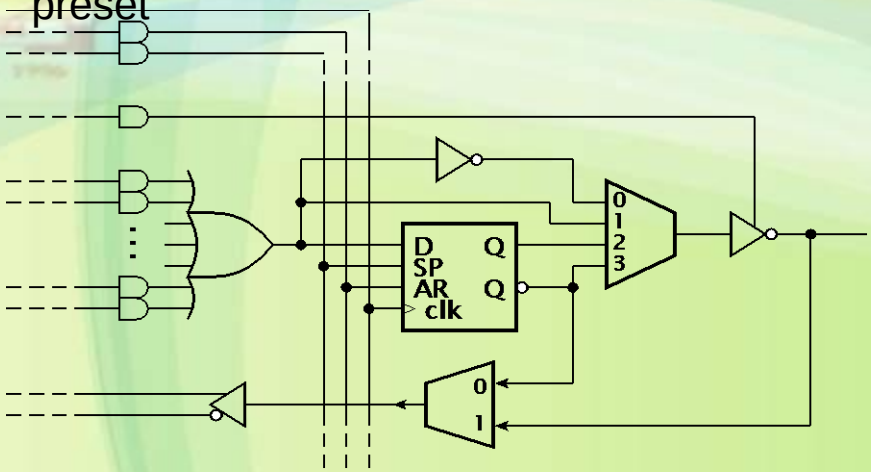
Designing with PALs

- Useful even for simple circuits
  - Single package solution lowers cost
- Describe function using Boolean equations
  - In HDL, or simple language
  - Synthesize to fuse map file used by programming instrument
  - If design doesn't fit
    - Partition into multiple PALs or use a more complex PLD

Generic Array Logic (GALs)

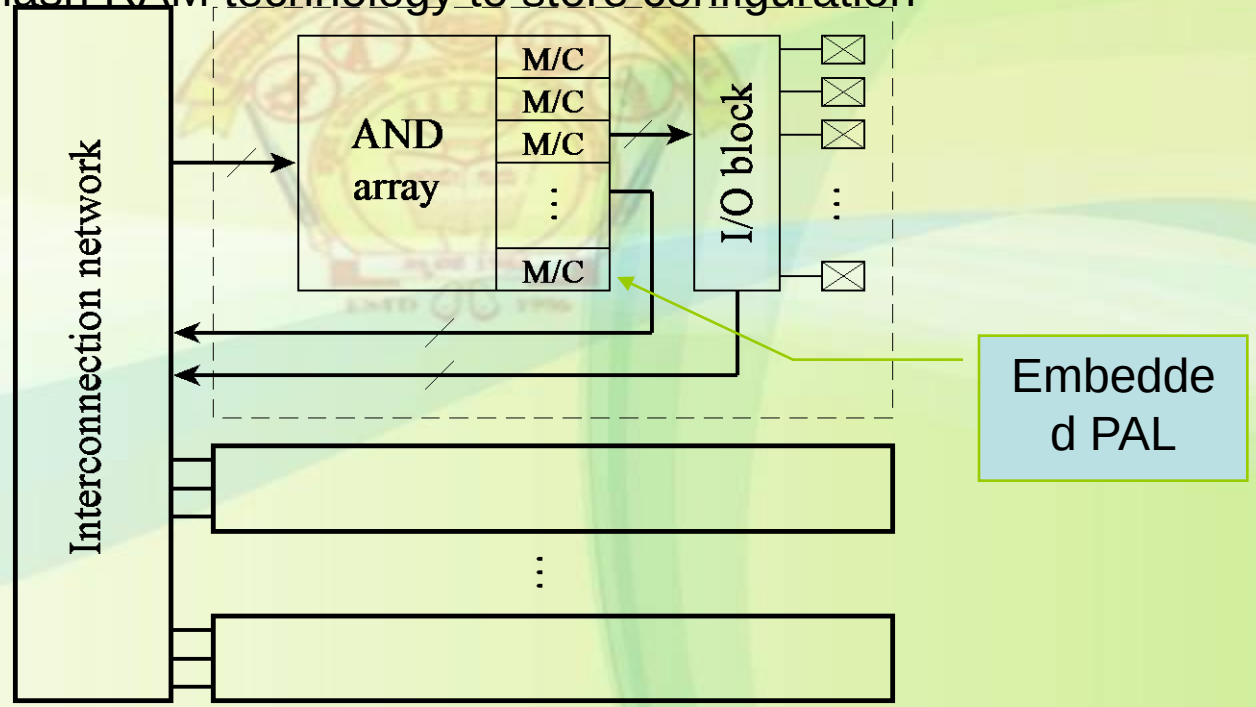


- PAL varies- o/p inverting or not, registers ?, o/p feedback to i/p ?
- Programmable Output Logic Macrocells (OLMCs)
  - OLMC replace OR gate, registers, tristate drivers
  - Use EEPROM technology
  - E.g. GAL22V10 –prog mux, OLMC-reset preset



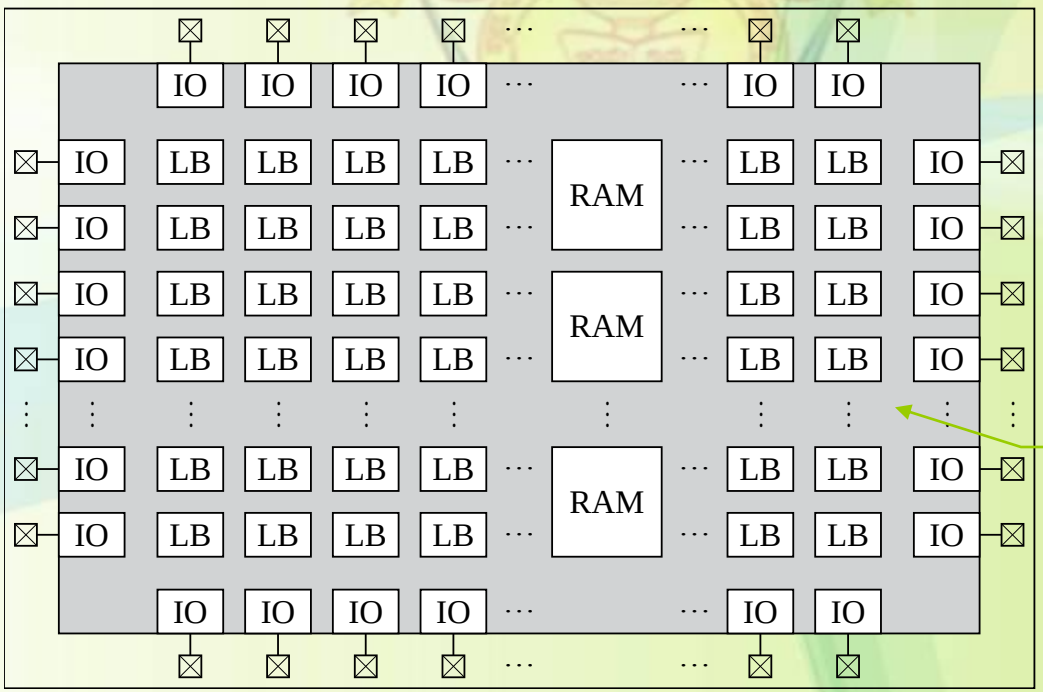
Complex PLDs (CPLDs)

- Cramming multiple PALs into an IC
  - Programmable interconnection network, PAL
  - PAL – AND array, macrocells (M/C), I/O block
  - M/C- OR gates, mux, F/F (choice combinational/registered connection)
  - Use flash RAM technology to store configuration



FPGAs

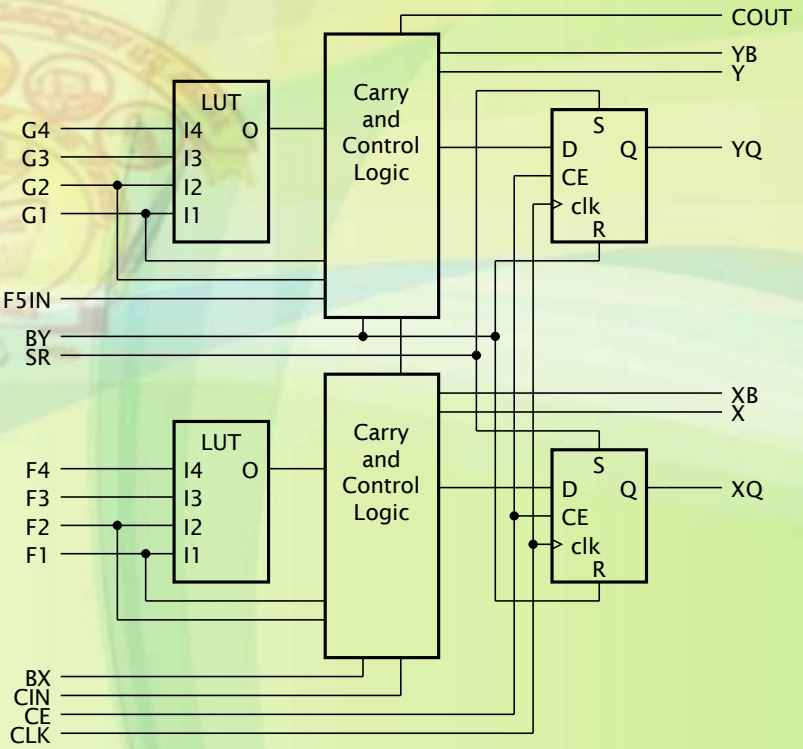
- Larger CPLDs- replica of PAL, but limitations mapping of resources, insufficient use of resources on chip
- Field Programmable Gate Arrays
  - Smaller logic blocks, embedded SRAM, interconnection N/W
  - Thousands or millions of equivalent gates
  - LB logic block- simple combinational & sequential logic functions



Logic Block Example

- Xilinx FPGA Logic Blocks
  - Lookup Tables (LUTs) plus flip-flops
  - E.g., Spartan-II

- Too complex to program LBs manually
  - Let synthesis tools map HDL code to LBs and program the interconnect



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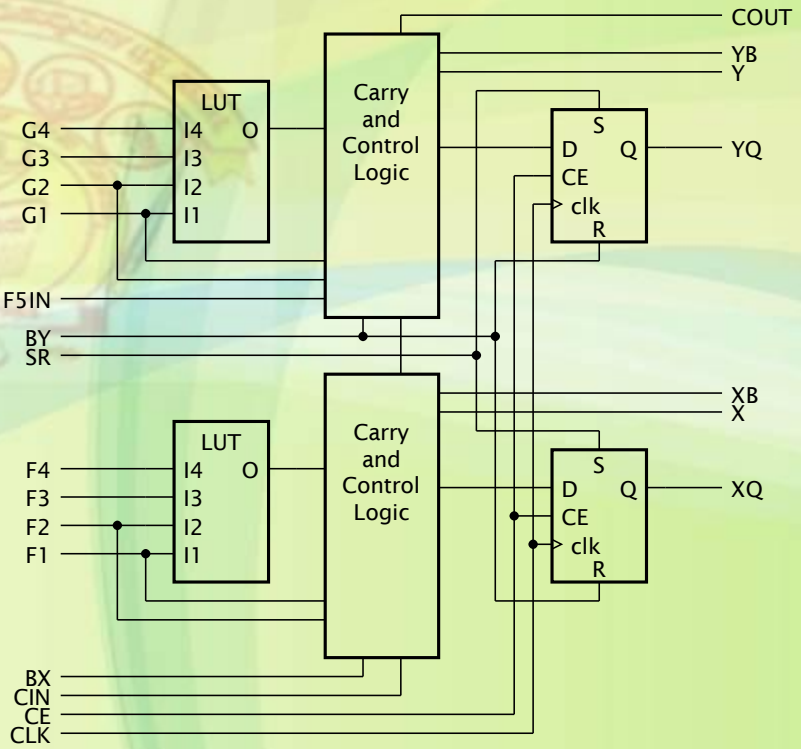


Platform FPGAs

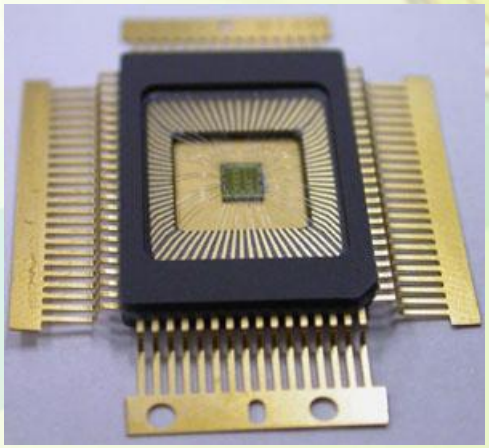
- Include embedded cores for special applications
  - Processor cores
  - Signal processing arithmetic cores – arithmetic circuits
  - Network interface cores – Tx, Rx
- Embedded software can run from SRAM in the FPGA
  - Single-chip solution, reduces cost
  - Avoids high NRE of ASIC

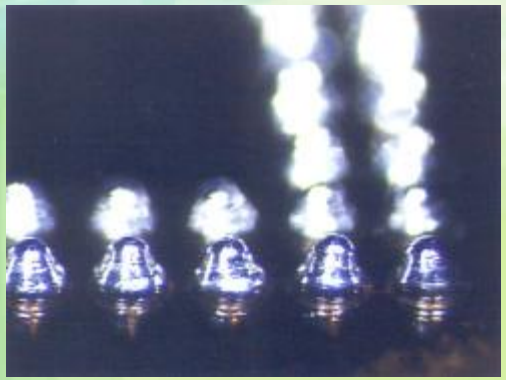
Structured ASICs

- Midway PLDs & standard cell ASICs
- Array of very simple logic elements
  - Not programmable, no programmable interconnect
- FPGA Customized by loading a configuration program
- Structured ASIC Customized by designing top metal interconnection layer(s)
  - Lower NRE than full ASIC design
  - Performance close to full ASIC
- May become popular for mid-volume applications

IC Packages

- Different IC Packages- different physical, electrical and thermal properties
- ICs are encapsulated in protective packages
  - Gold wires
  - External pins for connected to circuit board
  - Bond-wires or flip-chip connections



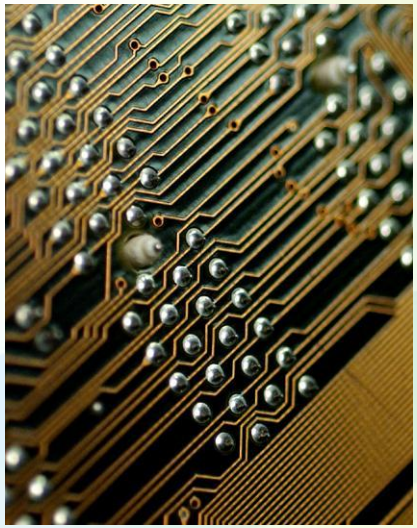


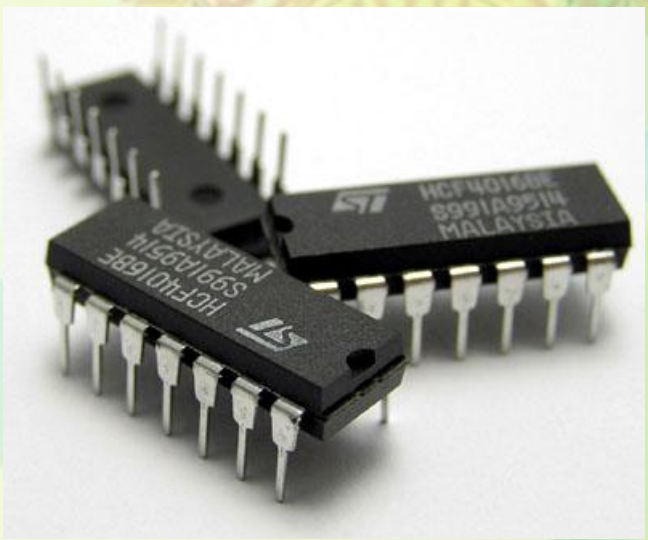
Printed Circuit Boards (PCBs)

- Layers of conducting wires (copper) between insulating material (fiberglass)
  - Manufactured using photolithography and etching
- Wires interconnect ICs and other components
  - External connections to other system components
  - Via connection

Through-Hole PCBs

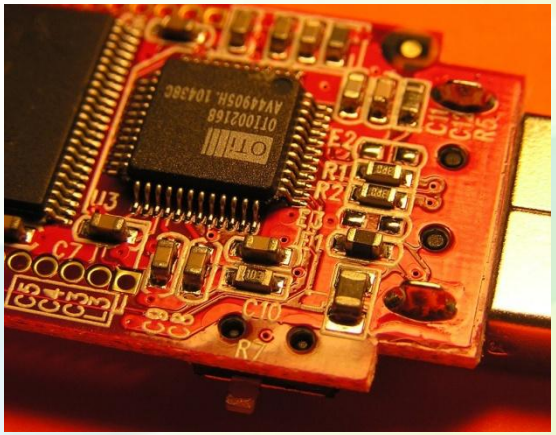
- IC package pins pass through drilled holes
  - Soldered to PCB wires that join the hole
  - Two rows 0.1 inch spacing
  - DIP 48 nos, PGA - pin grid array 400 nos

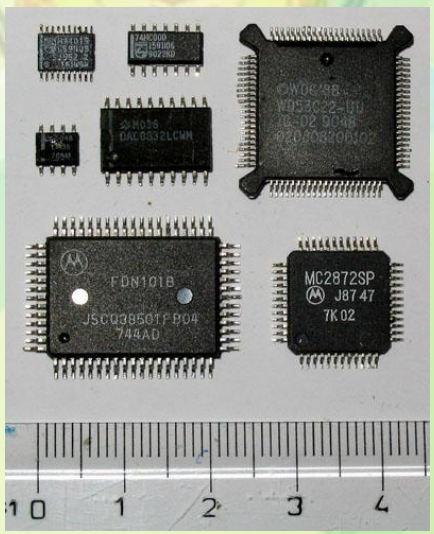


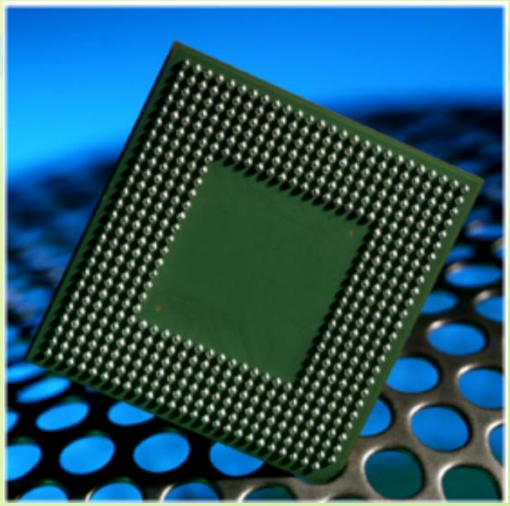


Surface Mount PCB

- IC package pins soldered to wires on PCB surface
  - Packages and PCB features are generally smaller than through-hole
  - QFP quad flat pack 0.65mm 400
  - BGA ball grid array 0.4mm 1800

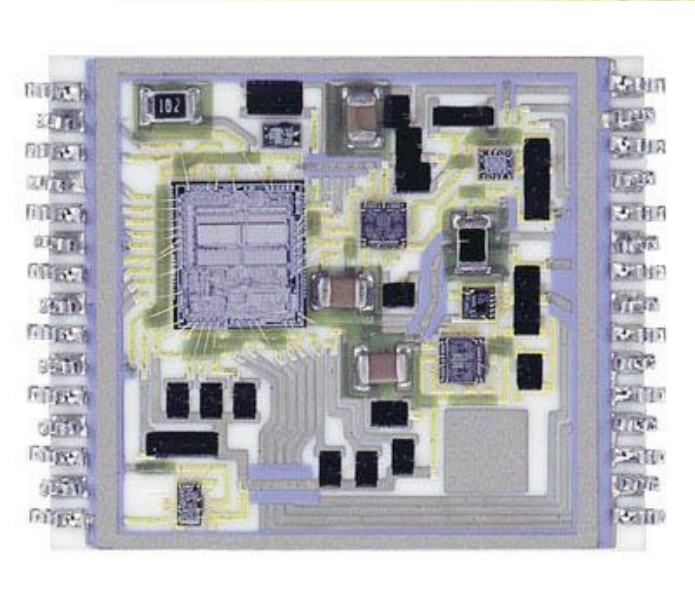






Multichip Modules (MCMs)

- Several ICs on a ceramic carrier
  - Can also include thin-film passives and discrete components
  - External connections for PCB mounting



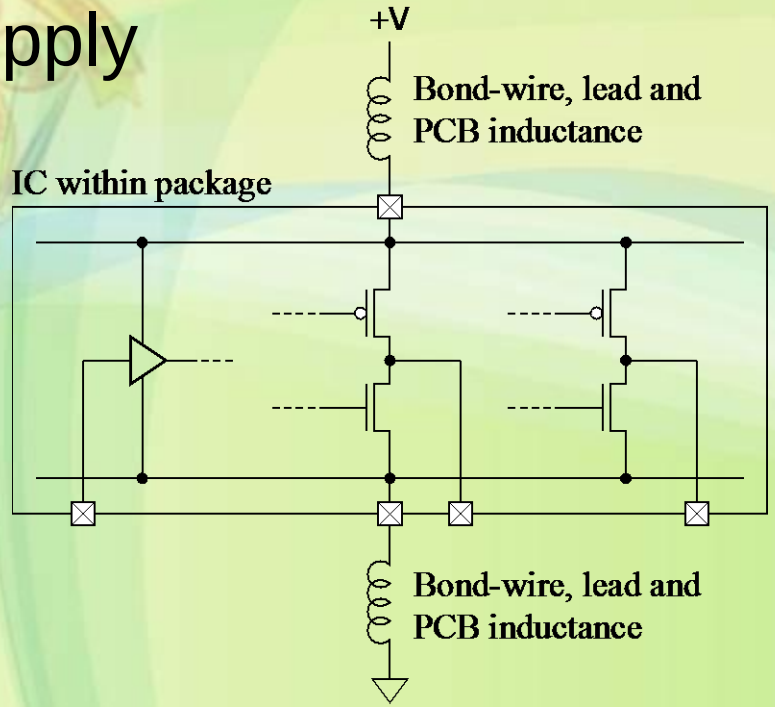
- Ideal for high-density applications
  - E.g., cell phones

Signal Integrity

- Signals propagate over bond wires, package pins, PCB traces
  - Various effects cause distortion and noise
  - Signal integrity: minimizing these effects
- Propagation delay in PCB trace
  - $\approx \frac{1}{2}c \Rightarrow \approx 150$mm/ns
- If two traces differ in length
  - Skew at arrival point can be significant
  - Careful PCB design needed

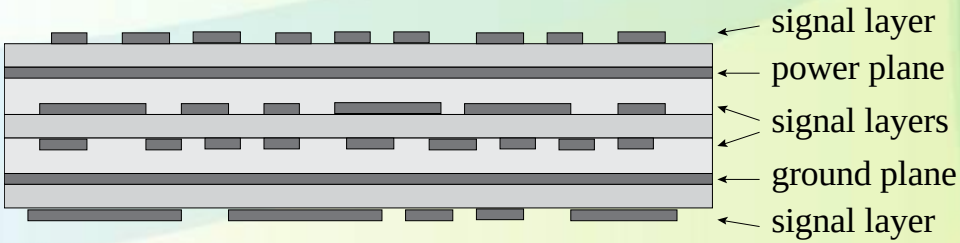
Ground Bounce

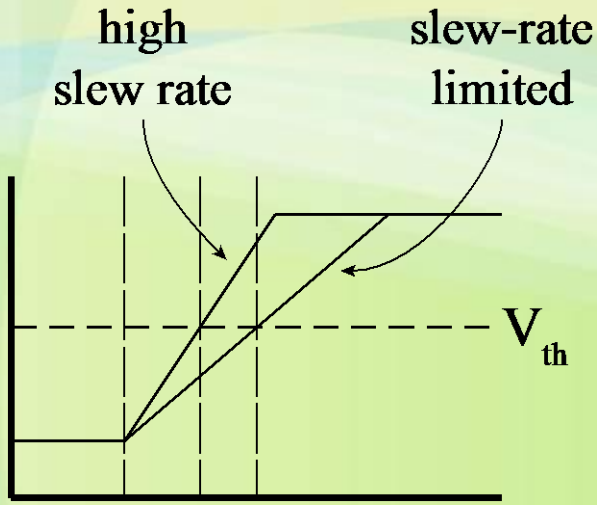
- Transient current flows when an output switches logic level
  - Parasitic inductance causes voltage shift on power supply & ground signals
  - Spikes on other drivers
  - Threshold shift on receivers



Minimizing Bounce

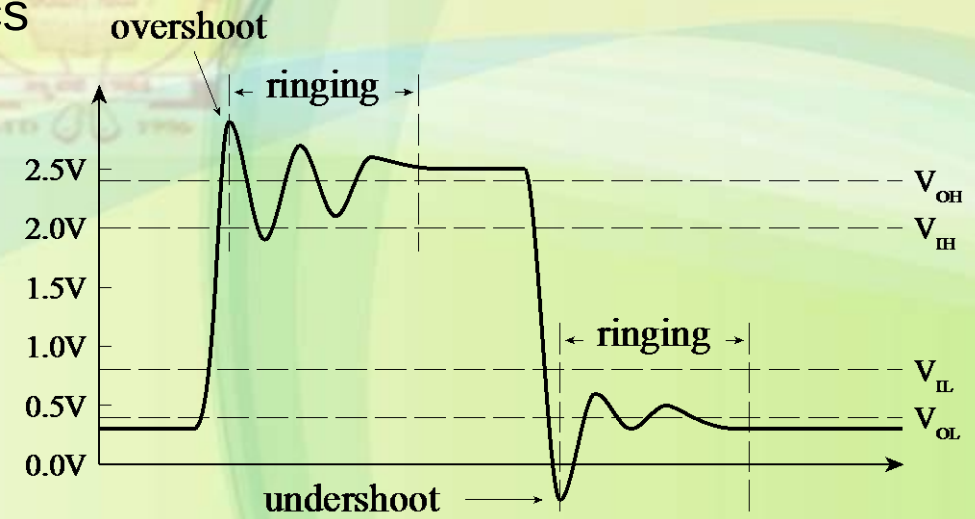
- Bypass capacitors between ground and +V
  - 0.01µF – 0.1µF, close to package pins
- Separate PCB planes for ground and +V
- Limit output slew rate
  - Trade off against propagation delay





Transmission Line Effects

- Occur when rise time is comparable to path delay
  - Reflections interfere with transitions, resulting in under/overshoot and ringing
  - Can cause false/multiple switching
  - Use PCB layout techniques to minimize effects
  - Appropriate layout termination of PCB Traces
  - Controlled characteristics impedance
  - Micro strip tr. Line
  - Modern design tools

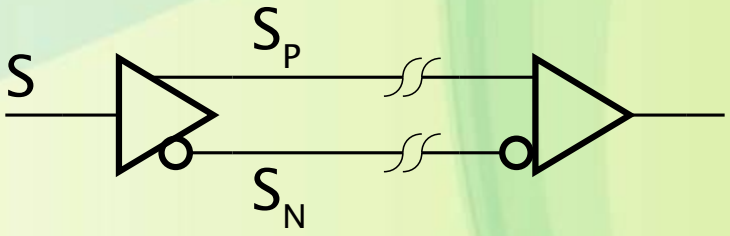


Electromagnetic Interference

- Transitions cause electromagnetic fields
  - Energy radiated from PCB traces
  - Induces noise in other systems
  - Subject to regulation
- Crosstalk
  - Radiation to other traces in the system
    - Particularly adjacent parallel traces
- PCB layout and slew-rate limiting can minimize both
- Tracs close to ground and power supply trace minimise EMI and crosstalk

Differential Signaling

- Reduces susceptibility to noise
- Transmit a signal (S_P) and negation (S_N)
  - At receiver, sense difference between them
  - $S_P - S_N$
- Noise induced on both S_P and S_N
  - $(S_P + V_{Noise}) - (S_N + V_{Noise}) = S_P - S_N$
- Cross talk effect cancelled out
- Advantages
  - Common mode noise, reduced o/p voltage swing, reduced EMI, reduced ground bounce, reduced cross talk



Summary

- Exponential improvements in IC manufacturing
- SSI and MSI TTL logic families
- ASICs: full-custom and standard cell
- PALs, CPLDs, FPGAs, platform FPGAs
- IC packages for PCB assembly
  - Through-hole and surface mount
- Signal integrity

Queries ...?