Department of Electronics & Communication Engg.

Course : ARM Microcontroller & ES-15EC62. **Sem.: 6th (2017-18)**

Course Coordinator:

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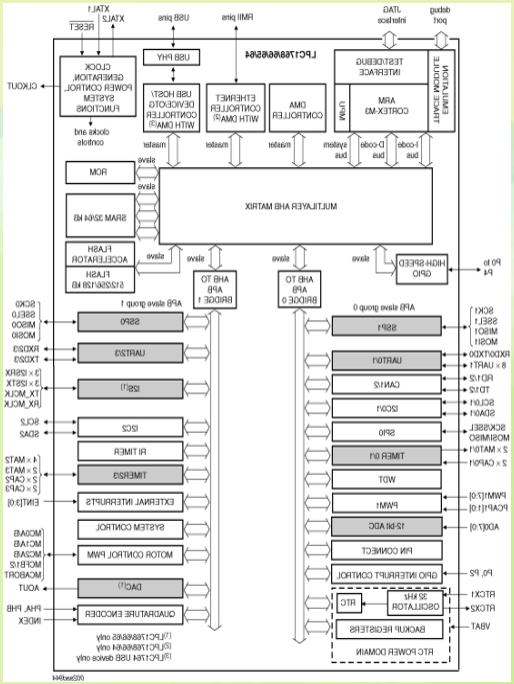
ARM Cortex-M3 Introduction

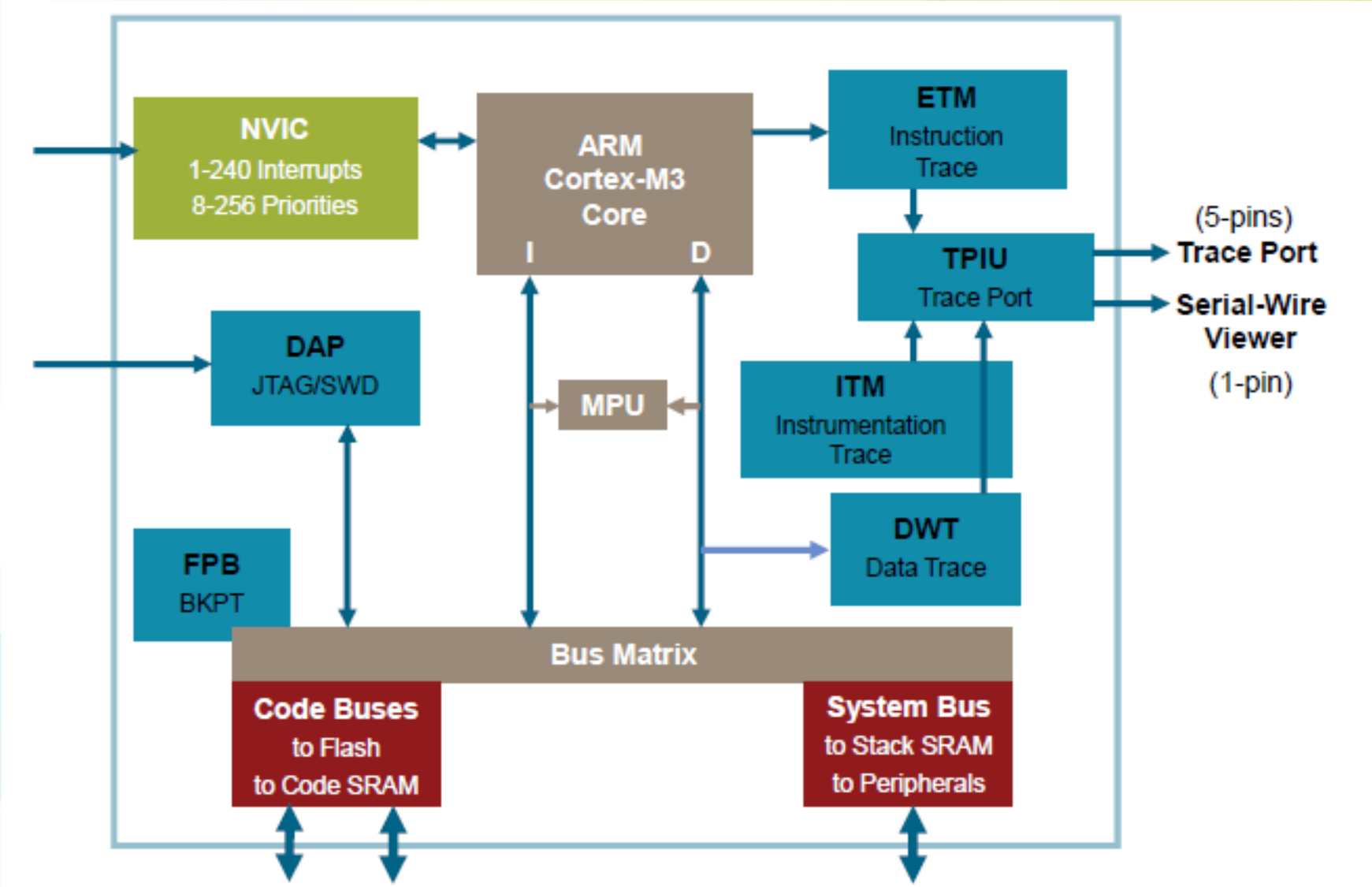
What's Happening in Microcontrollers?

Microcontrollers are getting **cheap**

- 32-bit ARM Cortex-M3 Microcontrollers@ $1
- Some microcontrollers sell for as little as $0.65
- Microcontrollers are getting **powerful**
- Lots of processing, memory, I/O in one package
- Floating-point is even available in some!
- Microcontrollers are getting **interactive**
- Internet connectivity, new sensors and actuators
- LCD and display controllers are common



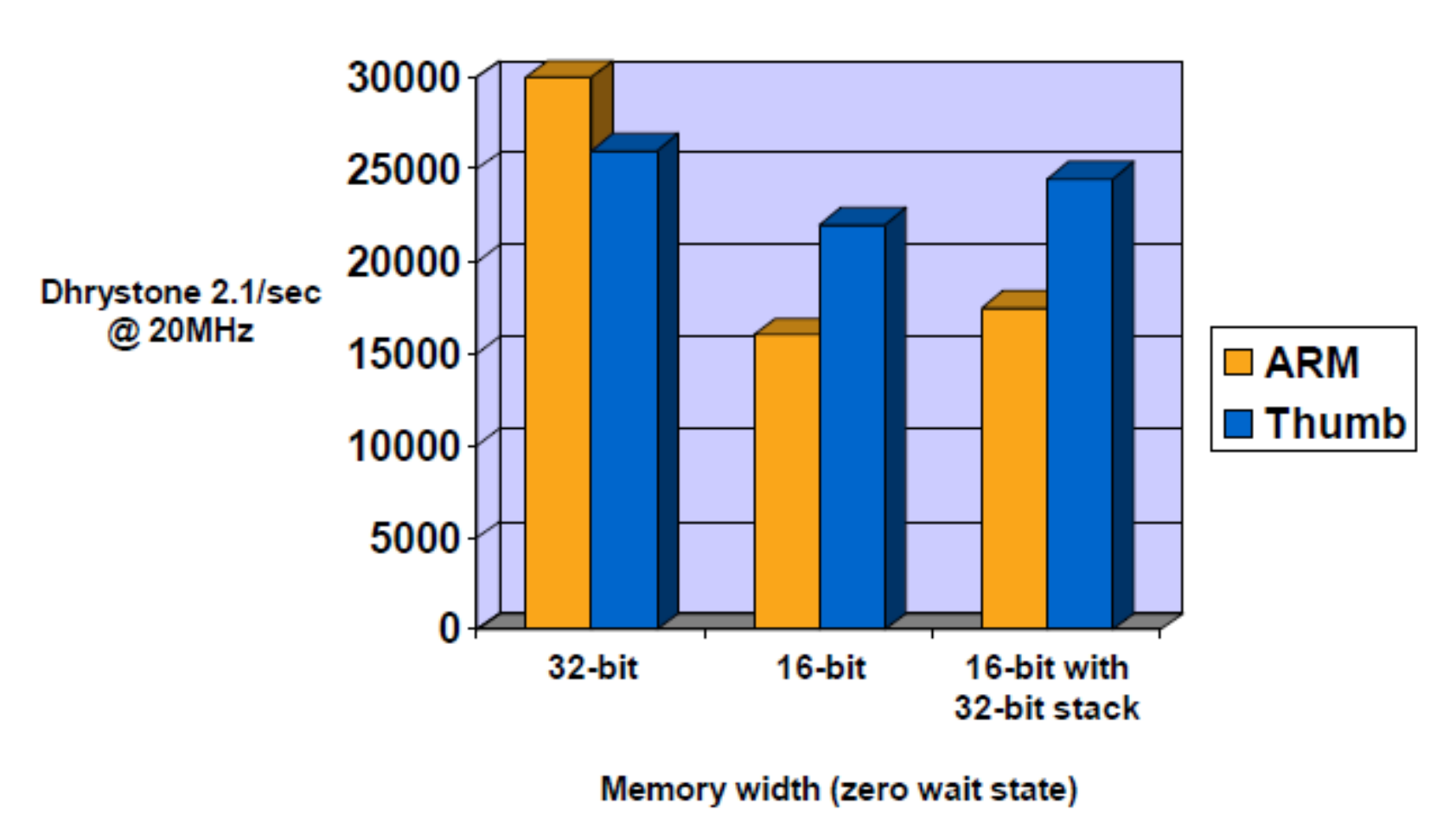
ARM Cortex-M3 Processor



ARM Cortex-M3 Microcontroller

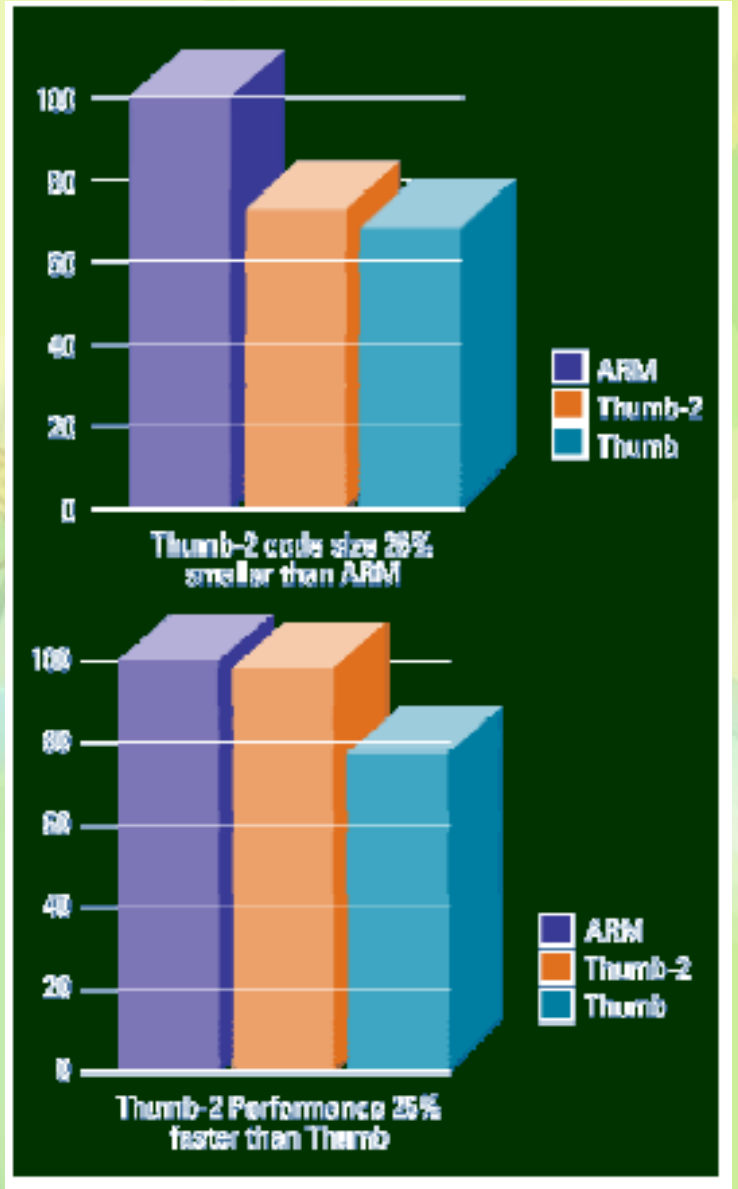
- 18 x 32-bit registers
- Excellent compiler target
- Reduced pin count requirements
- Efficient interrupt handling
- Power management
- Efficient debug and development support features
  - •Breakpoints, Watchpoints,
  - •Flash Patch support,
  - •Instruction Trace
- Strong OS support
  - •User/Supervisor model
  - •OS support features
- Designed to be fully programmed in C (even reset, interrupts and exceptions)

ARM and Thumb Performance



The Thumb-2 instruction set

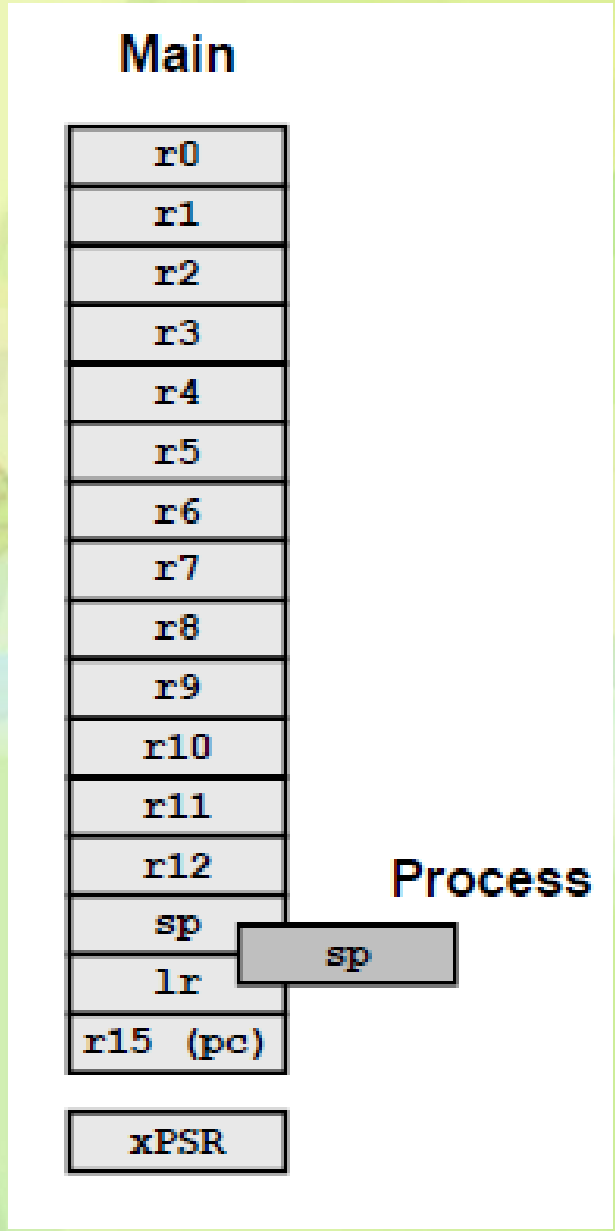
- Variable-length instructions
  - •ARM instructions are a fixed length of 32 bits
  - •Thumb instructions are a fixed length of 16 bits
  - •Thumb-2 instructions can be either 16-bit or32-bit
- Thumb-2 gives approximately 26% improvement in code density over ARM
- Thumb-2 gives approximately 25% improvement in performance over Thumb



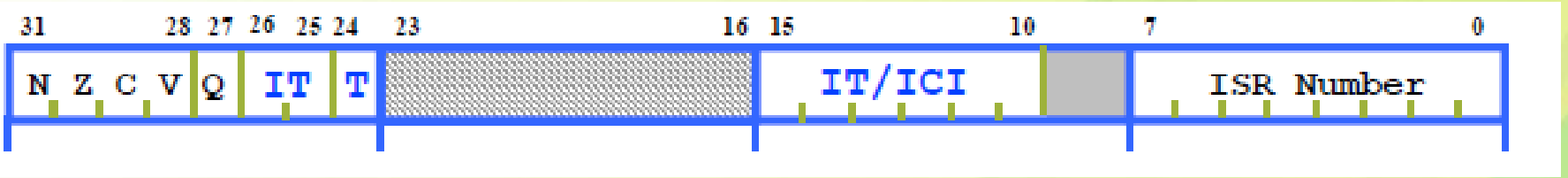
Cortex-M3 Overview

Cortex-M3 Register Set

Very compiler friendly
- Load/Store Architecture
- 32-bit registers
- Flexible register scheme
- Linear 32-bit address space

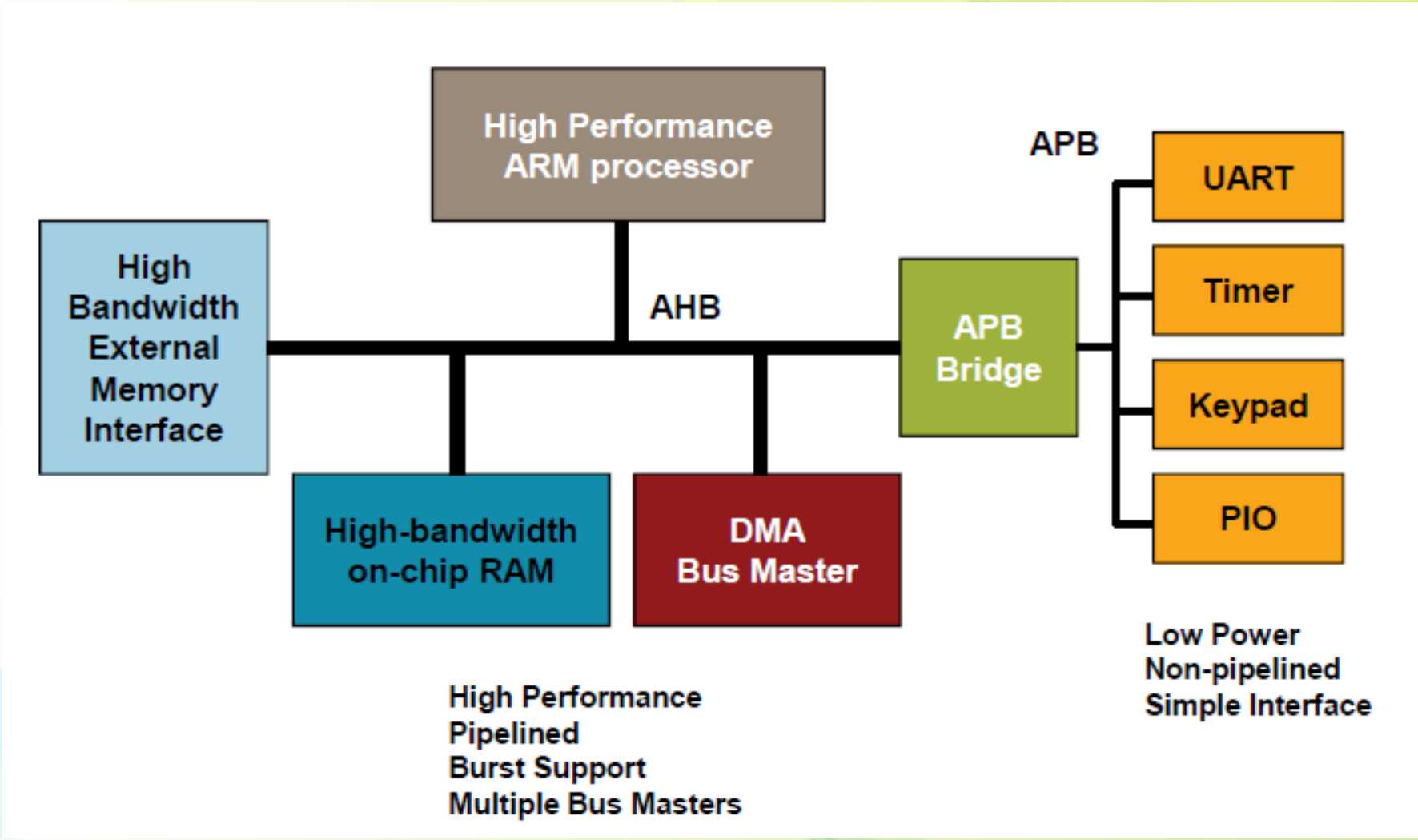


Program Status Register



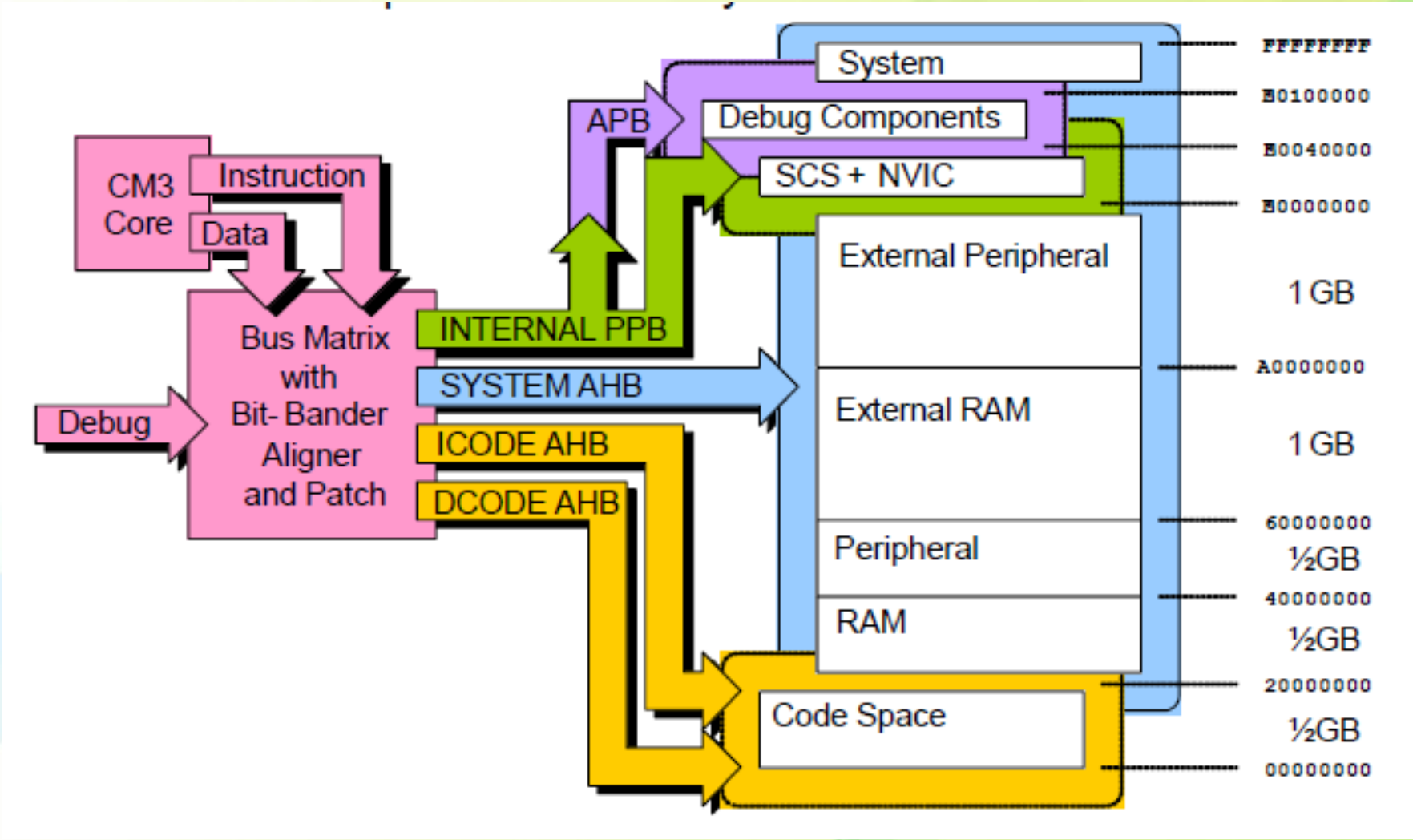
- One Status Register consisting of
  - •APSR - Application Program Status Register – ALU flags
  - •IPSR - Interrupt Program Status Register – Interrupt/Exception No.
  - •EPSR - Execution Program Status Register
  - •IT field – If/Then block information
  - •ICI field – Interruptible-Continuable Instruction information
- xPSR
  - •Composite of the 3 PSRs
  - •Stored on the stack on exception entry

An Example AMBA System

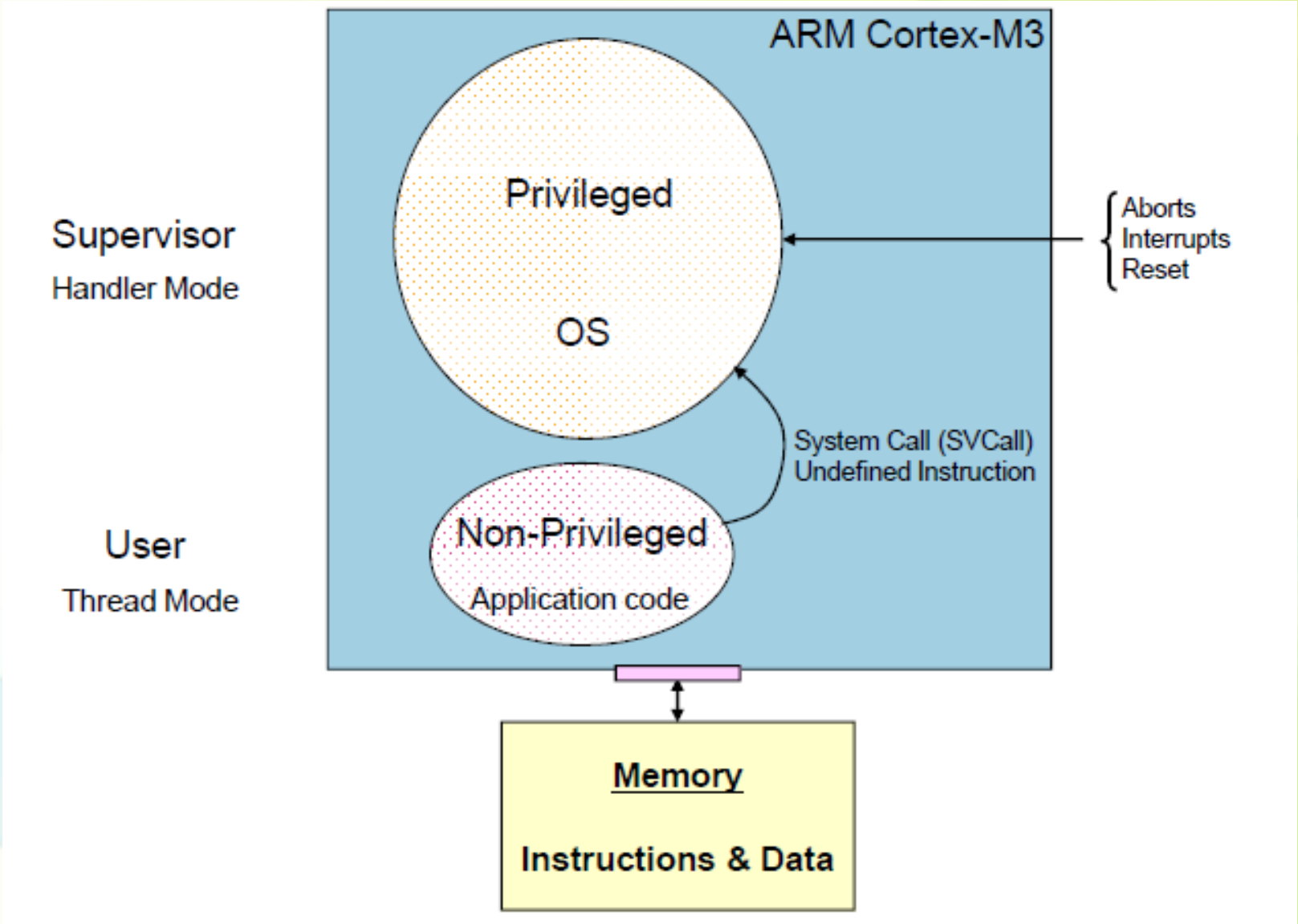


Memory Map

- Very simple linear 4GB memory map
- The Bus Matrix partitions memory access via the AHB and PPB buses



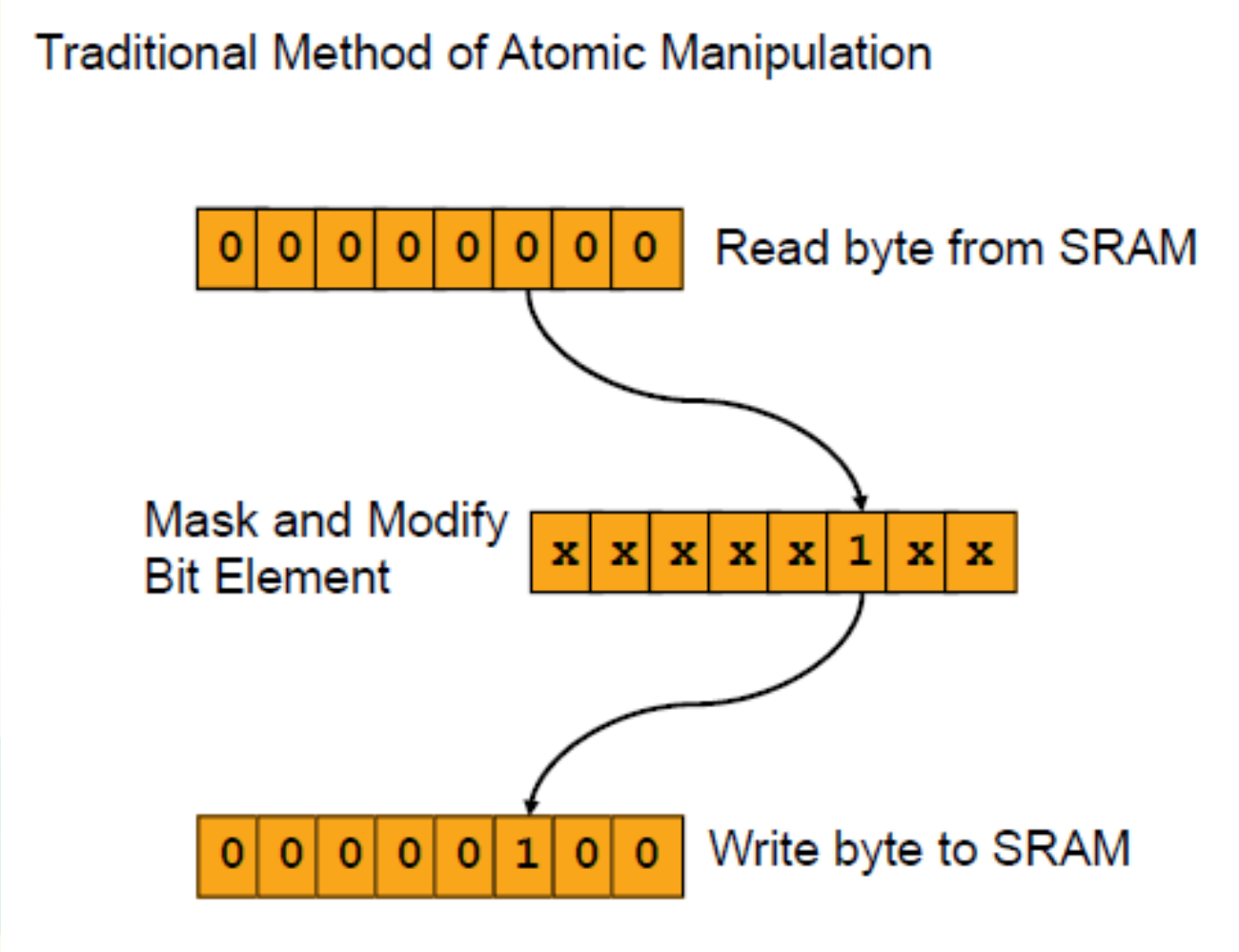
Processor Privilege



Memory Protection Unit (MPU)

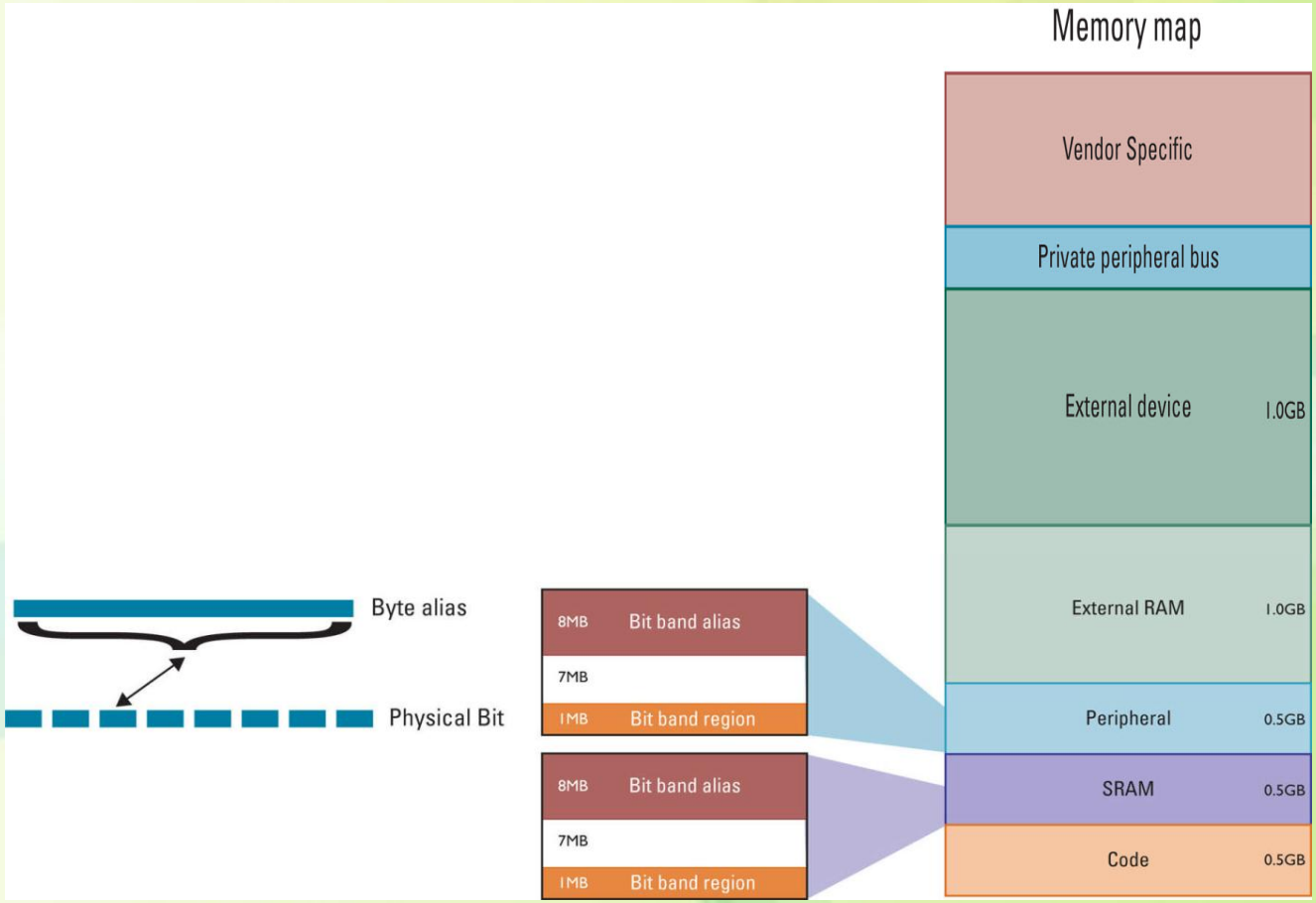
- MPU provides access control for various memory regions
- Zero Latency Memory Protection
  - 8 register-stored regions
  - Same regions used for instructions and data
  - Minimum region size 32 Bytes (max 4GB)
  - No address translation or page tables
- Configured via memory-mapped control registers

Cortex-M3 Bit Banding



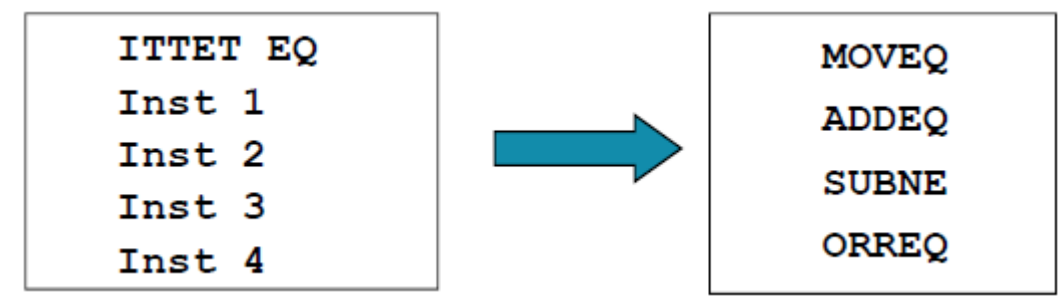
Cortex-M3 Bit Banding

- Writes to a word address in the bit band alias affect a single bit in the bit band region
- The write is translated to an atomic read-modify-write by the Cortex-M3 bus matrix
- Bit 0 of the stored register is written to the appropriate bit



Conditional Execution

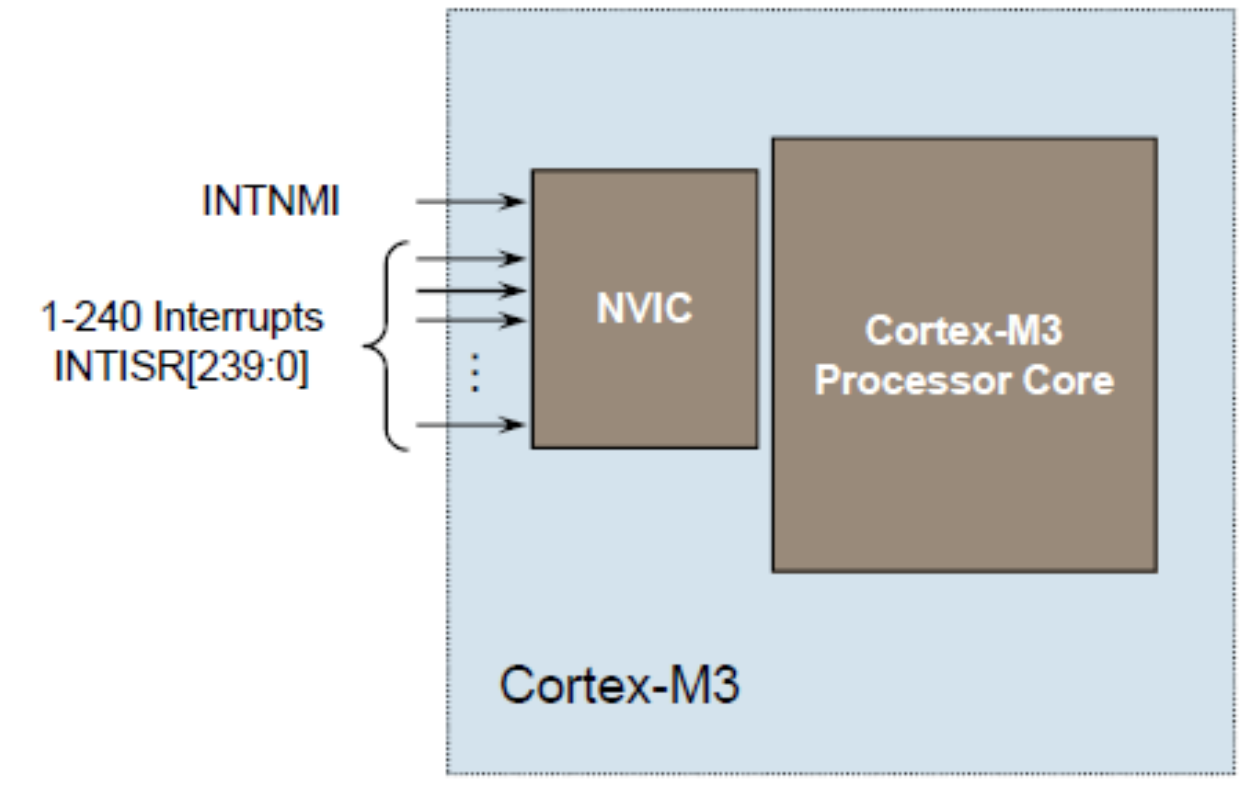
- If – Then (IT) instruction added (16 bit)
  - Up to 3 additional “then” or “else” conditions maybe specified (T or E)
  - Makes up to 4 following instructions conditional



- Any normal ARM condition code can be used
- 16-bit instructions in block do not affect condition code flags
  - Apart from comparison instruction
  - 32 bit instructions may affect flags (normal rules apply)
- Current “if-then status” stored in CPSR
  - Conditional block maybe safely interrupted and returned to
  - Must NOT branch into or out of ‘if-then’ block

Interrupt Handling

- One Non-Maskable Interrupt (INTNMI) supported
- 1-240 prioritizable interrupts supported
  - Interrupts can be masked
  - Implementation option selects number of interrupts supported
- Nested Vectored Interrupt Controller (NVIC) is tightly coupled with processor core
- Interrupt inputs are active HIGH



Exception Handling

- **Reset**
- **NMI**
- **Faults**
  - Hard Fault
  - Memory Manage
  - Bus Fault
  - Usage Fault
- **SVCall**
- **Debug Monitor**
- **PendSV**
- **SysTick Interrupt**
- **External Interrupt**

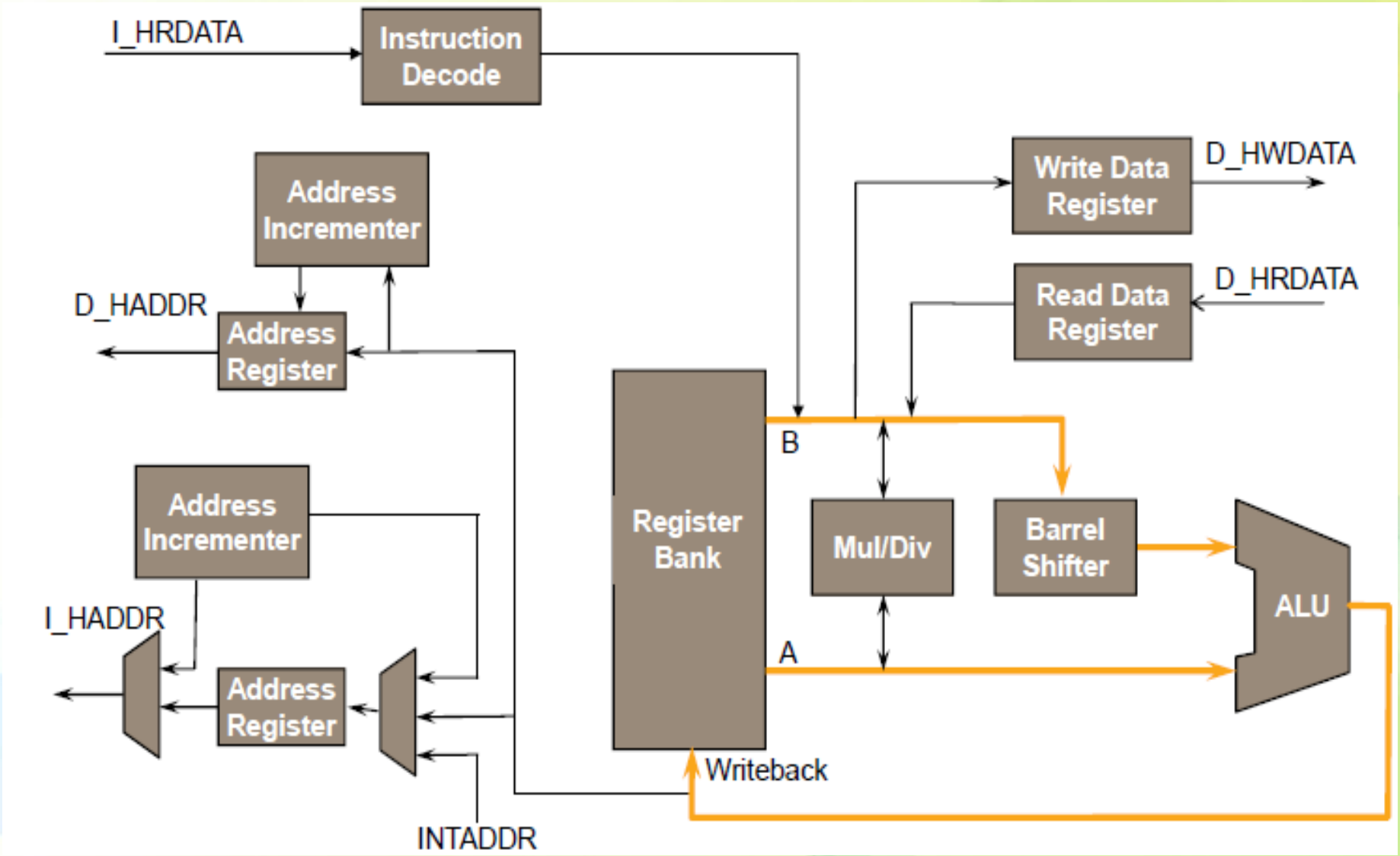
Power Management

- Multiple sleep modes supported
  - **Controlled by NVIC**
  - **Sleep Now – Wait for Interrupt/Event instructions**
  - **Sleep On Exit – Sleep immediately on return from last ISR**
  - **Deep Sleep**
    - Long duration sleep, so PLL can be stopped
    - Exports additional output signal SLEEPDEEP
- Cortex-M3 system is clock gated in all sleep modes
  - Sleep signal is exported allowing external system to be clock gated also
  - NVIC interrupt Interface stays awake
- Wake-Up Interrupt Controller (WIC)
  - External wake-up detector allows Cortex-M3 to be fully powered down
  - Effective with State-Retention / Power Gating (SRPG) methodology

Cortex-M3 Debug

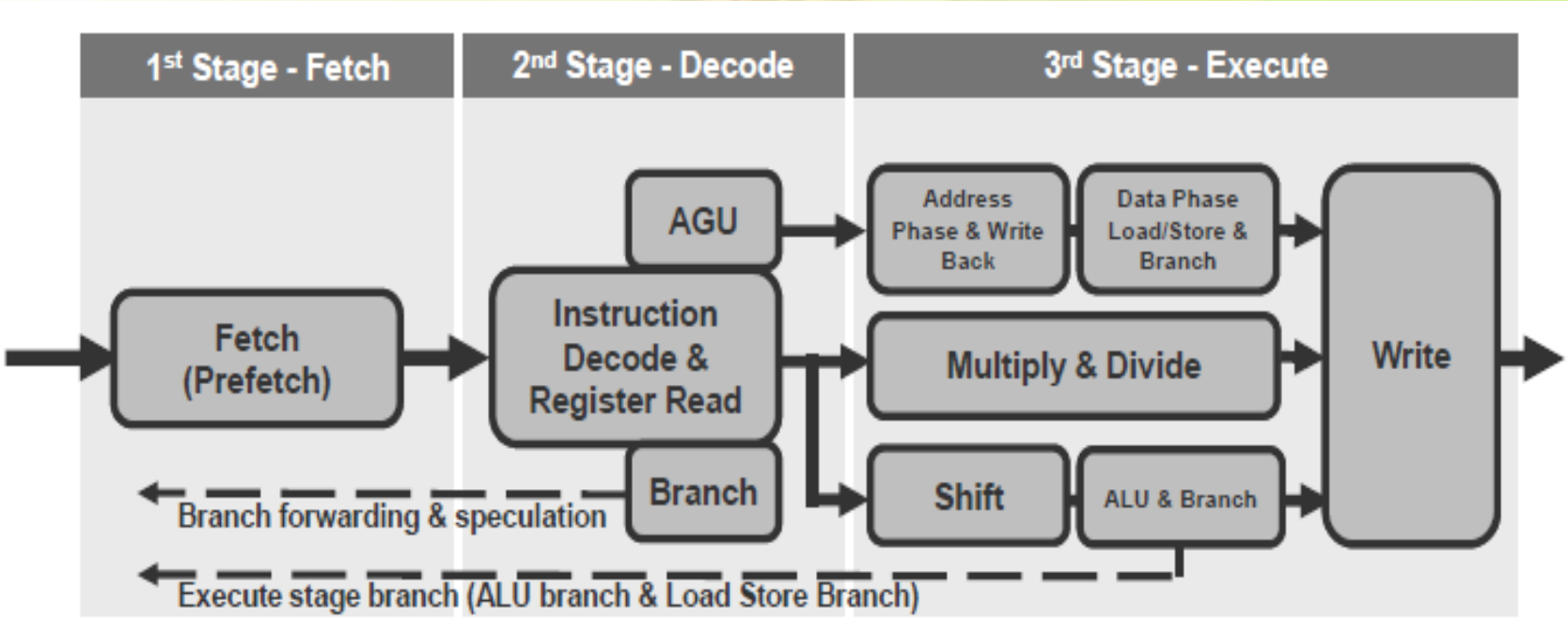
- Single stepping
- ITM (Instrumentation Trace Module)
  - Support for instrumented code
  - Like “printf” debugging, but single cycle writes to ITM module can be exported via serial interface
- Optional ETM (Embedded Trace Module) which provides instruction trace
- Access to all memory and registers via Debug Access Port (DAP)
- Profiling Support
  - Helps you optimize your code
  - A hardware triggered PC-sampler is provided by the Cortex-M3 core
- Flash patch / Breakpoints
  - 6 instruction comparators, ARMv5T BKPT instruction is supported
  - 2 literal comparators
  - Allows flash code to be remapped into SRAM or system address space
- Data Watch point and Trace (DWT) that implements 4 h/w watch points

Cortex-M3 Datapath

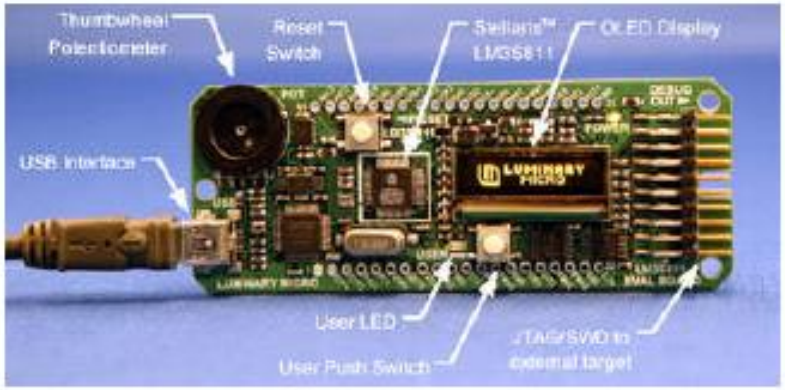


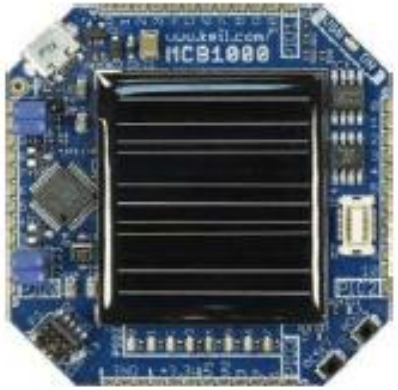
Cortex-M3 Pipeline

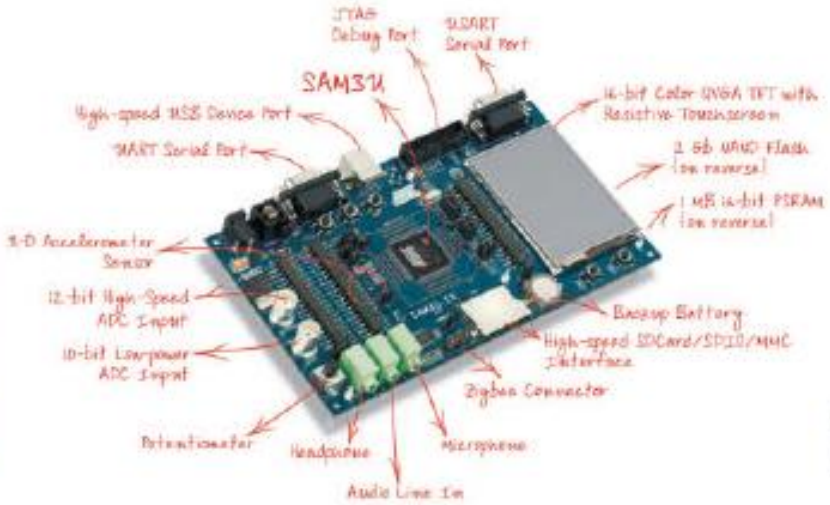
- Cortex-M3 has 3-stage fetch-decode-execute pipeline
  - Similar to ARM7
  - Cortex-M3 does more in each stage to increase overall performance



Cortex-M3 Development Platforms







Rapid Prototyping

- **Rapid Prototyping helps industries create new products**
  - Control, communication and interaction increasingly define products
  - Development cycles for microelectronics have not kept pace

3D Moulding

3D Printing

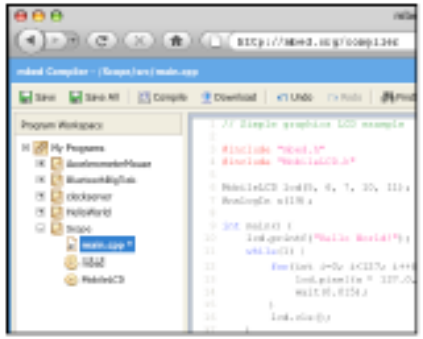
2D/3D Design

Web Frameworks

mbed

Getting Started and Rapid Prototyping with ARM MCUs Complete Targeted Hardware, Software and Web 2.0 Platform

Dedicated Developer Web Platform



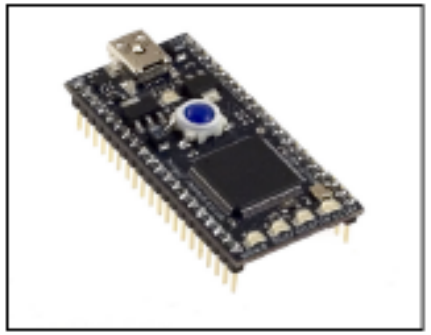
Lightweight Online Compiler

High-level Peripheral APIs

mbed

http://mbed.org

Rapid Prototyping for Microcontrollers



Cortex-M3 MCU in a Prototyping Form-Factor

Queries ...?