



S J P N Trust's

Hirasugar Institute of Technology, Nidasoshi.*Inculcating Values, Promoting Prosperity*

Approved by AICTE, Recognized by Govt. of Karnataka and Affiliated to VTU Belagavi.

Dept.

Exam.

Internal Assessment

Even Sem(2017-18)

FIRST INTERNAL ASSESSMENT

Sem: 6

Date: 05.03.18

Sub: ARM Microcontroller & ES

Time: 3pm to 4pm

Sub. Code:15EC62

Max. Marks: 25

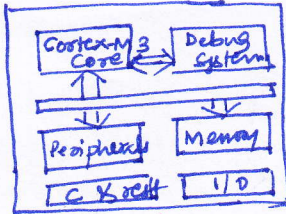
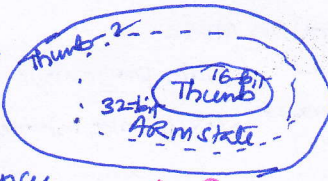
Note: Answer two full questions, draw sketches wherever necessary.

Q. No		Description of Question	Marks	CO	RBT Level
1	a	With neat block diagram, explain briefly ARM Cortex-M3 based MCU.	7	CO310.1	L1 L2
	b	Briefly explain Thumb2 technology.	6	CO310.1	L1 L2
OR					
2	a	List the ARM Cortex-M3 processor application.	6	CO310.1	L1 L2
	b	With neat block diagram, explain ARM Cortex-M3 registers.	7	CO310.1	L1 L2
3	a	Explain operation modes of ARM Cortex-M3 with operation mode transitions.	6	CO310.1	L1 L2
	b	Describe the ARM Cortex-M3 memory mapping.	6	CO310.1	L1 L2
OR					
4	a	List the characteristics of ARM Cortex-M3.	6	CO310.1	L1 L2
	b	Draw the register format of xPSR & explain.	6	CO310.1	L1 L2


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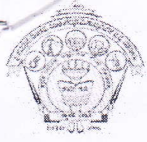
SCHEME OF EVALUATION

Sem : 6		Subject : ARM Microcontroller & ES	Sub Code : 15EC62	Date : 05/03/18		
Q. No.	Bit	Description	Marks	CO's	RBT LEVEL	
1.	a.	 <ul style="list-style-type: none"> Cortex M3 processor based MC can easily programmed using C Support ARM thumb-2-Technology 32-bit data path, Reg. bank, memory interface Harvard Architecture. <p style="text-align: center;">L-4 L-3</p>	7	CO310-1	L1 L2	
	b.	<p>Thumb-2 Technology ISA:</p> <ul style="list-style-type: none"> Cortex-M3 support the thumb-2 ISA It allows 32-bit & 16-bit instruction to be used together for high code density & high performance efficiency. In previous processors ^(CPU) had two operation states 32-bit ARM state & 16-bit thumb state. But thumb-2 had adv. over to additional. <ul style="list-style-type: none"> No state switching overhead - No need to separate files of ARM state & thumb state - Powerful instructions  <p style="text-align: center;">L-2</p>	6	310-1	L1 L2	
2.	a.	<p>List of CORTEX-M3 applications:</p> <ul style="list-style-type: none"> Low cost MC applications like toys. Automotive industry Data Communications Industry control Consumer products. <p style="text-align: center;">L-6</p>	6	310-1	L1 L2	
	b.	<p>Registers:</p> <p>R₀ R₁ R₂ R₃ . . R₁₂</p> <p>R₁₃ (MSP) R₁₃ (PSP) R₁₄ LR R₁₅ PC</p> <p style="text-align: center;">L-4</p> <ul style="list-style-type: none"> R₀ to R₁₂ are all General purpose registers. R₀-R₇ Low Reg. R₈-R₁₅ High Reg. <p style="text-align: center;">L-3</p> <p>MSP - Main stack pointer PSP - Process " LR - Link register PC - Program counter.</p>	7	310-1	L1 L2	



SCHEME OF EVALUATION

Sem : 6		Subject : ARM MC BES	Sub Code : 15EC62	Date : 05/03/18																																					
Q. No.	Bit	Description	Marks	CO's	RBT LEVEL																																				
3.	a.	<p>CORTEX M3 operation Modes:</p> <p>operation Mode 1. thread (Main program) 2. Handler (exception or Interrupt)</p> <p>PRIVILEGE LEVEL 1. Privileged 2. User</p> <p>mechanism to safe guard memory & basic security model.</p>	6	310.1	L1 L2																																				
	b.	<p>Memory MAP: 4 GB memory space. can be divided into ranges.</p> <table border="1"> <tr> <td>FF----</td> <td>System level</td> <td>← NVIC, MPU control seg to debug components.</td> </tr> <tr> <td>E0----</td> <td>External device</td> <td></td> </tr> <tr> <td>DF----</td> <td>External RAM</td> <td></td> </tr> <tr> <td>A0----</td> <td>External RAM</td> <td></td> </tr> <tr> <td>9F----</td> <td>External RAM</td> <td></td> </tr> <tr> <td>60----</td> <td>Peripherals</td> <td>Exp 2</td> </tr> <tr> <td>5F----</td> <td>Peripherals</td> <td></td> </tr> <tr> <td>40----</td> <td>SRAM</td> <td>← static RAM</td> </tr> <tr> <td>3F----</td> <td>SRAM</td> <td></td> </tr> <tr> <td>20----</td> <td>CODE</td> <td>← Program code</td> </tr> <tr> <td>1FFFFFFF</td> <td>CODE</td> <td></td> </tr> <tr> <td>0X00000000</td> <td>CODE</td> <td></td> </tr> </table>	FF----	System level	← NVIC, MPU control seg to debug components.	E0----	External device		DF----	External RAM		A0----	External RAM		9F----	External RAM		60----	Peripherals	Exp 2	5F----	Peripherals		40----	SRAM	← static RAM	3F----	SRAM		20----	CODE	← Program code	1FFFFFFF	CODE		0X00000000	CODE		6	310.1	L1 L2
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4.	a.	<p>Characteristics:</p> <ul style="list-style-type: none"> - High performance - Low power consumption - Debug supports. - Advanced Interrupt Handling feature - System Features 	6	310.1	L1 L2																																				
	b.	<p>xPSR</p> <p>31 30 29 28 27 26:25 24 23:20 19:16 15:10 9 8:0 N Z C V Q IC/IT T IC/IT Exception number</p> <p>PSR → APSR Application IPSR Interrupt EPSR Exception</p>	6	310.1	L1 L2																																				



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Internal Assessment

Even Sem(2017-18)

SECOND INTERNAL ASSESSMENTSem: 6
Date: 11.04.18Sub: ARM Microcontroller & ES
Time: 3pm to 4pmSub. Code:15EC62
Max. Marks: 25*Note: Answer two full questions, draw sketches wherever necessary.*

Q. No		Description of Question	Marks	CO	RBT Level
1	a	Explain the following instructions with example ASR, LSL, ROR & REV.	7	CO310.2	L1 L2 L3
	b	Write the memory map of Cortex M3 and Explain briefl bit-band operations.	6	CO310.2	L1 L2 L3
OR					
2	a	Explain the following 16-bit instructions in Cortex M3 ADC, LDR, PUSH, AND, MRS & MSR.	6	CO310.2	L1 L2 L3
	b	With neat block diagram, explain the organization of CMSIS.	7	CO310.2	L1 L2 L3
3	a	Explain the 6 purposes of Embedded systems with an example for each.	6	CO310.3	L1 L2 L3
	b	Mention the applications of Embedded systems with an example for each .	6	CO310.3	L1 L2 L3
OR					
4	a	Explain the components of typical Embedded systems in details.	6	CO310.3	L1 L2 L3
	b	Differentiate between General computing systems and Embedded systems.	6	CO310.3	L1 L2 L3


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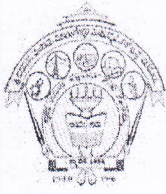
SCHEME OF EVALUATION

Q. No.	Bit	Description	Marks	CO's	RBT LEVEL
Sem : 6 Subject : ARM Microcontroller & ES Sub Code : ISEC62 Date : 11/04/18					
1	a.	ASR (Arithmetic shift Right) LSL (Logical shift left) ROR (Rotate Right) REV (Reverse byte inward) Example to each.	7	310.2	L1 L2 L3
1	b.	<p style="text-align: center;">@ Memory map.</p> <p style="text-align: center;">⑤ Bit Access to bit-band region via the bit-band alias</p>	6	310.2	L1 L2 L3
2	a.	ADC - ADD with carry, ADC R0, Rn, Rm; R0 = Rn + Rm + carry LDR - Load word from memory to reg, LDR R0, [Rn, #offset] PUSH - Push multiple reg., PUSH R1, R3, R5. AND - logical AND, AND R3, R7, R8 MRS - Move Reg. to special Reg., MRS R0, APSR MSR - Move Special Reg. to Reg., MSR APSR, R0	6	310.2	L1 L2 L3

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SCHEME OF EVALUATION

Sem : 6		Subject : ARM Microcontroller & ES	Sub Code : ISEC62	Date : 11/04/18		
Q. No.	Bit	Description		Marks	CO's	RBT LEVEL
2	b.	<p>User</p> <p>RTOS</p> <p>CMSIS</p> <p>MCU</p> <p>Explanation L3</p>		7	310.2	4L2L3
3	a.	<p><u>6 Purposes of ES:</u></p> <ol style="list-style-type: none"> 1. Data collection/storage/Representation : Digital camera. 2. Data communication : Wireless Network router 3. Data (signal) processing : Digital hearing Aid 4. Monitoring : Patient monitoring system 5. Control : Air conditioner for controlling room Temp. 6. Application specific user interface : Mobile, Running shoe. <p>L1 each.</p>		6	310.3	4L2L3
3	b.	<p><u>Applications of ES:</u></p> <ol style="list-style-type: none"> 1. Consumer electronics : Camcorders, Camera. 2. Household appliances : TV, DVD, washing machine 3. Home automation & security : Air Conditioner, CCTV 4. Automotive industry : ABS, Engine control 5. Telecom : cellular phones, handsets 6. Computer peripherals : Printers, Scanners, fax machines 7. Computer networking systems : switches, Hub, Router, firewall 8. Health care : ECG, EEG, 9. Measurement & instrumentation : CRO, PLC, Digital multimeter 10. Banking retail : ATM, POS 11. Card Readers : Barcode, smart card readers, <p>L1 each.</p>		6	310.3	4L2L3



SCHEME OF EVALUATION

Sem : 6		Subject : ARM Microcontroller & ES	Sub Code : ISEC62	Date : 11/04/18				
Q. No.	Bit	Description	Marks	CO's	RBT LEVEL			
4	a.	<p><u>Components of ES:</u></p> <p>Explanation ③</p>	6	300.3	L1L2L3			
4	b.	<table border="0"> <tr> <td style="vertical-align: top;"> <p><u>General computing system</u></p> <ol style="list-style-type: none"> System is combination of generic HW + general purpose OS for exe of variety of app General OS Applications are not ^{not} alterable & OS can be re installed processing speed is key factor in selection of system Non-time critical need not to be deterministic for the exe of behaviour Power saves </td> <td style="vertical-align: top;"> <p><u>Embedded systems.</u></p> <ol style="list-style-type: none"> system is combination of specific S/W + Embedded OS for exe of the set of application May of ^{not} contain Embedded OS A firmware of ES is to be pre programmed & non alterable Application specific critical need to be deterministic for the exe of behaviour more power saves <p style="color:red">① Deach.</p> </td> </tr> </table>	<p><u>General computing system</u></p> <ol style="list-style-type: none"> System is combination of generic HW + general purpose OS for exe of variety of app General OS Applications are not ^{not} alterable & OS can be re installed processing speed is key factor in selection of system Non-time critical need not to be deterministic for the exe of behaviour Power saves 	<p><u>Embedded systems.</u></p> <ol style="list-style-type: none"> system is combination of specific S/W + Embedded OS for exe of the set of application May of ^{not} contain Embedded OS A firmware of ES is to be pre programmed & non alterable Application specific critical need to be deterministic for the exe of behaviour more power saves <p style="color:red">① Deach.</p>	6	310.3	L1L2L3	
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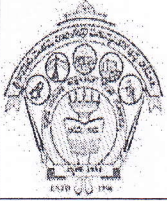
Internal Assessment

Even Sem(2017-18)

THIRD INTERNAL ASSESSMENTSem: 6
Date: 18.05.18Sub: ARM Microcontroller & ES
Time: 3pm to 4pmSub. Code:15EC62
Max. Marks: 25*Note: Answer two full questions, draw sketches wherever necessary.*

Q. No		Description of Question	Marks	CO	RBT Level
1	a	Explain the different characteristics of Embedded system in detail.	7	CO310.4	L1 L2 L3
	b	What is operational quality attribute? Explain the important operational quality attribute to be considered in any Embedded system design.	6	CO310.4	L1 L2 L3
OR					
2	a	Explain the important non-operational quality attribute.	7	CO310.4	L1 L2 L3
	b	With block diagram, mention the components used in the design of a washing machine and also explain its working.	6	CO310.4	L1 L2 L3
3	a	Briefly explain the functions of the operating system, with a diagram.	6	CO310.5	L1 L2 L3
	b	Explain the multiprocessing, multitasking and multiprogramming.	6	CO310.5	L1 L2 L3
OR					
4	a	What is RTOS? How to choose an RTOS.	6	CO310.5	L1 L2 L3
	b	Differentiate between Thread and Process.	6	CO310.5	L1 L2 L3


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Scheme


Even Sem
(2017-18)

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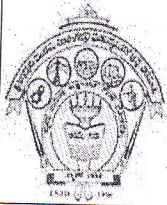
SCHEME OF EVALUATION IA-III

Sem : 6		Subject : ARM MC 95 ES	Sub Code : EC62	Date : 18/05/2018		
Q. No.	Bit	Description	Marks	CO's	RBT LEVEL	
1	a)	<p>Characteristics of an Embedded Systems:</p> <ol style="list-style-type: none"> 1. Application & Domain specific. Ex. cannot replace CPU of Microwave oven with Discondition. 2. Reactive and Real time: Ex. ABS 3. Operates in Harsh Environment. Ex. High shock, Power fluctuations, corrosion, aging 4. Distributed: Ex. Vending Machine, ATM 5. Small size and weight: Ex. product aesthetics (size, weight, shape, style etc) 6. Power Concerns: Ex. Power saving modes. 	[7]	310.4	L1 L2 L3	
	b)	<p>Operational Quality attributes:</p> <ol style="list-style-type: none"> 1. Response: Response is a measure of quickness of the system. 2. Throughput: deals with efficiency of the system. 3. Reliability: is a measure of how much % you can rely upon the proper functioning of the system. 4. Maintainability: deals with support & maintenance 5. Security: 6. Safety: deals with the possible damage. 	[6]	310.4	L1 L2 L3	
2.	a)	<p>Non-operational Quality attributes:</p> <ol style="list-style-type: none"> 1. Testability & Debug-ability: deals with how easily one can test his/her design, application and by which means he/she can test it. 2. Evolvability: embedded product can be modified to take advantage of new firmware or hardware technologies. 3. Portability: is a measure of 'system independence' 4. Time-to-prototype and market: is the time elapsed between the conceptualisation of the product and the time at which the product is ready for selling. 5. Per unit Cost and Revenue: 	[7]	310.4	L1 L2 L3	
	b)	<p>Washing machine - Application specific ES:</p> <p>An ES contains sensors, actuators, control unit and application specific user interface like keyboards, display unit etc.</p>	[6]	310.4	L1 L2 L3	


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SCHEME OF EVALUATION IA-

Sem : 6		Subject : ARM MC & FS		Sub Code : EC62	Date : 18/05/2018	Marks	CO's	RBT LEVEL
Q. No.	Bit	Description						
3.	a)				[6]	310.5	L1 L2 L3	
		<p>expln.</p> <p>b) → The ability of the operating system to have multiple programs in memory, which are ready for execution, is referred as <u>multi-programming</u></p> <p>→ The ability of an operating system to hold multiple processes in memory and switch the processors (CPU) from executing one process to another process is known as <u>multitasking</u>.</p> <p>→ <u>Multi processing</u> describes the ability to execute multiple processes simultaneously.</p>						

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Scheme

Even Sem
(2017-18)

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SCHEME OF EVALUATION IA-

Sem : 6		Subject : ARM MC K ES	Sub Code : ISEC 62	Date : 18/05/2018				
Q. No.	Bit	Description	Marks	CO's	RBT LEVEL			
4.	a)	<p>A Real-Time Operating System (RTOS) is an operating system (OS) intended to serve real-time applications that process data as it comes in, typically without buffer delays. Processing time requirements (including any OS delay) are measured in tenths of seconds or shorter increments of time.</p> <p>Functional Requirements: Non Functional reqt:</p> <ul style="list-style-type: none"> • Processor support • Memory requirements • Real-time Capabilities • Kernel and interrupt latency • Inter process communication and Task Synchronization • Modularisation Support • Support for Networking & Communication • Development lang. Support. 	[6]	310.5	L1 L2 L3			
	b)	<table border="0"> <tr> <td style="vertical-align: top;"> <p><u>Thread</u></p> <ul style="list-style-type: none"> • Thread is also called light weight process. • OS is not required for thread switching • One-thread can read, write or even completely clean another thread stack • All threads can share same set of open files & child processes. • Uses fewer resources </td> <td style="vertical-align: top;"> <p><u>Process</u></p> <ul style="list-style-type: none"> • Process is also called heavy weight process. • OS interface is required for process switching • Each process operates independently of the other process. • In multiple processing, each process executes the same code but has its own memory and file resources • Use more resources. </td> </tr> </table>	<p><u>Thread</u></p> <ul style="list-style-type: none"> • Thread is also called light weight process. • OS is not required for thread switching • One-thread can read, write or even completely clean another thread stack • All threads can share same set of open files & child processes. • Uses fewer resources 	<p><u>Process</u></p> <ul style="list-style-type: none"> • Process is also called heavy weight process. • OS interface is required for process switching • Each process operates independently of the other process. • In multiple processing, each process executes the same code but has its own memory and file resources • Use more resources. 	[6]	310.5	L1 L2 L3	
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