FIRST INTERNAL ASSESSMENT

Sem: 5 **Sub: Verilog HDL** **Sub. Code: 15EC53**
Date: 11.09.2018 **Time: 11am to 12pm** **Max. Marks: 25**

Note: Answer two full questions, draw sketches wherever necessary.

Q. No		Description of Question	Marks	CO	RBT LEVEL
1	a	With diagram, explain typical design flow.	6	CO303.1	L1L2L3
	b	Explain the structure of Verilog module.	7	CO303.1	L1L2L3
		OR			
2	a	List the useful features of Verilog HDL.	6	CO303.1	L1L2L3
	b	Name the different types of operators in Verilog. Explain the Logical. operators.	7	CO303.2	L1L2L3
3	a	Explain the two basic types of design methodology with diagram.	6	CO303.2	L1L2L3
	b	Write Verilog code for 4-bit ripple carry counter.	6	CO303.3	L1L2L3
		OR			
4	a	Write diagram of a 4-bit ripple carry adder and Boolean functions in Verilog. Draw the simulation waveform.	6	CO303.3	L1L2L3
	b	Write an Verilog code in data flow description for a 2-bit magnitude comparator with the help of truth table & simplified	6	CO303.3	L1L2L3

Course Coordinator **Module Coordinator** **HOD**

Prof. S S Patil **Prof. N M Patel** **Dr. V G Kasabegoudar**

IA - I SCHEME OF EVALUATION

15EC53

Sem : 5 | Subject : Verilog HDL | Sub Code : | Date : 14/09/2018

Q. No.	Bit	Description	Marks	CO's	RBT LEVEL
1.	a.	Design Specification Behavioural Description RTL Description (HDL) Functional Verification & Testing Logical Synthesis / Timing Verification Gate level Net list Logical Verification & Testing Flooring planning Automatic place & Route Physical Layout Layout verification Implementation (5) + Explanation (2)	7	303.1	L1 L2 L3

	b.	Explanation + Ex: (4)
		module HA (A, B, S, C);
		input A, B;
		output S, C;
		assign S = A ^ B;
		assign C = A & B;
		endmodule (2)
			6	303.1	L1 L2 L3

2.	a.	Features of Verilog: - Easy to learn & easy to use. - Different levels of abstraction to be mixed in the same model. - Most popular logic synthesis tools support verilog HDL - All fabrication Vendors provide verilog HDL libraries for post logic synthesis simulation. - Programming language interface (PLI) is a powerful feature that allows the user to write custom 'C' code to interact with the internal data structures of Verilog.	7	303.1	L1 L2 L3
	b.	Operators are classified as: (4) - Logical - Relational - Arithmatic - shift (2) Logical → (Binary) Bitwise: &, |, ~(&), ~(|), ~(^); Boolean: &&, ||; (Unary) Reduction: &, |, ~, ~(&), ~(|), ~(^)	6	303.2	L1 L2 L3

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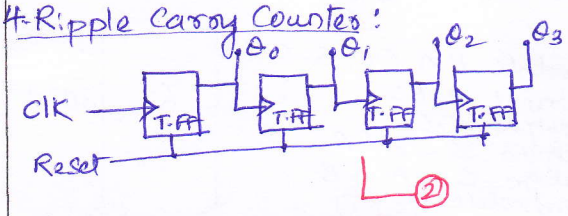
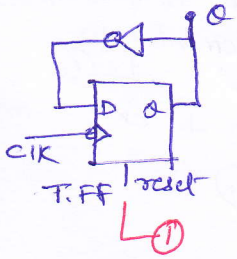
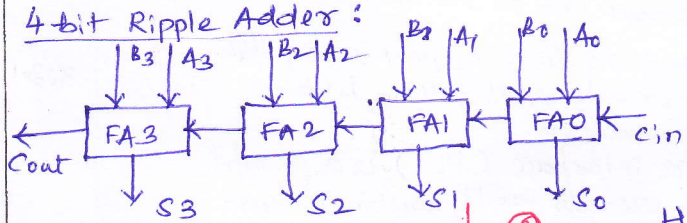
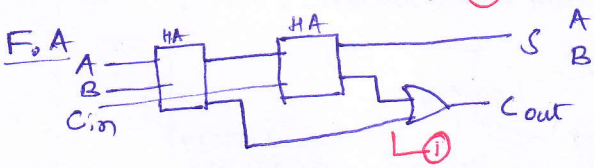
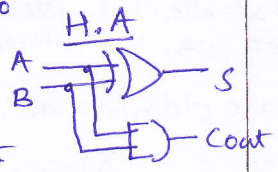
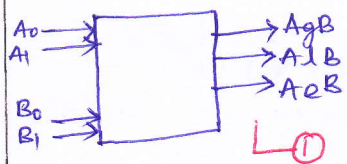
Sem : 5		Subject : Verilog HDL	Sub Code :	Date : 11/09/2018		
Q. No.	Bit	Description		Marks	CO's	RBT LEVEL
3.	a.	Digital Design Methodologies ① TOP-DOWN ② BOTTOM-UP		6	303.2	L1 L2 L3
		① Top level Block → Sub Block 1, Sub Block 2 → Leaf cell, Leaf cell, Leaf cell, Leaf cell ④				
		② Top level Block → Macro Cell 1, Macro Cell 2 → Leaf cell, Leaf cell, Leaf cell, Leaf cell				
		+ Expn ②				
	b.	4-Ripple Carry Counter:		6	303.3	L1 L2 L3
		 ②				
		 ①				
		TT + Program ③				
4.	a.	4 bit Ripple Adder:		6	303.3	L1 L2 L3
		 ②				
		F.A  ①				
		H.A 				
		TT + Program ③				
	b.	 ①	TT + Program ③	6	303.3	L1 L2 L3
		Expressions:				
		$A=B = \bar{A_0}B_0 + \bar{A_1}B_1(\bar{A_0} + B_0)$				
		$A>B = A_0\bar{B_0} + A_1B_1(\bar{B_0} + A_0)$				
		$A<B = (\overline{A_1 \oplus B_1}) + (\overline{A_0 \oplus B_0})$ ②				

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