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# HirasugarInstitute of Technology, Nidasoshi.

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| E&E Engg. Dept. |
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| Exam. |
| Internal Assessment |
| Odd Sem(2017-18) |

## FIRST INTERNAL ASSESSMENT

Sem: **5** Sub: **Verilog HDL** Sub. **Code: 15EC53**

Date: **15.09.2017** Time: **11am to 12pm** Max. Marks: **25**

***Note: Answer two full questions, draw sketches wherever necessary.***

| Q. No | | Discription of Question | Marks | CO's |
|---|---|---|---|---|
| 1 | a | With diagram, explain typical design flow. | 7 | CO303.1 |
| | b | Explain the structure of Verilog module. | 6 | CO303.1 |
| | | **--OR--** | | |
| 2 | a | List the useful features of Verilog HDL. | 7 | CO303.1 |
| | b | Name the different types of operators in Verilog. Explain the Logical. operators. | 6 | CO303.2 |
| 3 | a | Explain the two basic types of design methodology with diagram. | 6 | CO303.2 |
| | b | Write Verilog code for 4-bit ripple carry counter. | 6 | CO303.3 |
| | | **--OR--** | | |
| 4 | a | Write diagram of a 4-bit ripple carry adder and Boolean functions in Verilog. Draw the simulation waveform. | 6 | CO303.3 |
| | b | Write an Verilog code in data flow description for a 2-bit magnitude comparator with the help of truth table & simplified Boolean expression. | 6 | CO303.3 |

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| AY: 2017-18 (Odd) |



# - IA SCHEME OF EVALUATION

| Sem : 5 | Subject : Verilog HDL | Sub Code : 15EC53 | Date : 15/9/17 |
|---|---|---|---|

| Q. No. | Bit | Description | Marks | Mapped CO's |
|---|---|---|---|---|
| 1) | a. | Design specification<br>Behavioral Description<br>RTL Description (HDL)<br>Functional Verification & Testing<br>Logical Synthesis / Timing verification<br>Gate level Netlist<br>Logical verification and testing<br>Floor planning Automatic place & Route<br>Physical layout<br>Layout Verification<br>Implementation (5)<br>+ Explanation (2) | [7M] | |
| | b. | Explanation + (4)<br>Example:<br>module HA (A, B, S, C);<br>input A, B;<br>output S, C;<br>assign S = A ^ B;<br>assign C = A && B;<br>End module. (2) | [6M] | |
| 2) | a. | Features: Verilog:<br>- Easy to learn & easy to use.<br>- different levels of abstraction to be mixed in the same model<br>- Most popular logic synthesis tools support verilog HDL.<br>- All fabrication vendors provide verilog HDL libraries for post logic synthesis simulation.<br>- Programming Language Interface (PLI) is a powerful feature that allows the user to write Custom 'C' code to interact with the internal data structures of verilog. | [7M] | |
| | b. | Operators are classified as:<br>- Logical<br>- Relational<br>- Arithmatic<br>- Shift (2)<br>Logical.<br>(binary) Bitwise: &, \|, ~(&), ~(\|), ~(^)<br>(binary) Boolean: &&, \|\|<br>(unary) Reduction.: &, \|, ~, ~(&), ~(\|), ~(^) (4) | [6M] | |

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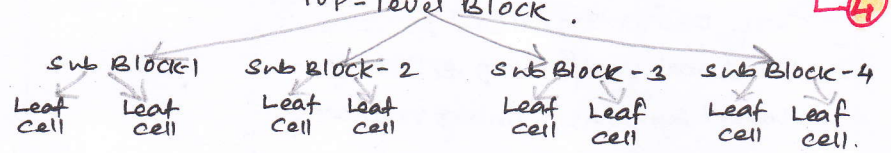
# - IA SCHEME OF EVALUATION

| Sem : | | Subject : | Sub Code : | Date : | |
|---|---|---|---|---|---|
| Q. No. | Bit | Description | | Marks | Mapped CO's |

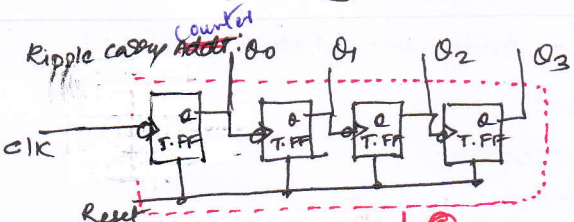
**3) a.** Digital Design Methodologies: ① TOP-DOWN ② BOTTOM-UP (4)



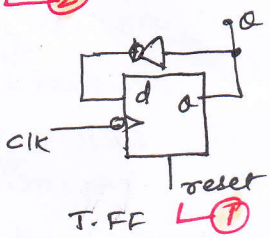

[6M]

+ BOTTOM up diagram + Expn (2)

**b.** Ripple carry counter




(2)

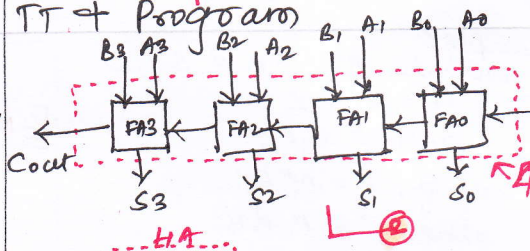



(1)

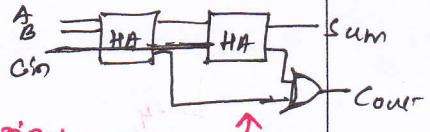
[6M]

(3) TT + Program

**4) a.**

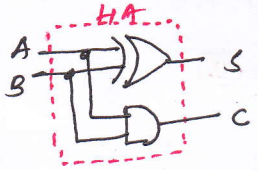



(2) 4-bit ripple Adder



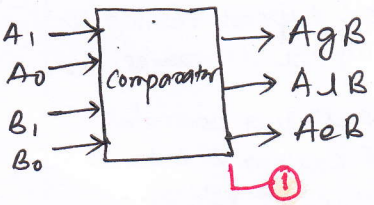

FA (1)

[6M]




+ TT + Program (3)

**b.**




(1)

TT + Program. (3)

[6M]

Expressions:

$A_eB = \overline{A_0} B_0 + \overline{A_1} B_1 (\overline{A_0} + B_0)$

$A_gB = A_0 \overline{B_0} + A_1 B_1 (\overline{B_0} + A_0)$

$A_eB = (\overline{A_1 \oplus B_1}) + (\overline{A_0 \oplus B_0})$

(2)

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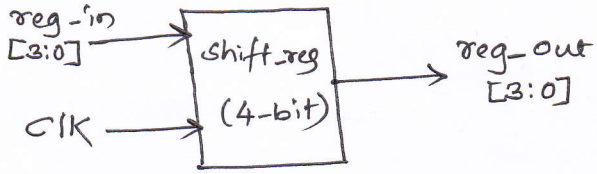
# SECOND INTERNAL ASSESSMENT

Sem: 5 | Sub: **Verilog HDL** | Sub. **Code: 15EC53**
Date: **18.10.2017** | Time: **11am to 12pm** | Max. Marks: **25**

***Note: Answer two full questions, draw sketches wherever necessary.***

| Q. No | | Discription of Question | Marks | CO's |
|---|---|---|---|---|
| 1 | a | Explain Data types of Verilog with suitable examples. | 7 | CO303.2 |
| | b | Write a note on i. Comments ii. Number specification iii. X and Z values iv. Identifiers and Keywords with suitable examples. | 6 | CO303.2 |
| | | ---------OR---------- | | |
| 2 | a | A 4-bit parallel Shift register has I/O pins as shown in the figure below. Write the module definition for this shift register. Include the list of ports and port declarations (no need to show the internals).   | 7 | CO303.3 |
| | b | Explain a components of a Verilog module with a neat diagram. | 6 | CO303.3 |
| 3 | a | Write Verilog Description for 4-bit Ripple carry FullAdder, wih stimulus. | 6 | CO303.3 |
| | b | Write Verilog code for 4to1 Multiplexer, at Gate level with stimulus. | 6 | CO303.3 |
| | | ----------OR---------- | | |
| 4 | a | Write data flow level of abstraction in Verilog of a 4-bit carry lookahead. | 6 | CO303.3 |
| | b | Write the result of the following operation if A=10010011 and B=01101111. i. A<<<2 ii. A%2 iii. !(&B) iv. &B v. A&&B | 6 | CO303.3 |

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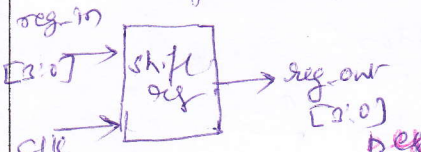
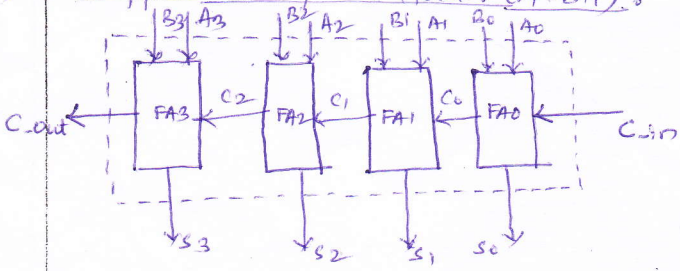
# - IA SCHEME OF EVALUATION

| Sem : 5 | Subject : Verilog HDL | Sub Code : 15EC53 | Date : 18/10/2017 |
|---|---|---|---|

| Q. No. | Bit | Description | Marks | Mapped CO's |
|---|---|---|---|---|
| 1 | a) | Data types: Nets, Registers, Vectors, Integer, Real, Time, Arrays, Memories, Parameters, strings (3) + Examples (4) | 7M | 303.2 |
| | b) | i. Comments: readability & documentation // /* */<br>ii. Number specification: sized 4'b1111, 4'd 99, unsized 'h 2BC, signed – 6'43<br>iii. x or z values: unknown (x), impedance (z)<br>iv. Identifiers & Keywords: define the language constructs | 6M | 303.2 |
| 2 | a) |  Design (3) + Coding (4) | 7M | 303.3 |
| | b) | Components of Verilog module:<br>Module Name, Port list, Port Declaration, Parameters<br>Declarations of 'wires', 'regs' and other variables<br>Data flow statements (assign)<br>Instantiation of lower level models<br>always and initial blocks. All behavioral statements go in these blocks<br>Tasks & functions<br>endmodule statements<br>Diagram (3) + Expln. (3) | 6M | 303.3 |
| 3 | a) | Ripple carry full Adder (4-bit):<br>  <br>Design (2) + Coding (2) + stimulus (2) | 6M | 303.3 |

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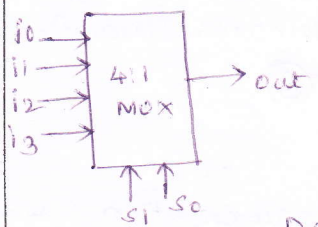
# - IA SCHEME OF EVALUATION

| Sem : | | Subject : | Sub Code : | Date : | |
|---|---|---|---|---|---|
| Q. No. | Bit | Description | | Marks | Mapped CO's |

**(3) b)** 4 to 1 Multiplexer:




| S1 | S0 | out |
|---|---|---|
| 0 | 0 | i0 |
| 0 | 1 | i1 |
| 1 | 0 | i2 |
| 1 | 1 | i3 |

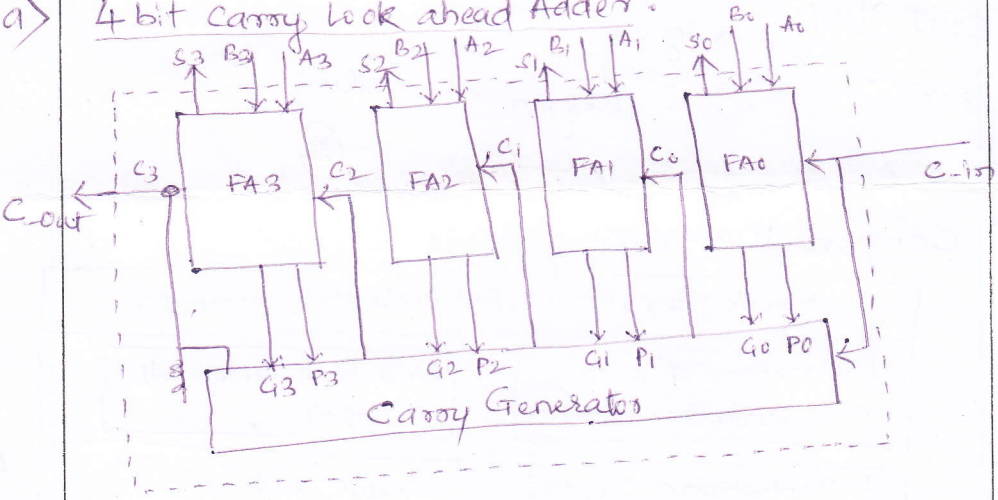
Circuit

Design + code + stimulus

(2) (2) (2)

6M — 303.3

**(4) a)** 4 bit Carry Look ahead Adder:




Design + code + stimulus

(2) (2) (2)

$P_i = A_i \oplus B_i$ $G_i = A_i \cdot B_i$ C_out = C3 @ C-1 = C_in

$S_i = A_i \oplus B_i \oplus C_{i-1}$

$C_i = G_i + P_i \cdot C_{i-1}$

6M — 303.3

**b)**

i. 01001111

ii. 1

iii. 1

iv. 0

v. 1 (True)

6M — 303.3

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## THIRD INTERNAL ASSESSMENT

Sem: **5** Sub: **Verilog HDL** Sub. **Code: 15EC53**

Date: **19.11.2017** Time: **11am to 12pm** Max. Marks: **25**

***Note: Answer two full questions, draw sketches wherever necessary.***

| Q. No | | Discription of Question | Marks | CO's |
|---|---|---|---|---|
| 1 | a | Write a Verilog behavioral 4:1 Multiplier program using CASE statement. | 7 | CO303.4 |
| | b | Explain LOOP statements in Verilog with example. | 6 | CO303.4 |
| | | **---------OR----------** | | |
| 2 | a | Write a note on Generate LOOP. | 7 | CO303.4 |
| | b | Write verilog Behavioral descriptiton program of 4-bit counter. | 6 | CO303.4 |
| 3 | a | Why VHDL? | 6 | CO303.5 |
| | b | Write a note on Data types in VHDL. | 6 | CO303.5 |
| | | **----------OR----------** | | |
| 4 | a | Write note on structure of VHDL module. | 6 | CO303.5 |
| | b | Write Full adder Data flow description program in verilog. | 6 | CO303.5 |

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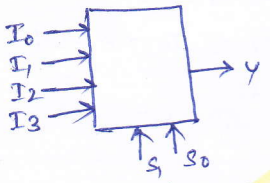
# - IA SCHEME OF EVALUATION

| Sem : 5 | Subject : Verilog HDL | Sub Code : 15EC53 | Date : 24/11/17 |
|---|---|---|---|

| Q. No. | Bit | Description | Marks | Mapped CO's |
|---|---|---|---|---|

**Q1) a. 7**

4:1 MUX :




(2)

+ Program

```
case ({S1,S0})
2'b00 : y = I0;
2'b01 : y = I1;
2'b10 : y = I2;
2'b11 : y = I3;
default : y = 1'bx;
Endcase
```

(4)

7M

**b. 6**

Loops :

'For' (2) 'while' (2) 'repeat' (1) 'forever' (1)

```
for (i=0; i<n; i=i+1)

i=0
while (i<n)
begin
  i=i+1;
end

repeat(n)
begin
end

forever #20 Q=~Q;
```

6M

**Q2) a. 7**

Generate Block : Explain (3)

Ex: (4)

```
module bitwise_XOR (out, A, B);
  Parameter N=32;
  output [N-1:0] out;
  input [N-1:0] A, B;
  genvar i;
  generate for (i=0; i<N; i=i+1)
    begin
      XOR (out[i], A[i], B[i]);
    end
  endgenerate
endmodule
```

7M

**b. 6**

4-bit counter :

Block dia (2)

```
always@ (posedge clr or negedge clk)
begin
  if (clr)
    Q <= 4'd0;
  else
    Q <= Q+1;
end
```

(4)

6M

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# - IA SCHEME OF EVALUATION

| Sem : | | Subject : | Sub Code : | Date : | |
|---|---|---|---|---|---|
| Q. No. | Bit | Description | | Marks | Mapped CO's |

**Q3)** a. (6)

**Why VHDL?**

- Power & flexibility
- Device Independent design
- Portability
- Benchmarking capabilities
- ASIC migration
- Fast time to market
- Low cost.

(6)

6M

b. (6)

**Data type:**

Data types in VHDL.

- Scalar
  - Bit
  - Boolean
  - Integer
  - Real
  - character
  - Physical
  - User defined
  - Severity
  - Natural
- Composite
  - Bit_vector
  - Array
  - Record
- Access
- File
- Others
  - std_logic
  - std_logic_vector
  - signed
  - unsigned

(6)

6M

**Q4)** a. (6)

**Structure of VHDL module:**

→ Two major constructs : Entity and Architecture + Explan.

(3)

```
Entity Adder is
  port ( A,B: in std_logic ; S,C : out std_logic);
end Adder;
Architecture HA of Adder is
begin
    S<= A XOR B;
    C<= A AND B;
End HA;
```

(3)

6M

b. (6)

**Full Adder:**


Design → TT
Expn

(3)

Program

```
Architecture FA of Adder is
begin
S<= A XOR B XOR Ci;
CO <=((A XOR B) AND Ci) OR
      (A AND B) ;
End FA;
```

(3)

6M

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