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Hirasugar Institute of Technology, Nidasoshi.

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Exam.
IA I
Even Sem (2017-18)

FIRST INTERNAL ASSESSMENT

Sem: IV **Sub:Microprocessor** **Sub. Code: 15EC42**

Date: 05/03/18 **Time: 03:00pm-04:00pm** **Max. Marks:25**

Note: Answer two full questions, draw sketches wherever necessary.

Q. No		Discription of Question	Marks	CO	RBT LEVEL
1	a	Explain the architecture of 8086 Microprocessor with a neat diagram along with functions of each block.	7	C210.1	L1,L2,L3
	b	Expalin the function of following units 1] Instruction Queue 2] Index Registers 3]Segment Registers	6	C210.1	L1,L2,L3
OR					
2	a	Explain PSW Register of 8086.	6	C210.1	L1,L2,L3
	b	Explain the following PINS of 8086. 1] LOCK 2] HOLD/HLDA 3] RQ/GT 4]INTA	7	C210.1	L1,L2,L3
3	a	How 20 bit Physical address is generated in 8086 Explain.	6	C210.1	L1,L2,L3
	b	Identify the Adressing Mode for the following instruction & Explain its working 1] MOV AX,100[BP] 2]MOV NUM[BX+SI] ,AX 3]MOV CL,'A'	6	C210.1	L1,L2,L3
OR					
4	a	Define any four Adressing mode in 8086 & Explain in detail with 2 examples each.	6	C210.1	L1,L2,L3
	b	Identify following Addressing Mode & Explain its working. 1] MOV BX,0345H 2]ADD AL,[BX+04] 3]MOV AX,[BX+SI] 4] MOV AX,[BX+SI+04]	6	C210.1	L1,L2,L3

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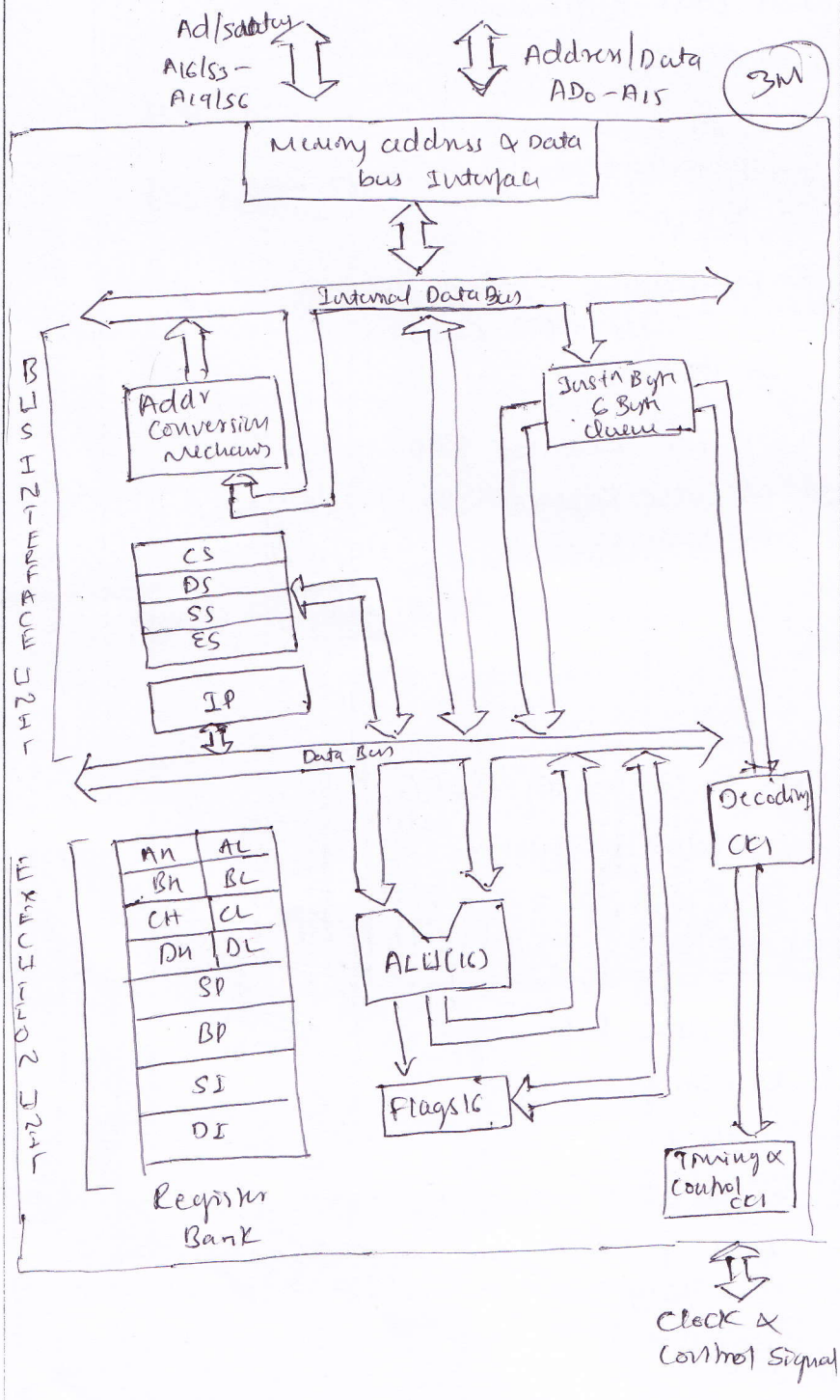
IA -I SCHEME OF EVALUATION

Sem : IV	Subject : Microprocessor	Sub Code : 15EC42	Date : 05/03/18

Q. No.	Bit	Description	Marks	CO's	RBT LEVEL
1	a	Architecture of 8086 Microprocessor	7	C210.1	L1, L2, L3



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SCHEME OF EVALUATION

Sem : IV | Subject : Microprocessor | Sub Code : 15EC42 | Date : 05/03/18

Q. No.	Bit	Description	Marks	CO's	RBT LEVEL
1	a	① BIU Interface unit Explanation ② Execution unit Explanation (4)			
1	b	① Explanation for Instruction queue with 6 bytes (2) ② Explanation Index Register (2) ⓐ Source Index Register ⓑ Destination " " (3) Segment Register Explanation (2) a) Code Segment c) Stack Segment b) Data Segment d) Extra "	6	C210.1	L1,L2,L3
2	a	PSW Register of 8086 Program Status Word 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 x x x x O D I T S Z x AC x P x CY → (3M) O – Overflow Bit D – Direction " T – Trap Flag " S – Sign " Z – Zero " " AC – Auxillary carry P – Parity Cy – carry Flag bit → (3M)	6	C210.1	L1,L2,L3

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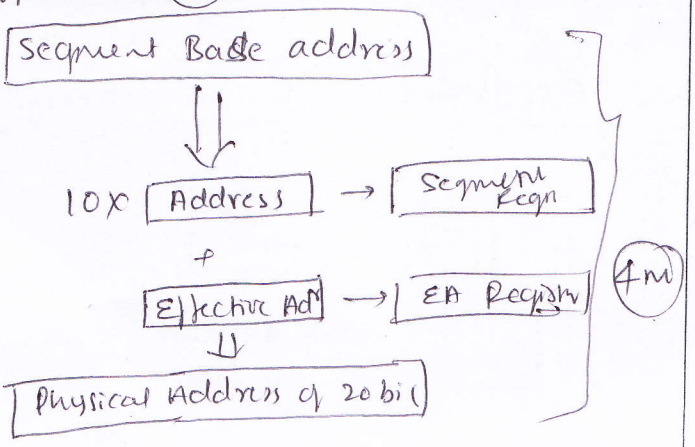
SCHEME OF EVALUATION

Sem : IV | Subject : Microprocessor | Sub Code : 15EC42 | Date : 05/03/18

Q. No.	Bit	Description	Marks	CO's	RBT LEVEL
2	b	Explaination for the following pins of 8086 1) LOCK → Locking the Bus service for Processor - Execution (1) 2) HOLD/HLDA → Hold & Hold response from the processor in Max Mode (2.5) 3) RQ/GT → Request & Grant pins (2.5) 4) INTA → Interrupt Acknoledgement (1)	7	C210.1	L1,L2,L3
3	a	Physical Address generation of 8086 Processor — (2M) 	6	C210.1	L1,L2,L3
3	b	(1) MOV AX, 100[BP] → Realative Based A.M — (2) (2) MOV NUM[BX+SI], AX → Ralative Base plus Index A.M — (2) (3) MOV CL, 'A' → Immidiate A.M — (2)	6	C210.1	L1,L2,L3

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SCHEME OF EVALUATION

Sem : IV | Subject : Microprocessor | Sub Code : 15EC42 | Date : 05/03/18

Q. No.	Bit	Description	Marks	CO's	RBT LEVEL
4	a	Addressing modes – Definition (2) Explanation for 2 A.M → (4)	6	C210.1	L1,L2,L3
4	b)	1) MOV BX, 034H — (1.5M) 3) MOV AX, [BX+SI] — (1.5M) 3) ADD AL, [BX+04] — (1.5M) 4) MOV AX, [BX+SI+04] — (1.5M)	6	C210.1	L1,L2,L3

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SCHEME OF EVALUATION IA- II

Sem : IV | Subject : Microprocessor | Sub Code : 15EC42 | Date : 11/04/18

Q. No.	Bit	Description	Marks	CO's	RBT LEVEL
1	a	Assembler Directives of 8086 & operators 1) DB - Define Byte 2) DW - Define word 3) DQ - Define Quadword 4) DT - Define Tenbytes 5) ASSUME - Assume Logical segment 6) END - End of program 7) ENDP - End of procedure 8) ENDS - End of segment 9) EVEN - Align of Even memory 10) EQU - Equate 11) EXTRN - External access 12) PUBLIC - Publically access 13) GROUP - Group Related Segments 14) LABEL → Allocation of Labels 15) ORG - Origination of segment 16) PROC - call for Procedure 17) - PTR - Pointer 18) PUBLIC - access Publically 19) SEG - Segment of label 20) SEGMENT - Logical Segment 21) SHORT - Lengthing displacement (+127 to -128) 22) TYPE - operator label type 23) GLOBAL - Variables	7	C210.2	L1,L2,L3

1	b	Addition of Two 16 digit packed BCD Number
		Data segment
		N1 dw 1234h,5678h,5678h,1234h
		N2 dw 5678h,1234h,1234h,5678h
		Res dw 0000h, 0000h, 0000h, 0000h.
		data Ends
		Assum CS: code, ds:data.
		Code Segment
		MOV Ax,data
		MOV ds,Ax
		Lea Si, N1+3
		Lea di, N2+3
		Lea bx, Res+3
		MOV CL, 04h
		up: MOV Ax,[Si]
		MOV Dx,[di]
		ADC Ax,Dx
		MOV [Bx],Ax
		dec Si
		dec di
		dec Bx
		dec cl
		jnz up
		MOV ah,4ch
		INT 21h
		Code ends
			6	C210.2	L1,L2,L3

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Exam.
IA II
Even Sem (2017-18)

SECOND INTERNAL ASSESSMENT

Sem: IV **Sub:Microprocessor** **Sub. Code: 15EC42**

Date: 11/04/18 **Time: 03:00pm-04:00pm** **Max. Marks:25**

Note: Answer two full questions, draw sketches wherever necessary.

Q. No		Discription of Question	Marks	CO	RBT LEVEL
1	a	Explain all the Assembler directives and Operators of 8086 with examples.	7	C210.2	L1,L2,L3
	b	Write an Assembly level Language program to add two 16 digit packed BCD number.	6	C210.2	L1,L2,L3
		OR			
2	a	Explain all the logical & string manipulation instruction of 8086 with examples.	6	C210.2	L1,L2,L3
	b	Explain all the Falg manipulation and processor control instruction of 8086 with examples.	7	C210.2	L1,L2,L3
3	a	What do you mean by IVT?Exaplin IVT of 8086 processor.	6	C210.3	L1,L2,L3
	b	Explain the classification of interrupts in 8086. Explain 8086 interrupt mechanism.	6	C210.3	L1,L2,L3
		OR			
4	a	Explain Hardware interrupts of 8086	6	C210.3	L1,L2,L3
	b	Expalin Interrupt INT N interrupt instruction	6	C210.3	L1,L2,L3

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SCHEME OF EVALUATION IA- II

Sem : IV | Subject : Microprocessor | Sub Code : 15EC42 | Date : 11/04/18

Q. No.	Bit	Description	Marks	CO's	RBT LEVEL
2	a	Logical & String Manipulation Instruction of 8086 with examples	6	C210.2	L1, L2, L3

① Logical Instructions

1) AND - Logical AND
2) OR - Logical OR
3) NOT - Logical Invert
4) XOR - Logical Enclusive OR
5) TEST - Logical compare instruction
6) SHL/SAL - Shift logical/Arithmatic Left
7) SHR - Shift Logical Right
8) SAR - Shift Arithmatic "
9) ROR - Rotate without Cary Right
10) ROL - Rotate Left without cary
11) RCR - Rotate Right with cary
12) RCL - Rotate Left through cary

String Instn

13) REP - Repeat Prefix
14) MOVSB/MOVSW -
15) CMPS - compare string
16) SCAS, LODS, STOS

2	b)	Flag manipulation & processor control Instn	7	C210.2	L1, L2, L3

1) CLC - Clear Cary Flag
2) CMC - Complement cary
3) STC - Set Cary Flag
4) CLD - Clear direction Flag
5) CLI - Clear Interrupt "
6) STI - Set interrupt "

1) WAIT -
2) HLT
3) NOP
4) ESC
5) LOCK

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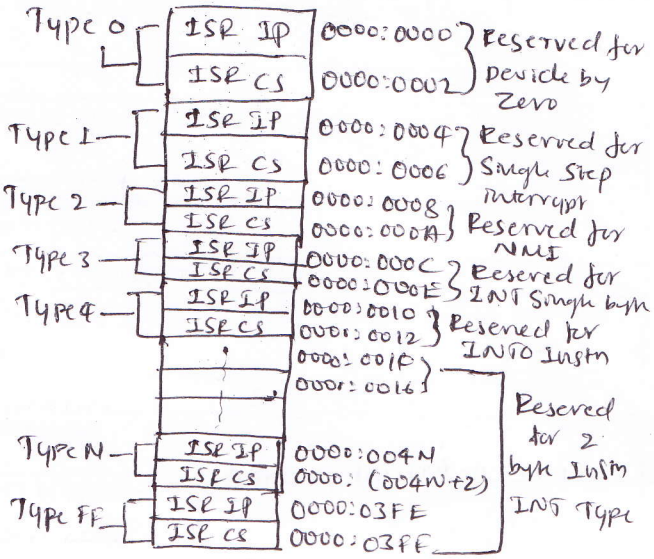
SCHEME OF EVALUATION IA- II

Sem : IV | Subject : Microprocessor | Sub Code : 15EC42 | Date : 11/04/18

Q. No.	Bit	Description	Marks	CO's	RBT LEVEL
3	a)	IVT – Interrupt Vector Table	6	C210.3	L1,L2,L3



3	b)	Classification 1) Maskable Interrupt 1) Hardware Interrupt 2) Non Maskable " 2) Software "	6	C210.3	L1,L2,L3

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SCHEME OF EVALUATION IA- II

Sem : IV **Subject :** Microprocessor **Sub Code :** 15EC42 **Date :** 4/04/18

Q. No.	Bit	Description	Marks	CO's	RBT LEVEL
4)	a	Hardware interrupt of 8086 1) NMI 2) INTR	6	C210.3	L1,L2,L3
4	b	Explain INT N interrupt instruction	6	C210.3	L1,L2,L3

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ECE Dept
Exam.
IA III
Even Sem (2017-18)

THIRD INTERNAL ASSESSMENT

Sem: IV **Sub:Microprocessor** **Sub. Code: 15EC42**

Date: 18/05/18 **Time: 03:00pm-04:00pm** **Max. Marks:25**

Note: Answer two full questions, draw sketches wherever necessary.

Q. No		Discription of Question	Marks	CO	RBT LEVEL
1	a	Interface Eight seven segment display using 8255 with 8086.	7	C210.4	L3
	b	What is maximum mode of operation for 8086 CPU explain in detail.	6	C210.4	L3
		OR			
2	a	Differentiate between memory mapped I/O & I/O mapped I/O schemes.	6	C210.4	L3
	b	What is minimum mode of operation for 8086 CPU explain in detail.	7	C210.4	L3
3	a	Explain the Architecture of 8087 Processor.	6	C210.5	L3
	b	Explain the difference between Von-Neuman & Harvard CPU architecture.	6	C210.5	L3
		OR			
4	a	Explain the interconnection of 8087 with the CPU.	6	C210.5	L3
	b	Explain the difference between CISC & RISC CPU architecture.	6	C210.5	L3

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SCHEME OF EVALUATION - III IA

Sem : IV	Subject : Microprocessor	Sub Code : 15EC42	Date : 18/05/18		
Q. No. / Bit	Description		Marks	CO's	RBT LEVEL

4 a — Marks: 7 | CO's: C210.4 | RBT LEVEL: L3

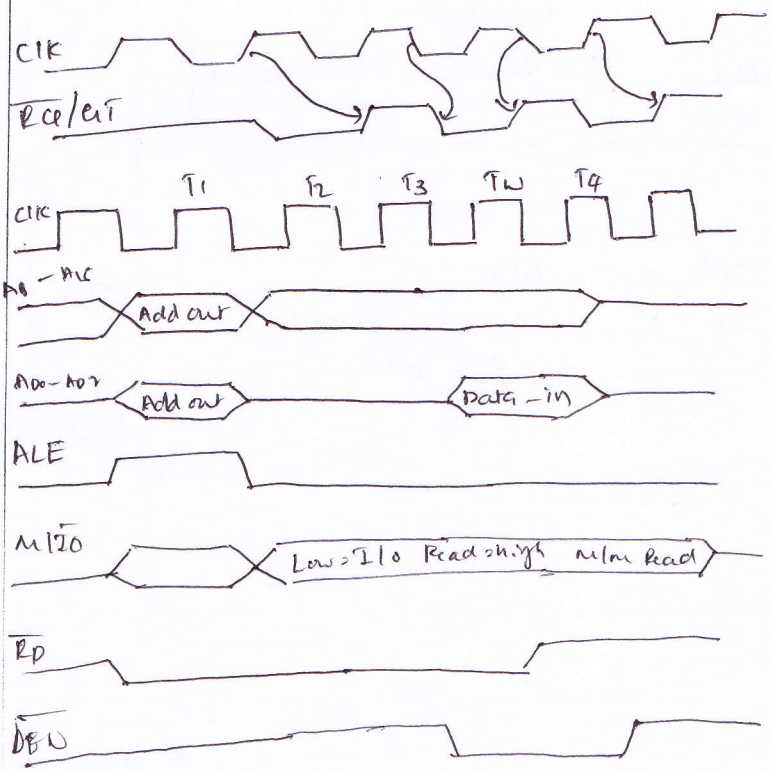
Interface Eight Seven Segment display using 8255 with 8086.

CKT diagram port A & port B of 8255 Configured to interface Seven segment display is drawn

PA = 00H, PB = 02H, PC = 04H, CR = 06H

4 b — Marks: 6 | CO's: C210.4 | RBT LEVEL: L3

Maximum mode of operation for 8086 CPU



Read operation

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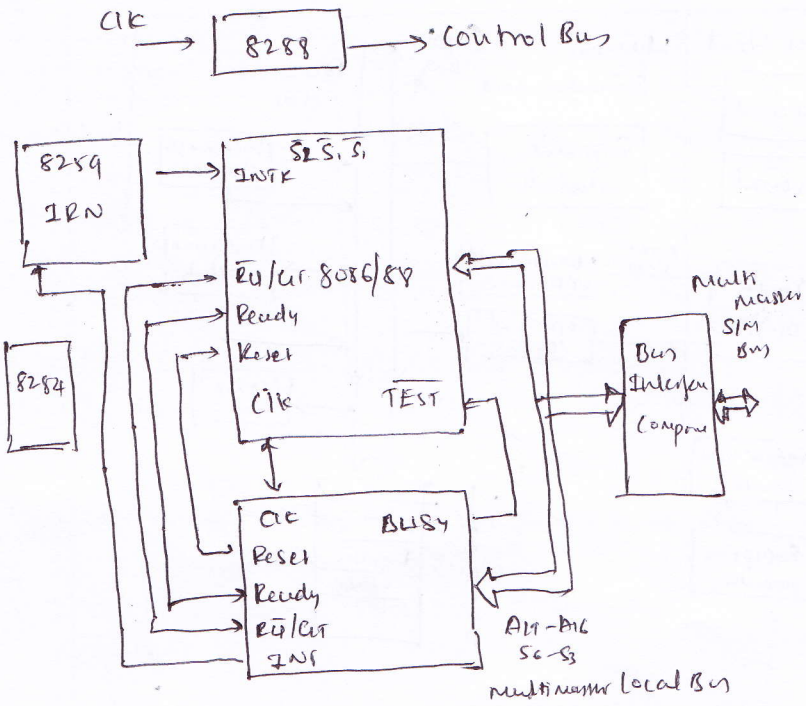
SCHEME OF EVALUATION

Sem : IV	Subject : Microprocessor	Sub Code : 15EC42	Date : 18/05/18

Q. No.	Bit	Description	Marks	CO's	RBT LEVEL
4	a	Interconnection of 8087 with the CPU  	6	C210.5	L3
4	b	Difference Between CISC & RISC CPU architecture CISC ① Instn size varies ② Instn length 1,2,3 or 4 bytes ③ More No. of Instn ④ Complex to decode Instn ⑤ Few Registers ⑥ H/w complicated RISC ① Fixed ② 4 bytes ③ Less Num of Instn ④ Easy to Decode ⑤ Many Registers ⑥ H/w NOT complicated	6	C210.5	L3

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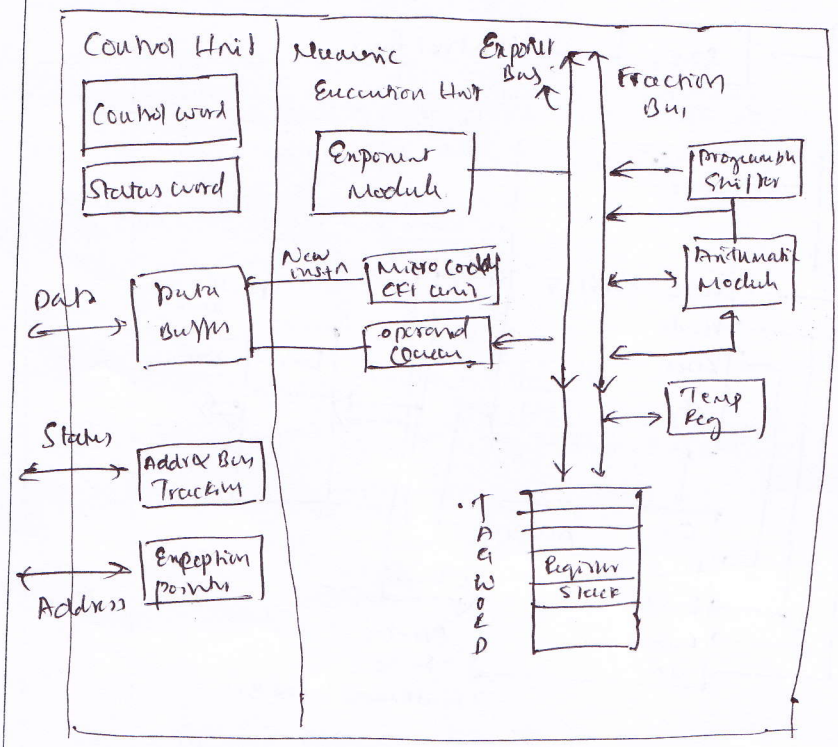
SCHEME OF EVALUATION

Sem : IV | Subject : Microprocessor | Sub Code : 15EC42 | Date : 18/05/18

Q. No.	Bit	Description	Marks	CO's	RBT LEVEL
3	a	Architecture of 8087 processor 	6	C210.5	L3
3	b	Von-Neuman | Hardwired CPU ① Consists of processor, Instn decoder, M/m Unit | ① It consists of separate M/m bank, processor, Instn decoder ② Execution of instn relatively slow | ② Execution of Instn is faster because fetching of code & data separately & simultaneously ③ RISC & CISC architecture is used | ③ RISC architecture is used ④ Parallelism | ④ more parallelism ⑤ General Mp | ⑤ Microcontroller ⑥ Real time Sim | ⑥ Real time Sim	6	C210.5	L3

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SCHEME OF EVALUATION

Sem : IV	Subject : Microprocessor	Sub Code : 15EC42	Date : 08/05/18

Q. No.	Bit	Description	Marks	CO's	RBT LEVEL
2	a	• Differentiate between Memory mapped I/O & I/O mapped I/O Schemes	6	C210.4	L3

M/M mapped I/O	I/O mapped I/O
① Address is 20 bit	① Address is 16 bit
② All M/M related instn can be used to access I/O	② IN, OUT instn are used to access
③ M/$\overline{IO}$ signal is made high	③ M/$\overline{IO}$ signal is made low
④ Maximum Memory 1MB	④ Maximum I/O devices 256 for direct & 65536 for indirect
⑤ More Hardware Required	⑤ Less Hardware Required
⑥ Faster access Comparatively	⑥ Slower access comparatively

2	b	Minimum mode operation Timing diagram of Minimum mode operation in both Read & Write operation	7	C210.4	L3

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