Analog Electronics (15EC32)

Module-5 Power Amplifiers Class : III Sem

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Syllabus.

Power Amplifiers: Definition and amplifier types, Series fed class A amplifier, Transformer coupled class A amplifier, Class B amplifier operation and circuits, Amplifier distortion, Class C and Class D amplifiers.

Voltage Regulators: Discrete transistor voltage regulation - Series and Shunt Voltage regulators

Text Book:

Robert L. Boylestad and Louis Nashelsky, —Electronics devices and Circuit theory ,

A **Power amplifier** in a stereo, radio or television system is **intented** to **deliver** a **large voltage** and **current into** a **low impedance** load such as a **loud speaker**.

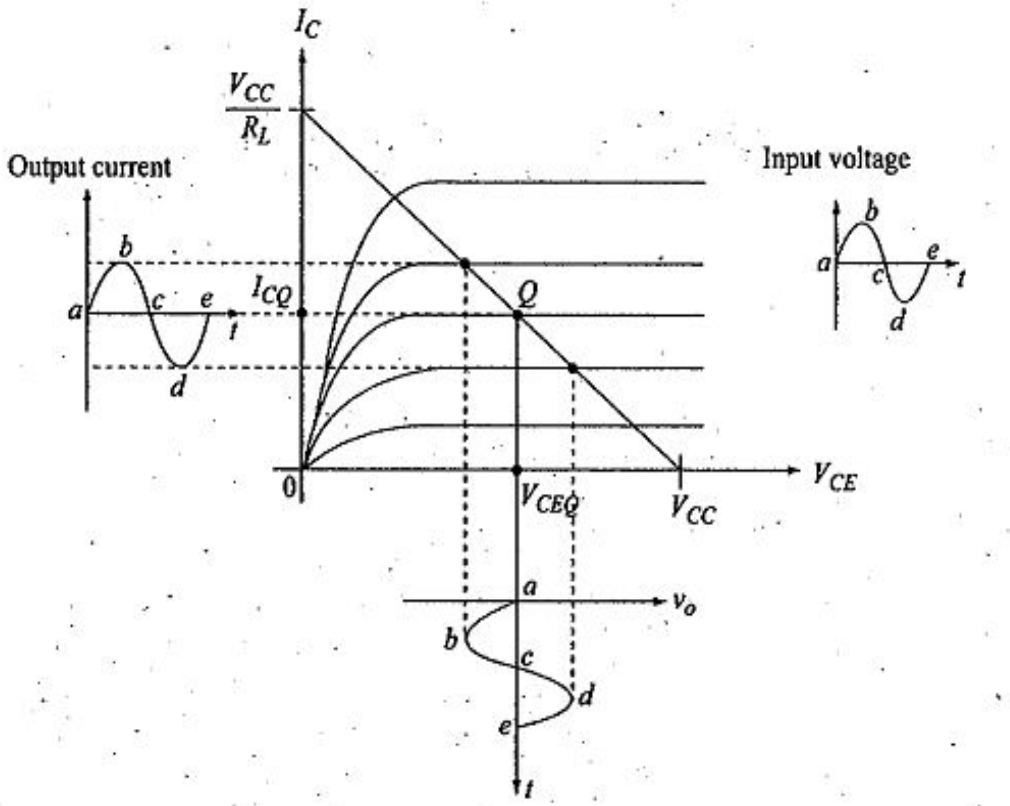
The power amplifiers are classified into :

1. **Class A power amplifier**
2. **Class B power amplifier**
3. **Class AB power amplifier**
4. **Class C amplifier**
5. **Class D power amplifier**

1. Class A Power amplifier :-

In class A power amplifier, the **Q-point** is **located** at the **centre** of the **load line** as shown in the figure, so that the **output signal varies over** the **full cycle** of the **input signal**.

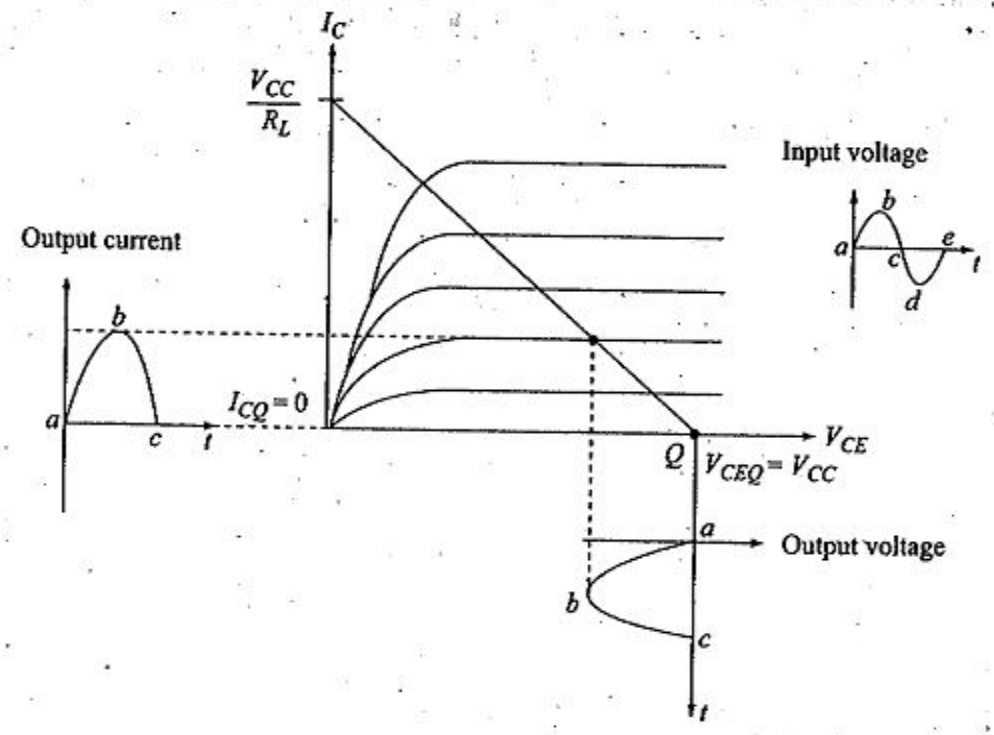
So **collector current flows** for **360^0 (FULL Cycle)** of the **input signal.**



2. Class B Power amplifier :-

In class B power amplifier, the **Q-point** is **located** at **cut-off** region of the **load line** as shown in the figure, so that the **output signal varies over one half cycle** of the **input signal**.

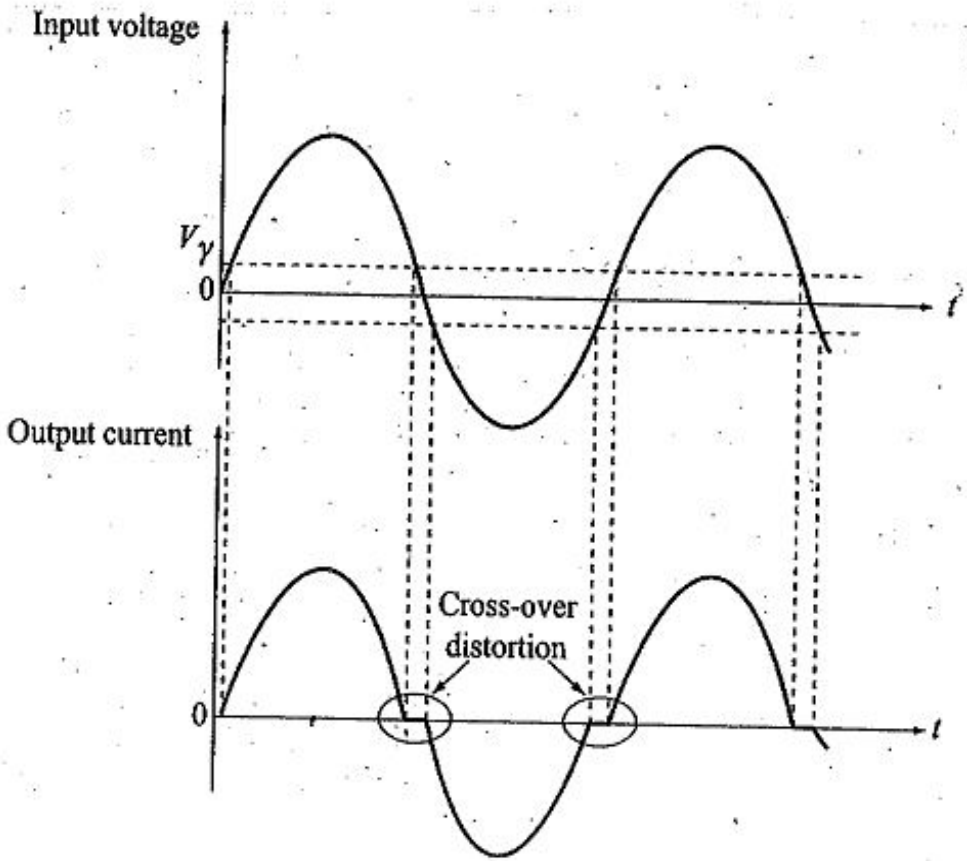
So **collector current flows** for **180^0 (HALF Cycle)** of the **input signal.**



3. Class AB Power amplifier :-

In class AB power amplifier, the **Q-point** and the **Input signal** are **selected** such that the **output signal** is **obtained** for **more** than **180^0** but less than **360^0**, for a **full input cycle**.

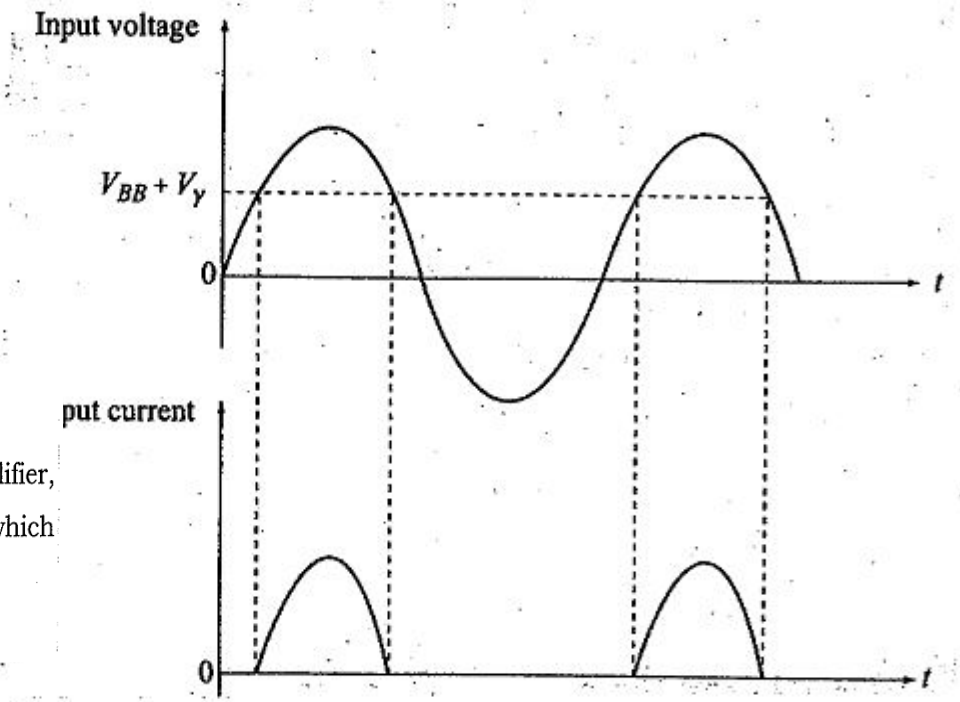
The **efficiency** of **class AB** amplifier is more than **Class A** but less than **Class B** amplifier.



4. Class C Power amplifier :-

In class C power amplifier, the **transistor** is **biased below cut-off** region as shown in figure. The **Q-point** of the transistor **remains** in **active** region for less than a **half cycle**. So only that much part is **reproduced** at the **output**. For the **remaining cycle** of the **input**, the transistor **remains** in **cut-off** region.

So the **collector current flows** for **less than 180°**.

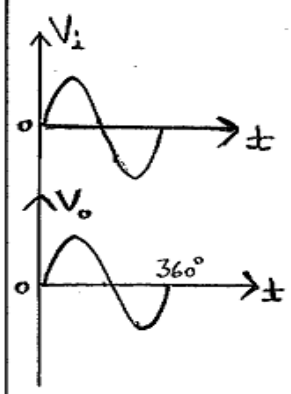
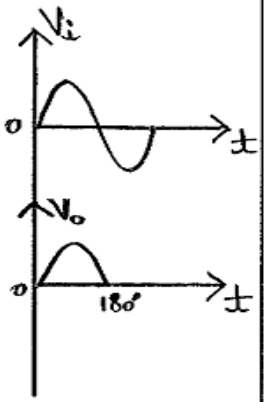
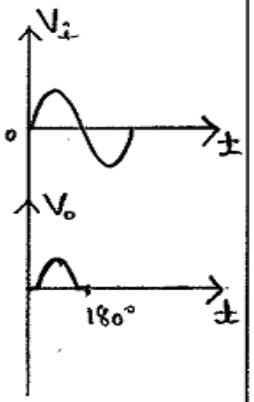
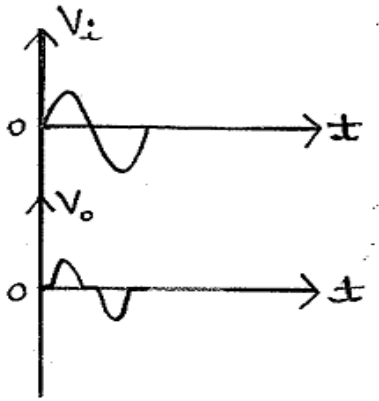


5. Class D Power amplifier :-

A class D amplifier is another class of power amplifier, which is **designed** to **operate** with **PULSE** (digital) signals, which are **ON** for a **short interval** and **OFF** for a **longer interval**.

The **overall efficiency** of **Class D** amplifier is **very HIGH**.

❖ Comparision of power amplifiers :-

Class	A	B	C	AB
Operating cycle	360⁰	180⁰	Less than 180⁰	More than 180⁰ & less than 360⁰
Position of Q-point	Centre of load line	On X-axis	Below X-axis	Above X-axis but below the centre of load line.
Input-Output waveforms				
Efficiency	Poor i.e 25% to 50%	Better, 78.5%	High	More than class A and Less than Class B amplifier
Distortion	Absent No distortion	Present More than class A	Highest	Present

Class-A Power amplifier :-

Depending on how the load is connected at the amplifier output, we have two types of class A power amplifiers as given below :

1. **Series-fed directly coupled Class A power amplifier.**
2. **Transformer-coupled Class A power amplifier.**

1. Series-fed directly coupled Class A power amplifier :-

→ The simple fixed-bias ckt connection shown in fig 1) can be used to discuss the main features of a class-A series fed amplifier.

→ R_C is the load which is connected in series with the collector, so the name series-fed ampl^r

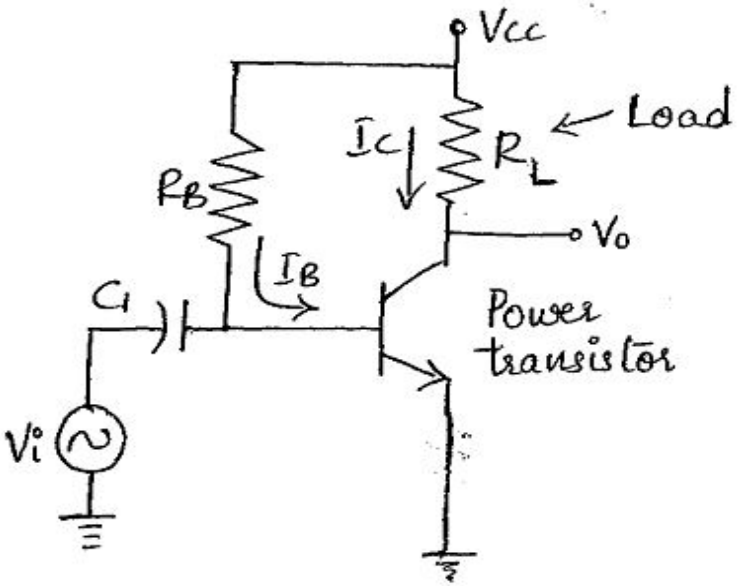


fig 1): Series-fed class A large signal amplifier.

DC Analysis :-

Applying KVL to the base loop

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$I_B = \frac{V_{CC} - 0.7V}{}$$ —— (1)

the collector current

$$I_C = \beta I_B$$ —— (2)

Applying KVL to the collector-emitter ckt,

$$V_{CC} = I_C R_L + V_{CE}$$

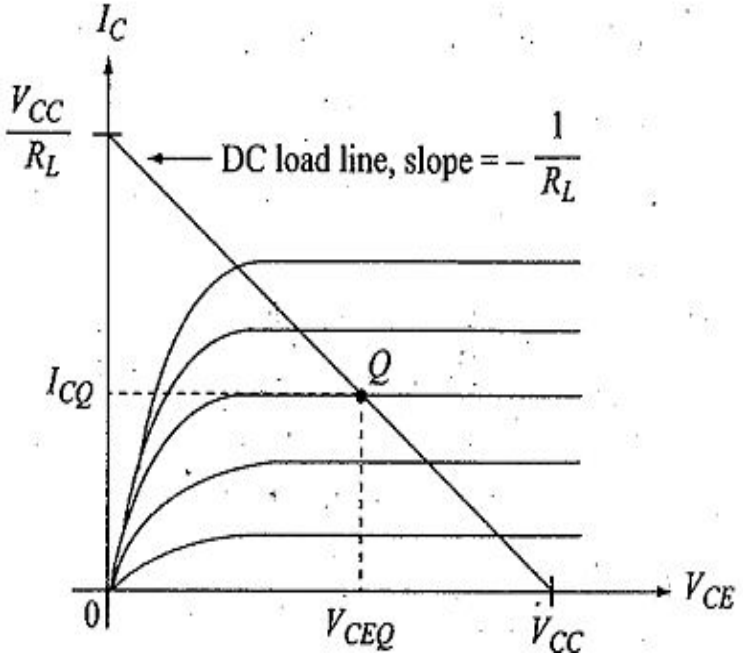
$$\therefore \boxed{I_C = \frac{V_{CC} - V_{CE}}{R_L}} \quad \text{—(3)}$$

$$\boxed{I_C = \frac{V_{CC}}{R_L} - \frac{V_{CE}}{R_L}}$$

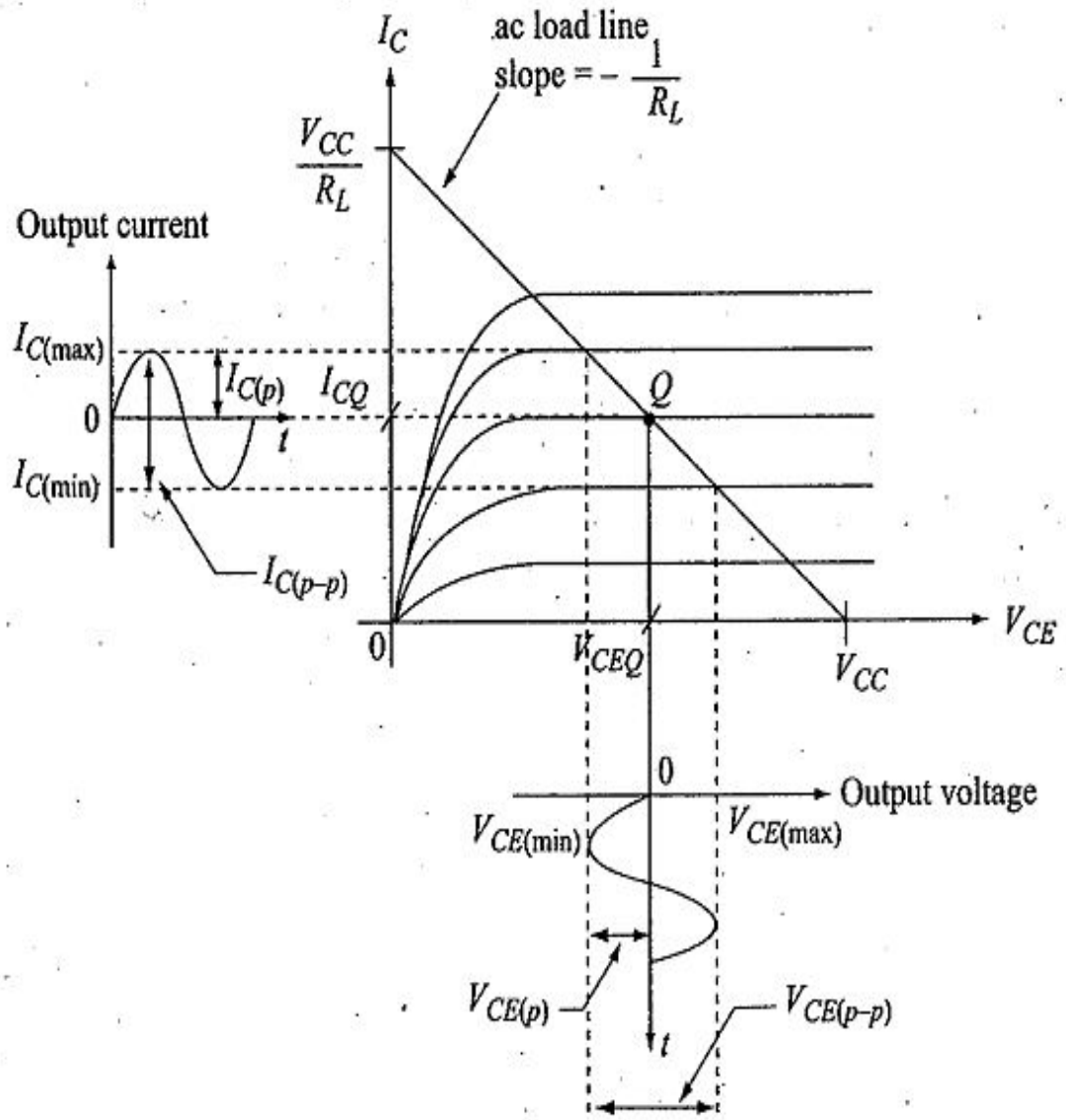
Eqn (3) can be written as

$$I_C = \left(-\frac{1}{R_L}\right) V_{CE} + \frac{V_{CC}}{R_L}$$

Thus, the slope of the dc load line is $\left(-\frac{1}{R_L}\right)$ & the intercept on the current axis is $\frac{V_{CC}}{R_L}$.



AC Analysis :-



→ In the ckt of fig(1), both the dc current & the ac current flows through the same load R_L connected in series with the collector.

→ Hence the ac load line is the same as the dc load line.

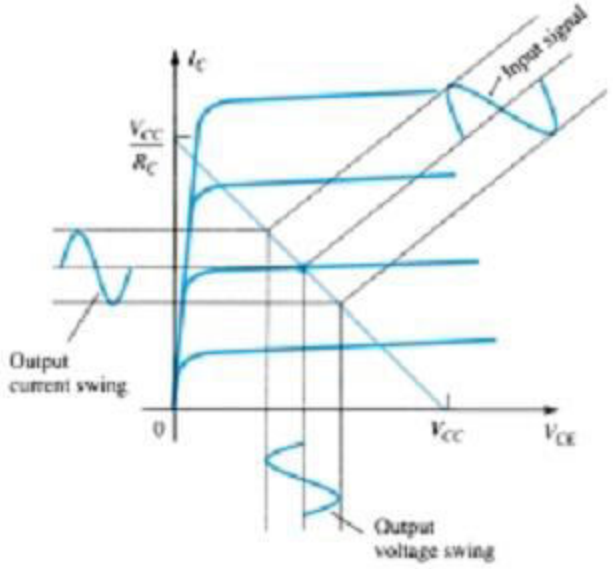
Hence the Q-point can be defined as $Q(V_{CEQ}, I_{CQ})$

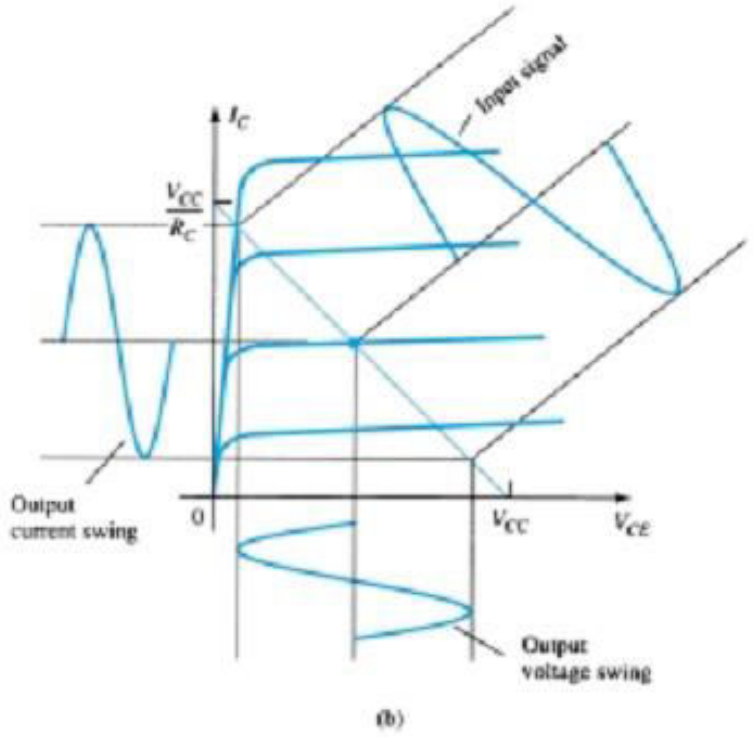
Power Consideration :-

* For the power amplifier, the input power is supplied from the dc source V_{cc}.
* With no i/p signal (ac signal), the dc current drawn is the collector bias current I_{cq}.

∴ The dc power i/p is given by

$$P_i(dc) = V_{cc} I_{cq}$$





(b)

Output Power (AC power o/p) :-

→ The ac signal V_i causes the base current to vary around the dc bias current & the collector current around its quiescent level I_{CQ}.

→ The ac i/p signal results in ac current & ac V$_{CE}$ signals.

→ The larger the i/p signal, the larger is the o/p swing.

The ac power delivered to the load (R_C) can be expressed in a no of ways :-

i) Using RMS signal values.

ii) Using peak signals values

iii) Using peak-to-peak signal values

iv) Using Maximum & minimum values.

Using RMS signals :-

The ac power delivered to the load (R_c) is given by

$$P_o(ac) = V_{CE(rms)} \cdot I_{C(rms)} \quad \text{—(1)}$$

$$\rightarrow \boxed{P_o(ac) = I^2_{C(rms)} \cdot R_L}$$

$$P_o(ac) = V_{CE(rms)} \cdot \frac{V_{CE(rms)}}{R_L}$$

$$\rightarrow \boxed{P_o(ac) = V^2_{CE(rms)} / R_L}$$

$$\boxed{V_{CE(rms)} = I_{C(rms)} \cdot R_L \qquad I_{C(rms)} = \frac{V_{CE(rms)}}{R_L}}$$

ii) Using peak signals :-

$$P_{o(ac)} = V_{CE(rms)} I_{C(rms)}$$

w.k.t

$$V_{rms} = \frac{V_m}{\sqrt{2}}$$

$$I_{rms} = \frac{I_m}{\sqrt{2}}$$

$$\rightarrow * \quad P_{o(ac)} = \frac{V_{CE(p)}}{\sqrt{2}} \cdot \frac{I_{C(p)}}{\sqrt{2}}$$

$$\boxed{P_{o(ac)} = \frac{V_{CE(p)} \cdot I_{C(p)}}{2}}$$

$$\rightarrow * \quad P_{o(ac)} = \frac{I_{C(p)} \cdot R_L \; I_{C(p)}}{2}$$

$$V_{CE(p)} = I_{C(p)} \times R_L$$

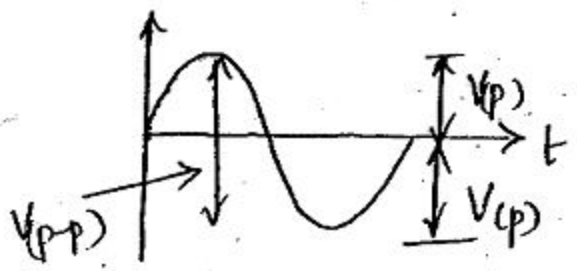
$$I_{C(p)} = \frac{V_{CE(p)}}{R_L}$$

$$\boxed{P_{o(ac)} = \frac{I_{C(p)}^2 \cdot R_L}{2}}$$

$$\rightarrow * \quad P_{o(ac)} = \frac{V_{CE(p)}}{2} \cdot \frac{V_{CE(p)}}{R_L}$$

$$\boxed{P_{o(ac)} = \frac{V_{CE(p)}^2}{2R_L}}$$

(iii) Using peak-to-peak signals :-



$$V_{(p-p)} = V_{(p)} + V_{(p)}$$

$$V_{(p-p)} = 2\,V_{(p)}$$

$$\boxed{V_{(p)} = \frac{V_{(p-p)}}{2}}$$

Also $I_{(p-p)} = I_{(p)} + I_{(p)}$

$$I_{(p-p)} = 2\,I_{(p)}$$

$$\boxed{I_{(p)} = \frac{I_{(p-p)}}{2}}$$

$$P_{o(ac)} = V_{CE(rms)} \cdot I_{C(rms)}$$

$$= \frac{V_{CE(p)}}{\sqrt{2}} \cdot \frac{I_{C(p)}}{\sqrt{2}}$$

$$= \frac{V_{CE(p)} \cdot I_{C(p)}}{2}$$

$$= \frac{V_{CE(p-p)}/2 \cdot I_{C(p-p)}/2}{2}$$

$$\boxed{P_{o(ac)} = \frac{V_{CE(p-p)} \cdot I_{C(p-p)}}{8}}$$

w.k.t

$$V_{CE(p)} = \frac{V_{CE(p-p)}}{2}$$

$$I_{C(p)} = \frac{I_{C(p-p)}}{2}$$

$$P_{o(ac)} = \frac{V_{CE(p-p)}}{8} \cdot \frac{V_{CE(p-p)}}{R_L}$$

$$\boxed{P_{o(ac)} = \frac{V^2_{CE(p-p)}}{8 \cdot R_L}}$$

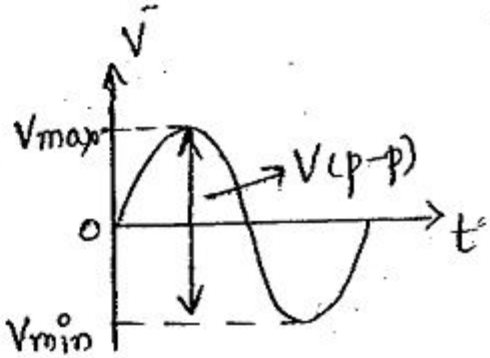
$$I_{C(p-p)} = \frac{V_{CE(p-p)}}{R_L}$$

$$V_{CE(p-p)} = I_{C(p-p)} \times R_L$$

$$P_{o(ac)} = I_{C(p-p)} \cdot R_L \cdot \frac{I_{C(p-p)}}{8}$$

$$\boxed{P_{o(ac)} = \frac{I^2_{C(p-p)} \cdot R_L}{8}}$$

iv) Using Maximum & Minimum Values :-



→ $V_{CE(p-p)} = V_{max} - V_{min}$

→ $I_{C(p-p)} = I_{max} - I_{min}$

$$P_{o(ac)} = \frac{V_{CE(p-p)} \cdot I_{C(p-p)}}{8}$$

$$\boxed{P_{o(ac)} = \frac{[V_{max} - V_{min}][I_{max} - I_{min}]}{8}}$$

Efficiency :-

The efficiency of an amplifier represents the amount of ac power delivered or transfered to the load, from the dc source.

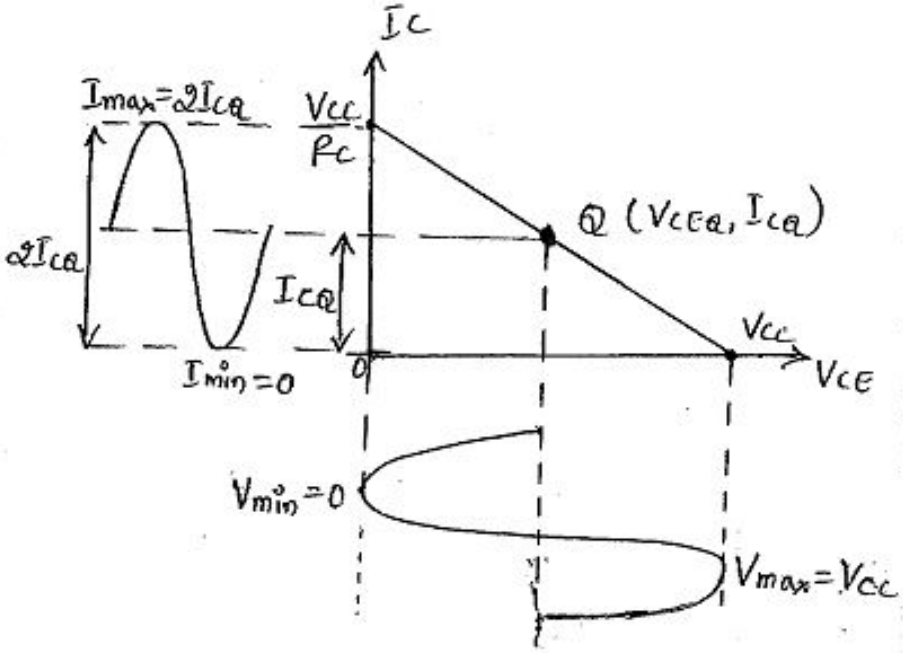
$$\% \eta = \frac{P_o\,(ac)}{P_i\,(dc)} \times 100\ \%$$

Maximum efficiency :-

For maximum swings

$V_{max} = V_{cc}$ & $V_{min} = 0$

$I_{max} = 2I_{CQ}$ & $I_{min} = 0$



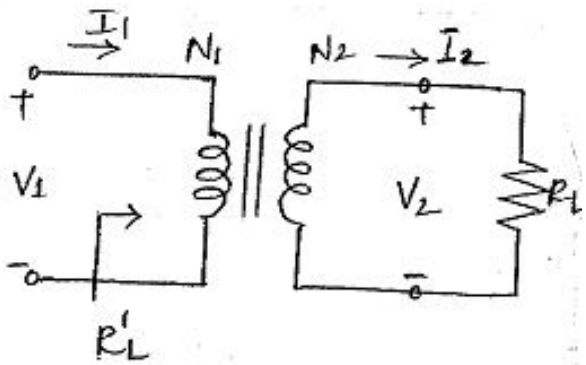
$\therefore$ Maximum $\% \eta = \dfrac{\text{maximum } P_o\,(ac)}{\text{maximum } P_i\,(dc)} \times 100\ \%$

$$= \frac{(V_{max} - V_{min})(I_{max} - I_{min})}{8\, V_{cc}\, I_{CQ}} \times 100\ \%$$

$$= \frac{V_{cc} \cdot 2 I_{CQ}}{4 \cdot 8 V_{cc} I_{CQ}} \times 100\ \%$$

Maximum $\%\eta = 25\ \%$

Properties of Transformer :-



→* While analysing the transformer, it is assumed that the transformer is ideal & there are no losses in the transformer.

→* Why the winding resistances are assumed to be zero.

let

$N_1 \rightarrow$ No of turns on primary

$N_2 \rightarrow$ No of turns on secondary

$V_1 \rightarrow$ Voltage applied to primary

$V_2 \rightarrow$ secondary voltage.

$I_1 \rightarrow$ primary current

$I_2 \rightarrow$ Secondary current.

i) Turns ratio :-

The ratio of no of turns on secondary to the no of turns on primary is called turns ratio of the transformer denoted by 'n'.

$$\frac{N_2}{N_1} : 1 \quad \text{or} \quad \frac{N_1}{N_2} : 1$$

ii) Voltage transformation :-

The transformer transforms the voltage applied on one side to other side proportional to the turns ratio. The transformer can be step up or step down transformer.

$$\frac{V_2}{V_1} = \frac{N_2}{N_1} = n \quad \text{---(1)} \Rightarrow \frac{V_1}{V_2} = \frac{N_1}{N_2}$$

iii) Current transformation :

$$\frac{I_2}{I_1} = \frac{N_1}{N_2} = \frac{1}{n} \quad \text{---(2)}$$

iv) Impedance Transformation :-

→ * Since the vtg & ct can be changed by a transformer, an impedance seen from either side can also be changed.

load on the secondary,

$$R_L = \frac{V_2}{I_2} \quad \text{—③}$$

& $$R_L' = \frac{V_1}{I_1} \quad \text{—④}$$

where R_L' is the load reflected at the primary.

Multiplying eq^ns ① & ②

$$\frac{V_1 I_2}{V_2 I_1} = \frac{N_1^2}{N_2^2} \quad \text{—⑤}$$

$$\frac{V_1/I_1}{V_2/I_2} = \left(\frac{N_1}{N_2}\right)^2 \quad \text{—⑥}$$

substituting eq^ns ③ & ④ in eq^n ⑥ we have

$$\frac{R_L'}{R_L} = \left(\frac{N_1}{N_2}\right)^2$$

or $$\boxed{R_L' = R_L \left(\frac{N_1}{N_2}\right)^2}$$ or $$\boxed{R_L' = \frac{R_L}{n^2}} \quad \text{—⑦}$$

$R_L' > R_L$ can be achieved by choosing $N_1 > N_2$ ie we have to use a step down transformer of appropriate turns ratio.

ADVANTAGES :-

- The efficiency of the operation is higher than directly coupled amplifier.
- The impedance matching required for maximum power transfer is possible.
- There is perfect isolation b/n the a.c power developed across the load & the d.c i/p power due to transformer.

DISADVANTAGES :-

- Due to the inductance of the transformer winding, the frequency response is poor compared to series-fed amplifier
- The circuit is bulky, heavy & costly due to the transformer.
- The designing of turns ratio & other parts of the ckt is complicated compared to series-fed ampl^r.

1. **Explain the operation of the transformer coupled class-A power amplifier. Prove that the maximum power efficiency is 50%.**

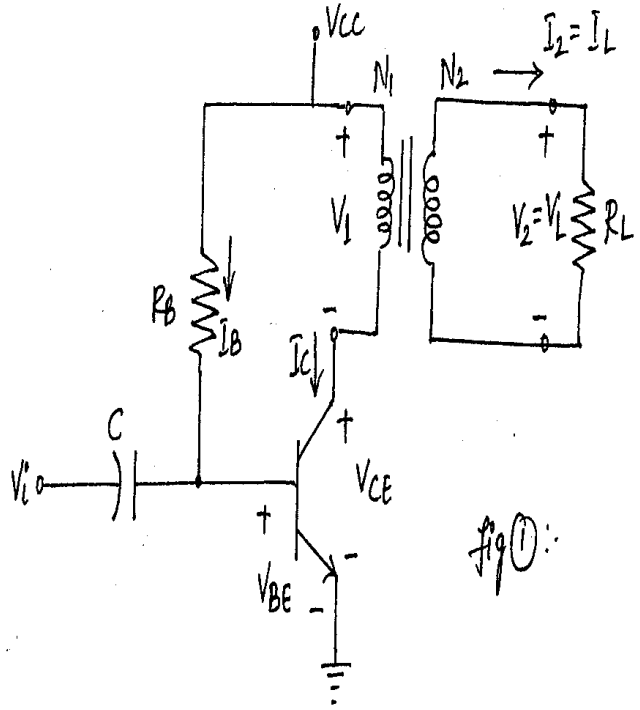


Fig ①:

DC Operation :-

→ It is assumed that the winding resistances are zero ohms.

→ There is no dc voltage drop across primary of transformer w.r.t the slope of dc load line is reciprocal of the d.c resistance in the collector ckt $\left(\frac{1}{R_{(dc)}} = \frac{1}{0} = \infty\right)$.

Applying KVL to the collector ckt

$$V_{CC} - V_{CE} = 0$$

$$\therefore V_{CC} = V_{CE}$$

$$\boxed{V_{CE_Q} = V_{CC}}$$ – This is the dc bias vtg V_{CEQ} for the transistor.

→ Hence the d.c load line is a vertical straight line passing through a v.lg point on the x-axis which is $V_{CE_Q} = V_{cc}$.

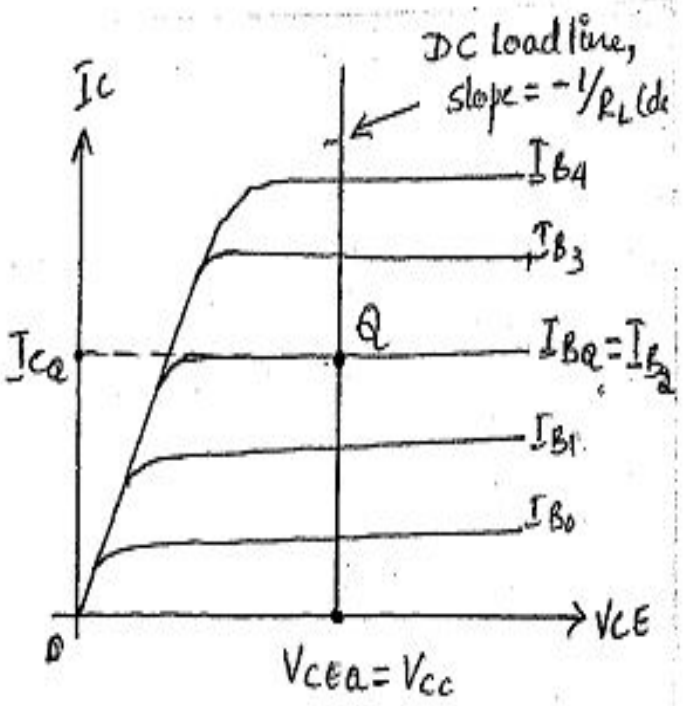


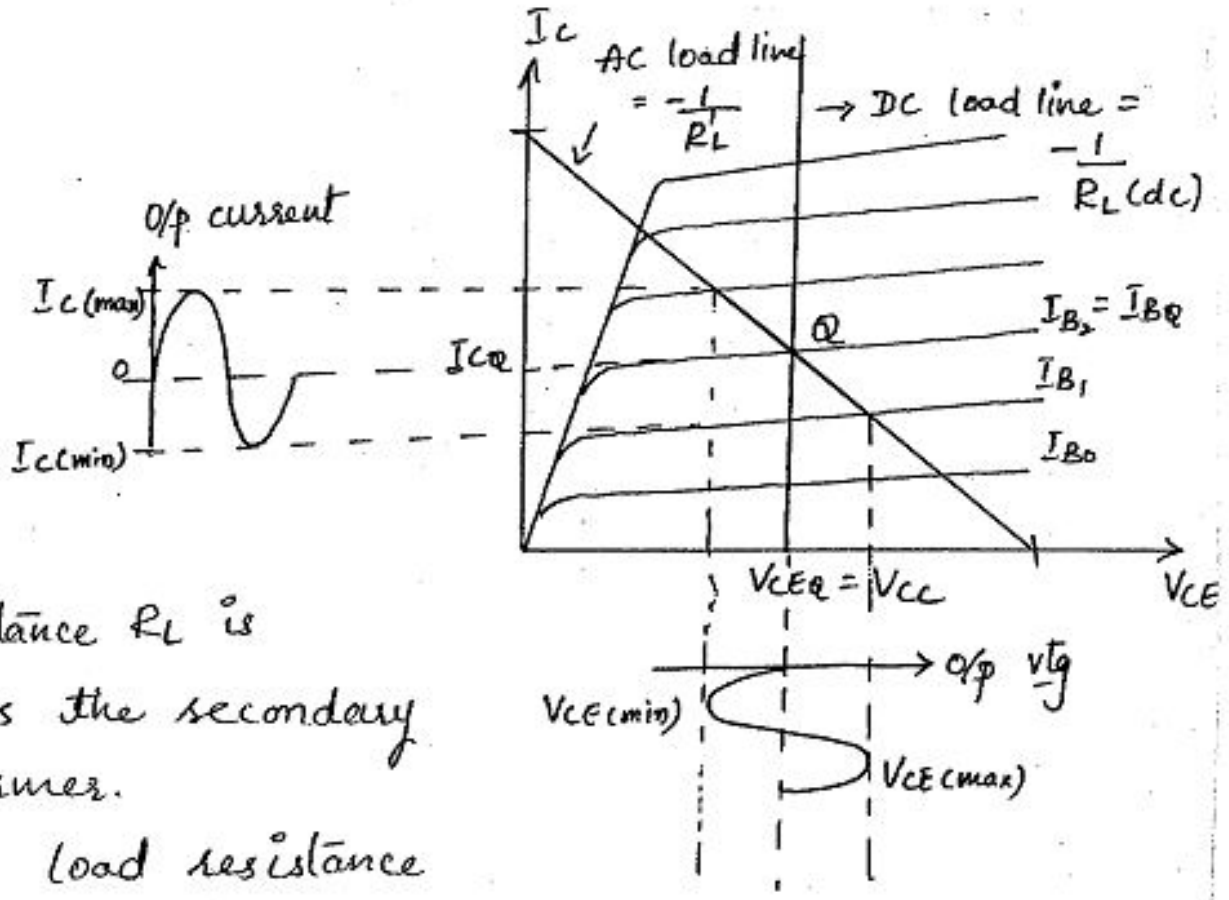
fig 2 : DC load line

DC I/P Power :-

The dc current drawn is collector bias current I_{CQ}

$$P_{i(dc)} = V_{cc} I_{CQ}$$

AC Analysis :-



→ The load resistance R_L is connected across the secondary of the Transformer.

→ The reflected load resistance R_L' is calculated using the formula

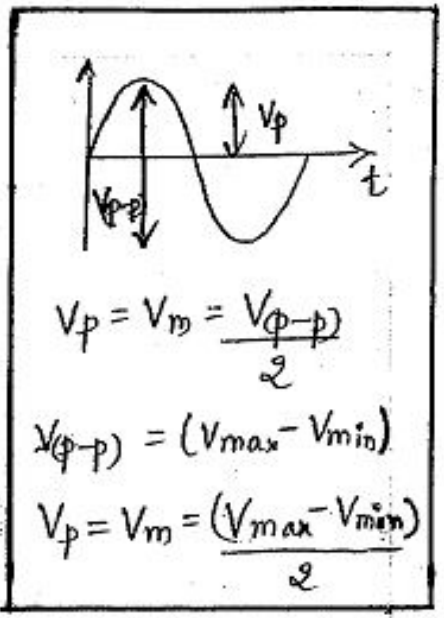
$$R_L' = \left(\frac{N_1}{N_2}\right)^2 R_L$$

Expression for AC O/P power :-

let

V_{1m} = peak value of primary voltage.

I_{1m} = peak value of primary current.



$V_p = V_m = \frac{V_{(p-p)}}{2}$

$V_{(p-p)} = (V_{max} - V_{min})$

$V_p = V_m = \frac{(V_{max} - V_{min})}{2}$

$$\rightarrow P_{ac} = \frac{V_{1m} \cdot I_{1m}}{2} \quad \text{---(1)}$$

$$V_{1m} = \frac{V_{(p-p)}}{2} \quad \& \quad I_{1m} = \frac{I_{(p-p)}}{2}$$

$$V_{1m} = \frac{(V_{max} - V_{min})}{2} \quad \& \quad I_{1m} = \frac{(I_{max} - I_{min})}{2} \quad \text{---(2)}$$

Substituting eq^n (2) in (1), we get

$$P_{ac} = \frac{1}{2} \cdot \frac{(V_{max} - V_{min})}{2} \cdot \frac{(I_{max} - I_{min})}{2}$$

$$\boxed{P_{ac} = \frac{(V_{max} - V_{min})(I_{max} - I_{min})}{8}}$$

Similarly the ac power delivered to the load or secondary can be calculated using secondary quantities.

let

V_{2m} = peak value of secondary or load v/g.

I_{2m} = peak value of secondary or load current.

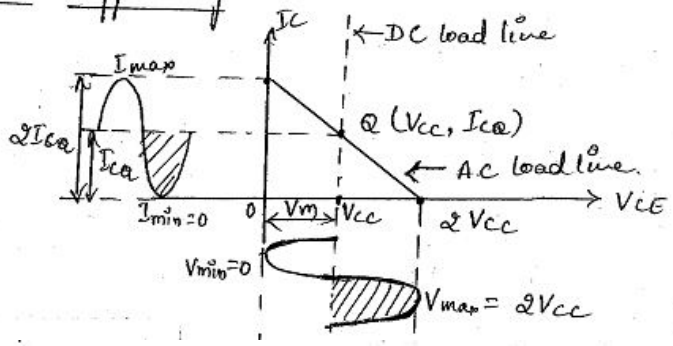
$$P_{ac} \doteq \frac{V_{2m} \cdot I_{2m}}{2}$$

$$P_{ac} = \frac{(V_{max} - V_{min})\,(I_{max} - I_{min})}{8}$$

$$\eta\,\% = \frac{P_{ac}}{P_{dc}} \times 100$$

$$\eta\,\% = \frac{(V_{max} - V_{min})\,(I_{max} - I_{min})}{8\,(V_{cc}.I_{cq})} \times 100.$$

Maximum Efficiency :-



Maximum Efficiency :-

For maximum η, P_{out} is also maximum.

$$\boxed{\begin{aligned} V_{max} &= 2V_{cc} \;\&\; V_{min} = 0 \\ I_{max} &= 2I_{cq} \;\&\; I_{min} = 0 \end{aligned}}$$

$$\eta\,\% = \frac{P_{ac}}{P_{dc}} \times 100 = \frac{(V_{max} - V_{min}).(I_{max} - I_{min})}{8.V_{cc}.I_{cq}} \times 100\,\%$$

$$= \frac{2V_{cc}.2I_{cq}}{8\,V_{cc}.I_{cq}} \times 100\,\%$$

$$= \frac{4}{8/2} \times 100\,\%$$

$$\therefore \boxed{\eta\,\% = 50\,\%}$$

Maximum theoretical efficiency :-

$$\%\eta = 50\left(\frac{V_{CE_{max}} - V_{CE_{min}}}{V_{CE_{max}} + V_{CE_{min}}}\right)^{2}\ \%$$

ADVANTAGES :-

- The efficiency of the operation is higher than directly coupled amplifier.
- The impedance matching required for maximum power transfer is possible.
- There is perfect isolation b/n the a.c power developed across the load & the d.c i/p power due to transformer.

DISADVANTAGES :-

- Due to the inductance of the transformer winding, the frequency response is poor compared to series-fed amplifier.
- The circuit is bulky, heavy & costly due to the transformer.
- The designing of turns ratio & other parts of the ckt is complicated compared to series-fed ampl^{r}.

Class B-POWER AMPLIFIERS

Class-B power Amplifiers :-

→ In class B amplifier the collector current flows only for a half cycle of the full cycle i/p signal.

→ To get a full cycle across the load, a pair of transistors are used in Class-B operation.

→ The two transistors conduct in alternate half cycles of the i/p signal & a full cycle is obtained across the load.

→ The two transistors are identical in characteristics & are called matched transistors.

→ Depending upon the types of the two transistors, ie p-n-p or n-p-n, there are two types of class-B amplifiers :-

1) Puss-pull Class-B → where the transistors are of same type ie. either p-n-p or n-p-n.

2) Complementary symmetry Class-B → where the two transistors form a complementary pair ie. one n-p-n & other p-n-p.

2. Draw the circuit diagram and explain the operation with relevant waveforms of class-B push pull amplifier. Also show that the maximum conversion efficiency of class-B push-pull amplifier is 78.5%.

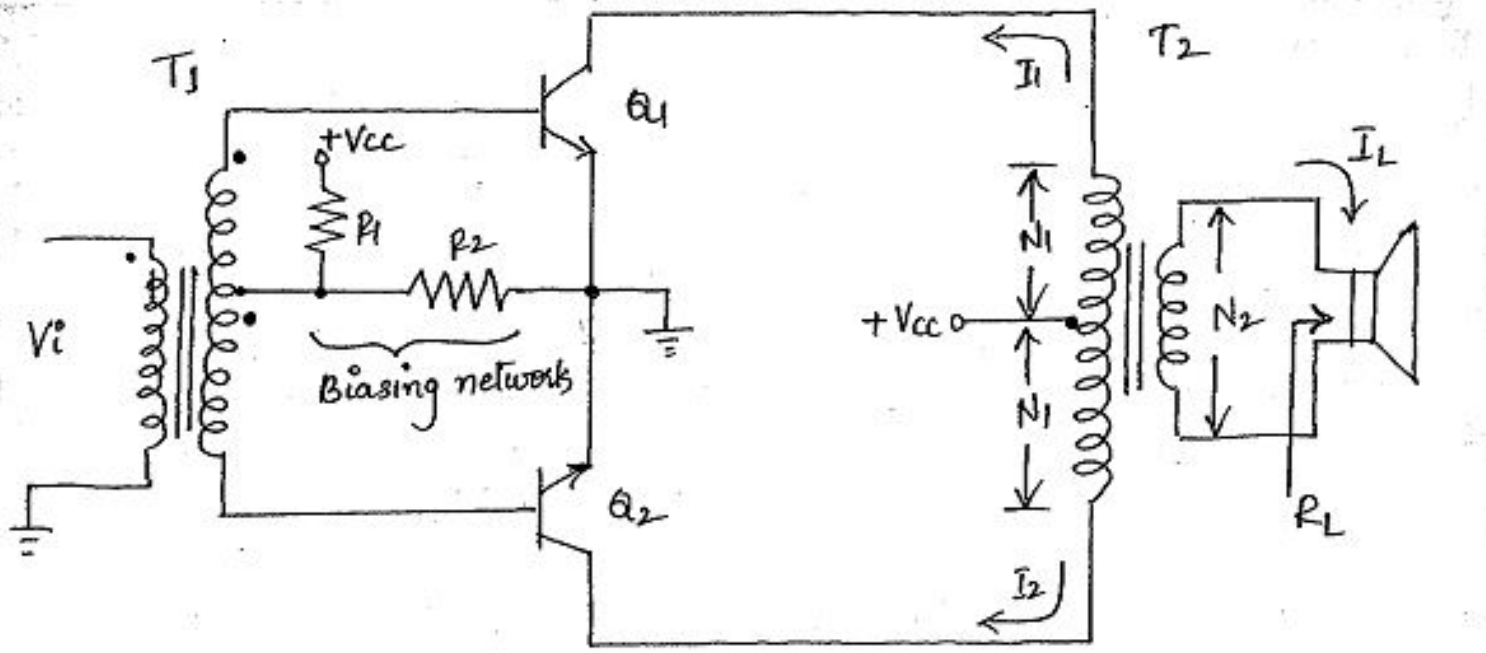
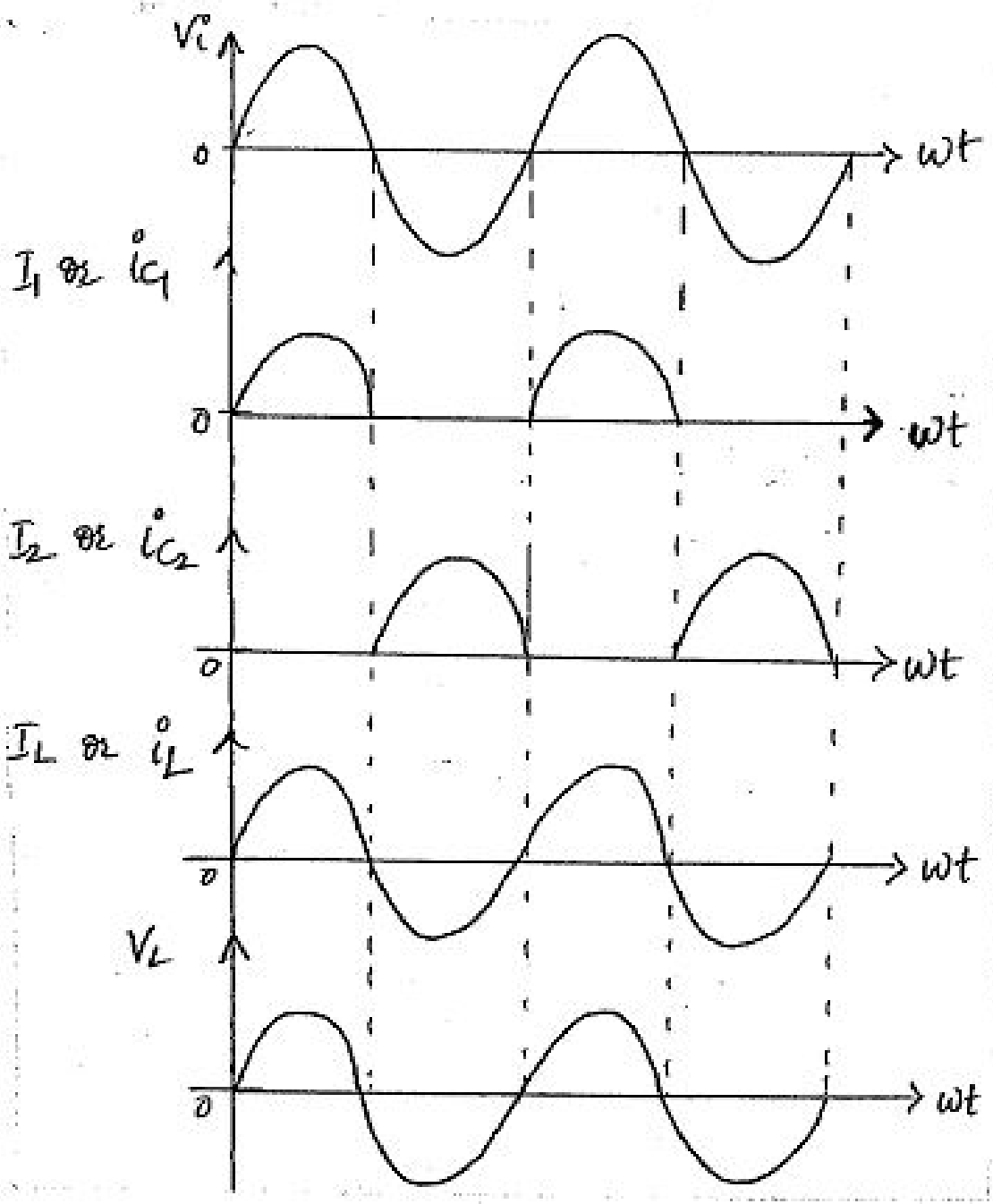


fig ① : Class-B Push-pull amplifier ckt.


V_i
0
ωt
I_1 or i_{C_1}
0
ωt
I_2 or i_{C_2}
0
ωt
I_L or i_L
0
ωt
V_L
0
ωt

→ The circuit consists of
i) Two-centre tapped transformer (T_1 & T_2)
ii) Two identical transistors Q_1 & Q_2 (n-pn)

→ The transformer 'T_1' is an i/p transformer & is called phase splitter. It is required to produce two signal voltages, which are 180° out of phase with each other.

→ These two signal voltages, with opposite polarity, drive the i/p of transistor Q_1 & Q_2. (i_{b_1} & i_{b_2})

→ The transformer 'T_2' is an o/p transformer & is required to couple a.c o/p signal from the collector to load.

Operation :-

→ During +ve half cycle of the i/p signal, the base of transistor Q_1 is +ve & that of Q_2 is -ve. As a result of this, Q_1 conducts, while the transistor Q_2 is OFF.

→ When the i/p signal goes -ve, Q_1 turns OFF & Q_2 conduct Thus, at an instant, only one transistor in the circuit conducts.

→ Each transistor handles one-half of the i/p signal.

→ The o/p transformer joins these two half-signals & produces a full-cycle in the load.

→ However it has been found that joining of o/ps of two transistors is never perfect & hence the o/p is distorted.

→ The load current is given by

$$\boxed{I_L = I_1 - I_2} \quad \text{or} \quad \boxed{i_L = i_{C_1} - i_{C_2}}$$

→ During one half cycle, one part of the circuit pushes the signal high & during other half cycle, the other part pulls the signal low. Hence the name push-pull ampl^{r}.

→ The class-B push pull ampl^{r} is known as double ended class-B ampl^{r}.

ADVANTAGES :-

1) The efficiency is higher than class A amplifier (78.5 %)
2) When there is no i/p signal, the power dissipation is zero.
3) Impedance matching can be achieved perfectly due to the presence of o/p transformer.
4) Even harmonics are absent in the o/p. This reduces harmonic distortion.
5) Because of the absence of even harmonics in the o/p, the ckt gives more o/p power per transistor for a given amount of distortion.

DISADVANTAGES :-

1) Two centre-tap transformers are necessary.
2) The transformers make the circuit bulky, heavy & costlier compared to other power amplifiers.
3) Frequency response is poor due to the presence of inductance of the transformers.
4) It is difficult to find the exact centre-tap in the two transformers.

DC operation :-

→* The dc biasing point ie Q-point is adjusted on the x-axis such that $V_{CEQ} = V_{cc}$ & $I_{CEQ} = 0$.

→* Hence co-ordinates of the Q-point are $(V_{cc}, 0)$

DC power i/p :-

→* Each transistor o/p is in the form of half rectified sinusoid with a peak value of I_m or $I_{c(p)}$.

→* Thus the average current in each transistor is $\frac{I_m}{\pi}$.

→* Since there are two transistors, the dc current drawn from the supply V_{cc}, by both the Transistors is

$$I_{dc} = 2 (\text{average current in each transistor})$$

$$\therefore \boxed{I_{dc} = \frac{2 I_m}{\pi}}$$

The dc power i/p to the power amplifier is given by

$$P_{i(dc)} = V_{cc} \cdot I_{dc}$$

$$P_{i(dc)} = V_{cc} \left(\frac{2 I_m}{\pi}\right)$$

$$\boxed{P_{i(dc)} = \frac{2}{\pi} \cdot V_{cc} \cdot I_m}$$

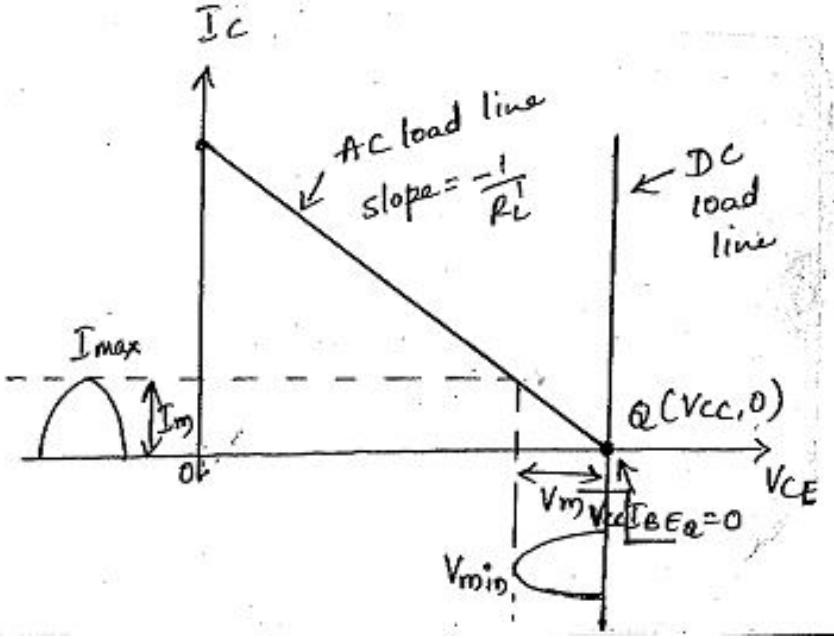
AC operation :-

The a.c power o/p is given by

$$P_{ac} = V_{rms} \cdot I_{rms}$$

$$= \frac{V_m}{\sqrt{2}} \cdot \frac{I_m}{\sqrt{2}}$$

$$\boxed{P_{ac} = \frac{V_m \cdot I_m}{2}}$$



$$P_{ac} = \frac{V_m}{2} \cdot \frac{V_m}{R_L'}$$

OR

$$P_{ac} = I_m R_L' \cdot \frac{I_m}{2}$$

$$\boxed{P_{ac} = \frac{V_m^2}{2 R_L'}}$$

$$\boxed{P_{ac} = \frac{I_m^2}{2} \cdot R_L'}$$

Efficiency :-

$$\% \eta = \frac{P_{ac}}{P_{dc}} \times 100$$

$$= \frac{\frac{V_m \cdot I_m}{2}}{V_{cc} \cdot \frac{2 I_m}{\pi}} \times 100$$

$$\% \eta = \frac{V_m}{2} \cdot \frac{1}{\frac{2 V_{cc}}{\pi}} \times 100$$

$$\boxed{\% \eta = \frac{V_m \cdot \pi}{4 V_{cc}} \times 100}$$

Maximum Efficiency :-

$V_m = V_{CC}$ → for maximum efficiency.

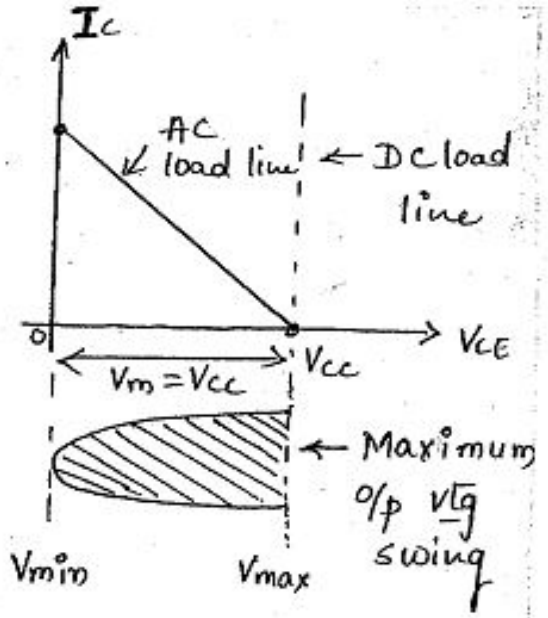
$$\% \eta = \frac{V_m \cdot \pi}{4 V_{CC}} \times 100$$

w.k.t $V_m = V_{max} - V_{min}$

$= V_{CC} - 0$

$V_m = V_{CC}$

$$\% \eta_{max} = \frac{V_{CC} \cdot \pi}{4 V_{CC}} \times 100$$



$$\% \eta_{max} = \pi/4 \times 100$$

$$\boxed{\% \eta_{max} = 78.5\ \%}$$

Power dissipation :-

$$P_d = P_{dc} - P_{ac}$$

$$= \frac{2}{\pi} V_{cc} . I_m - \frac{V_m I_m}{2}$$

w.k.t

$$P_{dc} = \frac{2}{\pi} V_{cc} . I_m$$

$$P_{ac} = \frac{V_m . I_m}{2}$$

w.k.t $I_m = V_m / R_L'$

$$P_d = \frac{2 V_{cc} . V_m}{\pi R_L'} - \frac{V_m}{2} \cdot \frac{V_m}{R_L'}$$

$$\boxed{P_d = \frac{2}{\pi} \cdot \frac{V_{cc} . V_m}{R_L'} - \frac{V_m^2}{2 R_L'}} \quad \text{—— (1)}$$

→ In Class A amplifier power dissipation is maximum when there is no i/p signal.

→ But in Class B amplifier, when i/p signal is zero, $V_m = 0$ hence the power dissipation is zero & not maximum.

Maximum Power dissipation :-

→ The condition for maximum power dissipation can be obtained by differentiating the eqn (1) w.r.t V_m & equating it to zero.

$$P_d = \frac{2}{\pi} \cdot \frac{V_{cc} V_m}{R_L'} - \frac{V_m^2}{2 R_L'}$$

$$\hookrightarrow \frac{dP_d}{dV_m} = \frac{2}{\pi} \frac{V_{cc}}{R_L'} - \frac{2 V_m}{2 R_L'} = 0$$

$$\frac{2V_{cc}}{\pi R_L'} = \frac{2V_m}{2R_L'}$$

$$V_m = \frac{2V_{cc}}{\pi} \cdot \frac{R_L'}{R_L'}$$

$$\boxed{V_m = \frac{2}{\pi} V_{cc}} \quad -(22)$$

→ This is the condition for maximum power dissipation

Substituting eq^n (22) in eq^n (1)

$$(P_d)_{max} = \frac{2V_{cc}}{\pi R_L'} \cdot \frac{2V_{cc}}{\pi} - \left(\frac{2V_{cc}}{\pi}\right)^2 \cdot \frac{1}{2R_L'}$$

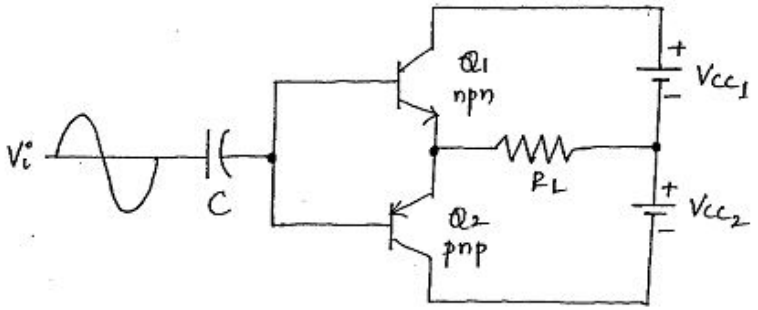
$$= \frac{4}{\pi^2} \cdot \frac{V_{cc}^2}{R_L'} - \frac{2}{\pi^2} \frac{4V_{cc}^2}{2R_L'} \cdot \frac{1}{2R_L'}$$

$$= \frac{4}{\pi^2} \cdot \frac{V_{cc}^2}{R_L'} - \frac{2}{\pi^2} \cdot \frac{V_{cc}^2}{R_L'}$$

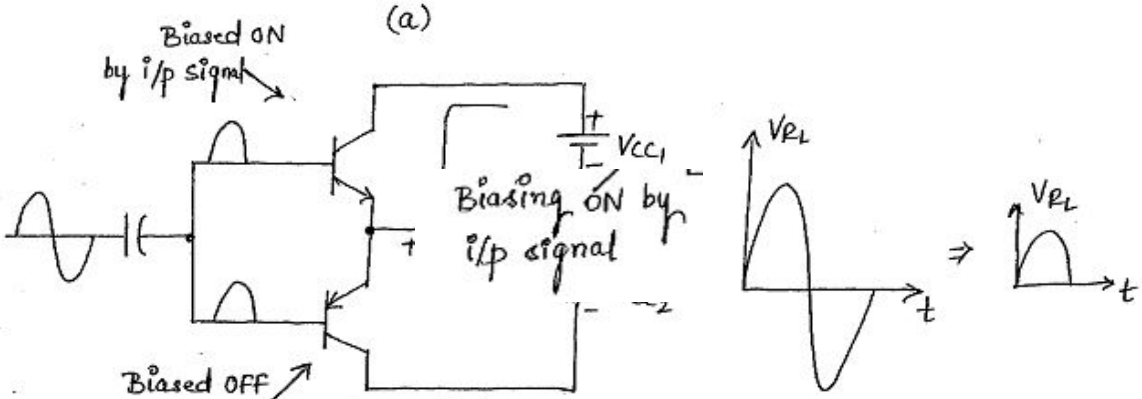
$$\boxed{(P_d)_{max} = \frac{2}{\pi^2} \cdot \frac{V_{cc}^2}{R_L'}}$$

❖ COMPLEMENTARY Symmetry Class B Amplifier :-

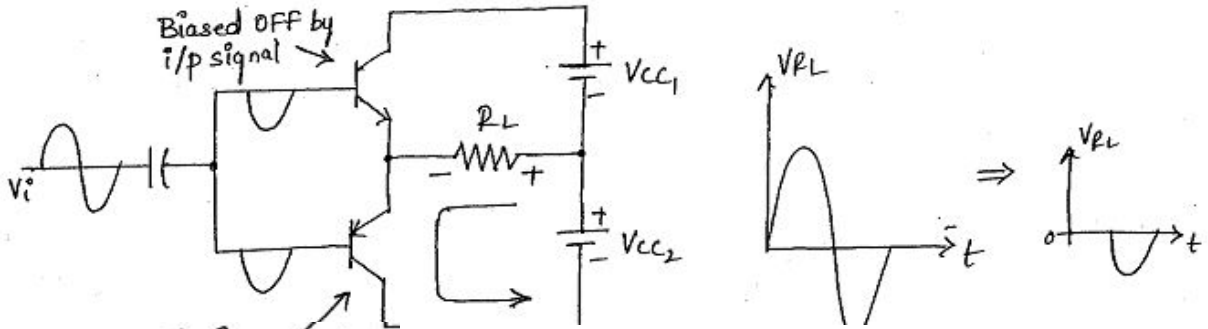
(Common collector-emitter follower)

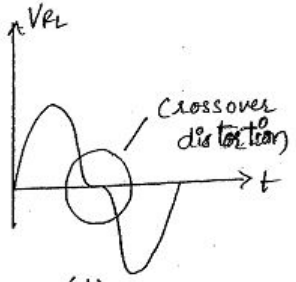


(a)



(b)





→ In complementary symmetry Class B amplifier, one is n-p-n and the other is p-n-p transistor.

→ The transistor Q_1 is n-p-n while Q_2 is p-n-p type.

→ The circuit is driven from a dual supply of $\pm V_{cc}$.

→ During +ve half cycle of the i/p signal, the transistor Q_1 will be biased into conduction, resulting in a half cycle signal across the load.

→ During -ve half cycle of the i/p signal, the p-n-p transistor Q_2 will be biased into conduction resulting in -ve half cycle across the load R_L.

→ Thus for a complete cycle of i/p, a complete cycle of o/p signal is obtained across the load.

Mathematical Analysis :-

→ All the results derived for Push-pull transformer coupled Class-B amplifier are applicable to the complementary Class B amplifier.

→ The only change is that as the o/p transformer is not present, hence in the expressions, R_L value must be used as it is, instead of R'_L.

Advantages :-

1> As the circuit is transformerless, its weight, size & cost are less.

2> Due to common collector configuration, impedance matching is possible.

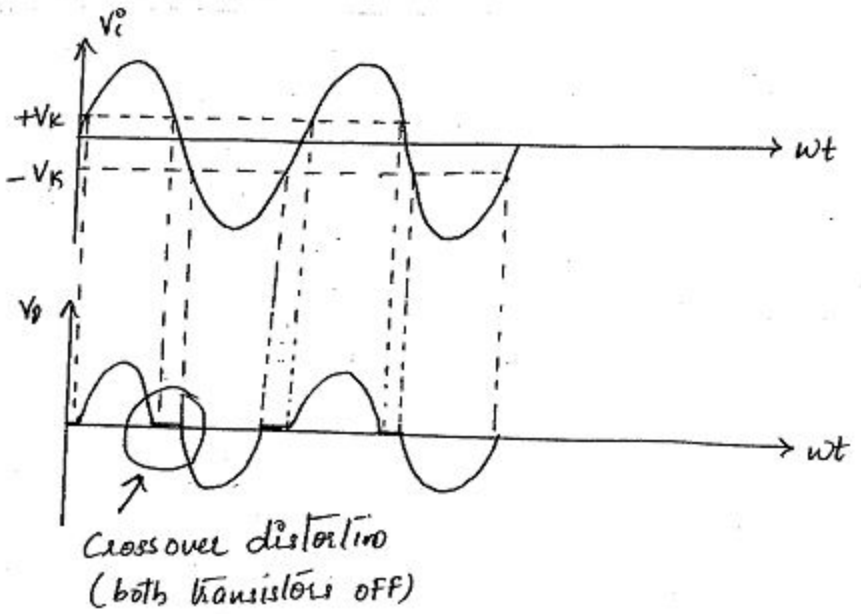
3> The frequency response improves due to transformerless Class B amplifier ckt.

Disadvantages :-

1> The circuit needs two separate voltage supplies.

2> The o/p is distorted to cross-over distortion.

Cross-over distortion :-



→ For a transistor to be in active region the base emitter-junction must be forward biased.

→ The junction is cannot be forward biased till the voltage applied becomes greater than cut-in vtg (V_K) of the junction, which is generally 0.7V for silicon & 0.2 V for Ge.

→ Thus when i/p is less than 0.7V, the base-emitter junction is reverse biased, the collector current remain zero & transistor remains in cut-off region.

→ Hence there is a period b/n the crossing of the half cycles of the i/p signal, for which none of the transistors is active & the o/p is zero.

→ Hence the o/p signal gets distorted.

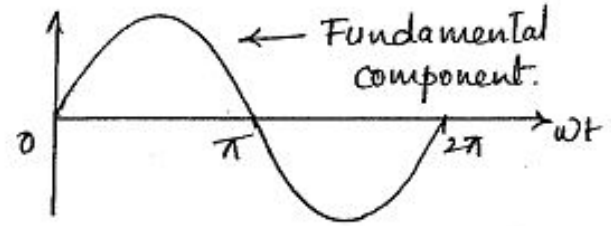
→ Such distortion in the o/p signal is called cross-over distortion.

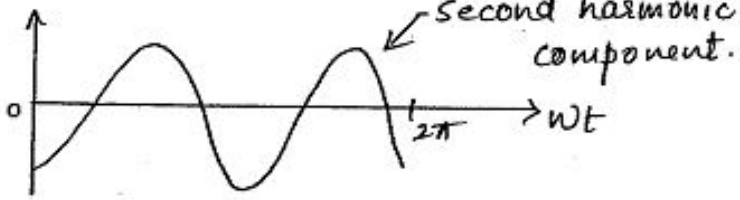
→ Due to cross-over distortion each transistor conducts for less than a half cycle rather than the complete half cycle.

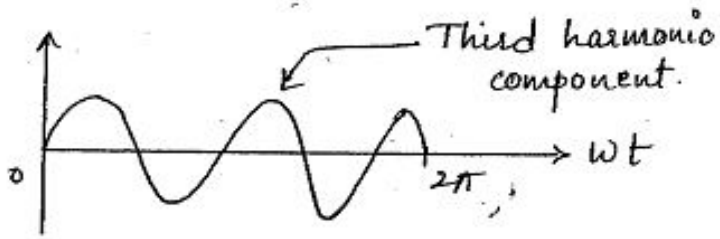
Comparision of Push Pull and Complementary symmetry circuits :-

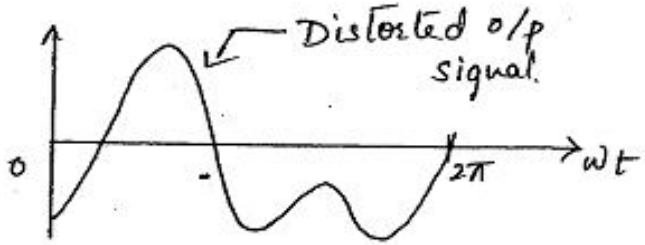
Sl No.	Push Pull Class B	Complementary symmetry class B
1.	**Both** the **transistors** are **either *p-n-p*** or ***n-p-n***.	**Transistors** are **complementary** type i.e. **one *n-p-n*** and **other *p-n-p***.
2.	The **transformer** is **used** to connect the load as well as input.	The circuit is **transformer less**.
3.	The **impedance matching** is **possible** due to the output **transformer**.	The impedance matching is possible due to **common collector circuit**.
4.	Frequency response is **poor**	Frequency response is **improved**
5.	Due to transformers, the circuit is **bulky**, **costly** and **heavier**.	As transformer less, the circuit is **not bulky** and **less costly**.
6.	**Dual power** supply is **not required**.	**Dual power** supply is **required**.
7.	The **efficiency** is **higher** than **class A** i.e **78.5%**	The **efficiency** is **higher** than the **push pull** i.e **>78.5%**
8.	Circuit is **complicated**	Circuit is **simple**.

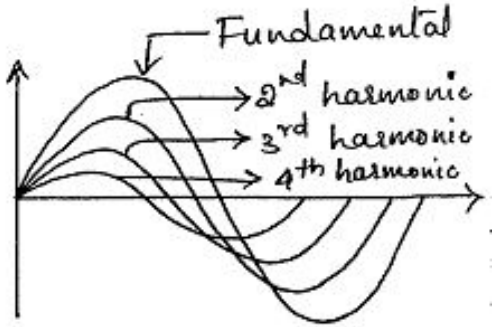
Harmonic distortion :-











→ The presence of frequency components in the o/p waveform which are not present in the i/p signal is called as harmonic distortion.

→ The component with frequency same as i/p signal is called fundamental frequency.

→ Additional frequency components which are integer multiples of fundamental frequency are called harmonics.

→ The fourier analysis of the o/p signal reveals that as the order of the harmonic increases, its amplitude decreases & frequency increases.

Expression for % harmonic distortion :-

→ In general.

% n^{th} harmonic distortion is given by

$$\% D_n = \frac{\text{Magnitude of } n^{th} \text{ harmonic component}}{\text{Magnitude of fundamental.}} \times 100$$

$$D_n = \frac{|B_n|}{|B_1|} \times 100\ \%$$

where B_1 → amplitude of the fundamental frequency component.

B_n → amplitude of the n^{th} frequency component.

Eg → % second harmonic distortion is given by

$$D_2 = \frac{|B_2|}{|B_1|} \times 100\ \%$$

→ Total harmonic distortion

$$THD = \sqrt{D_2^2 + D_3^2 + \ldots D_n^2} \times 100\ \%$$

15.5 DISCRETE TRANSISTOR VOLTAGE REGULATION

Two types of transistor voltage regulators are the series voltage regulator and the shunt voltage regulator. Each type of circuit can provide an output dc voltage that is regulated or maintained at a set value even if the input voltage varies or if the load connected to the output changes.

Series Voltage Regulation

The basic connection of a series regulator circuit is shown in the block diagram of Fig. 15.12. The series element controls the amount of the input voltage that gets to the output.

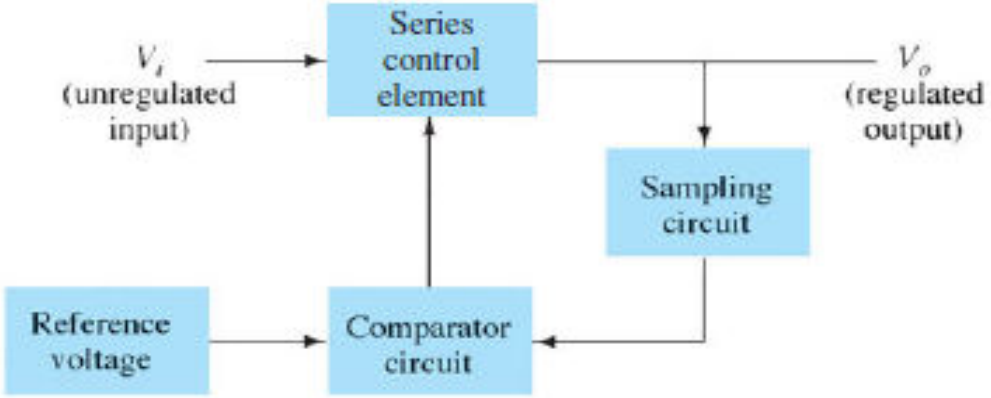


FIG. 15.12
Series regulator block diagram.

The output voltage is sampled by a circuit that provides a feedback voltage to be compared to a reference voltage.

1. If the output voltage increases, the comparator circuit provides a control signal to cause the series control element to decrease the amount of the output voltage—thereby maintaining the output voltage.
2. If the output voltage decreases, the comparator circuit provides a control signal to cause the series control element to increase the amount of the output voltage.

Series Regulator Circuit A simple series regulator circuit is shown in Fig. 15.13. Transistor Q_1 is the series control element, and Zener diode D_Z provides the reference voltage. The regulating operation can be described as follows:

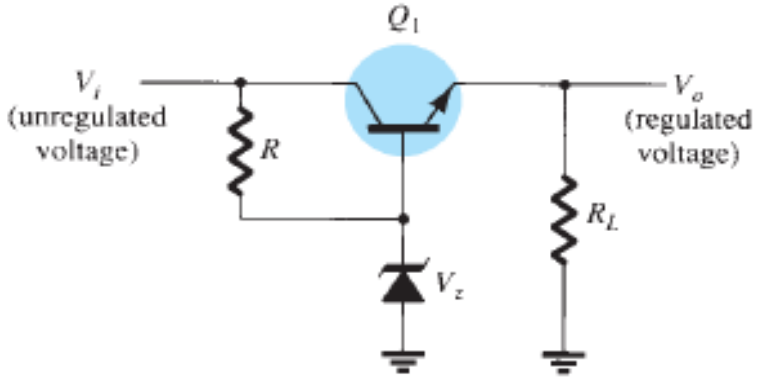


FIG. 15.13
Series regulator circuit.

1. If the output voltage decreases, the increased base-emitter voltage causes transistor Q_1 to conduct more, thereby raising the output voltage—maintaining the output constant.
2. If the output voltage increases, the decreased base-emitter voltage causes transistor Q_1 to conduct less, thereby reducing the output voltage—maintaining the output constant.

EXAMPLE 15.8 Calculate the output voltage and the Zener current in the regulator circuit of Fig. 15.14 for $R_L = 1\ \text{k}\Omega$.

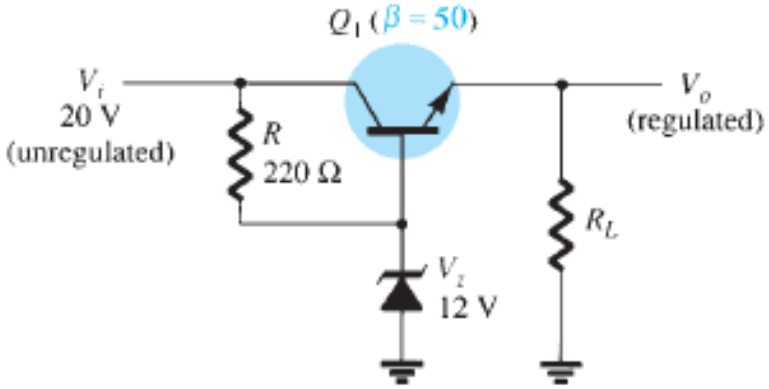


FIG. 15.14
Circuit for Example 15.8.

Solution:

$$V_o = V_Z - V_{BE} = 12\ \text{V} - 0.7\ \text{V} = \mathbf{11.3\ V}$$
$$V_{CE} = V_i - V_o = 20\ \text{V} - 11.3\ \text{V} = 8.7\ \text{V}$$
$$I_R = \frac{20\ \text{V} - 12\ \text{V}}{220\ \Omega} = \frac{8\ \text{V}}{220\ \Omega} = 36.4\ \text{mA}$$

For $R_L = 1\ \text{k}\Omega$,

$$I_L = \frac{V_o}{R_L} = \frac{11.3\ \text{V}}{1\ \text{k}\Omega} = 11.3\ \text{mA}$$

Shunt Voltage Regulation

A shunt voltage regulator provides regulation by shunting current away from the load to regulate the output voltage. Figure 15.20 shows the block diagram of such a voltage regulator. The input unregulated voltage provides current to the load. Some of the current is pulled away by the control element to maintain the regulated output voltage across the load. If the load voltage tries to change due to a change in the load, the sampling circuit provides

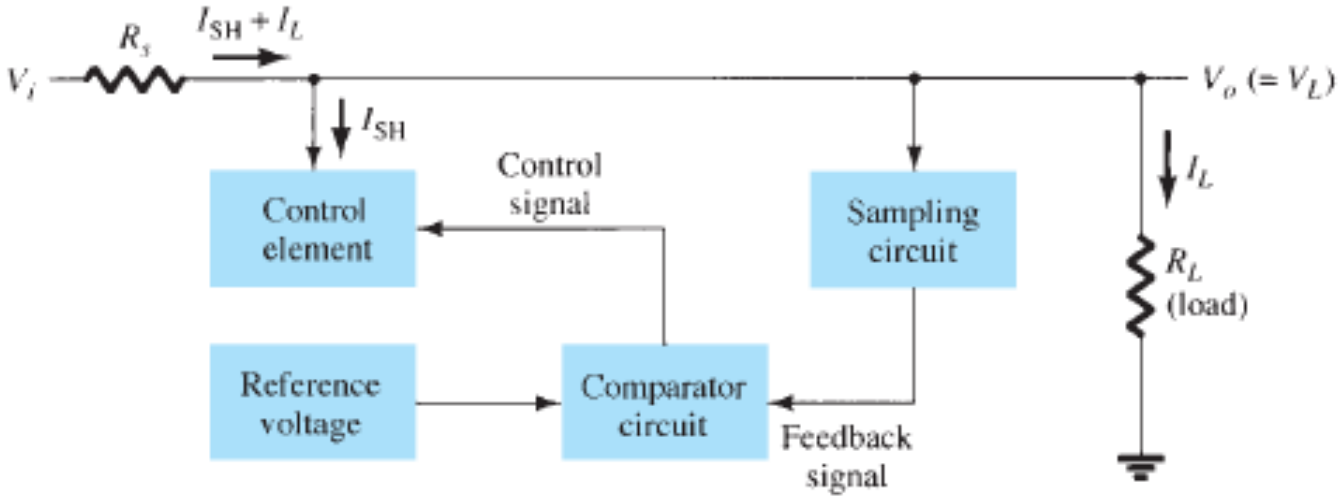


FIG. 15.20

Block diagram of shunt voltage regulator.

a feedback signal to a comparator, which then provides a control signal to vary the amount of the current shunted away from the load. As the output voltage tries to get larger, for example, the sampling circuit provides a feedback signal to the comparator circuit, which then provides a control signal to draw increased shunt current, providing less load current, thereby keeping the regulated voltage from rising.

Basic Transistor Shunt Regulator A basic shunt regulator circuit is shown in Fig. 15.21. Resistor R_S drops the unregulated voltage by an amount that depends on the current supplied to the load R_L. The voltage across the load is set by the Zener diode and transistor base-emitter voltage. If the load resistance decreases, a reduced drive current to the base of Q_1 results, shunting less collector current. The load current is thus larger, thereby maintaining the regulated voltage across the load. The output voltage to the load is

$$V_L = V_Z + V_{BE} \tag{15.19}$$

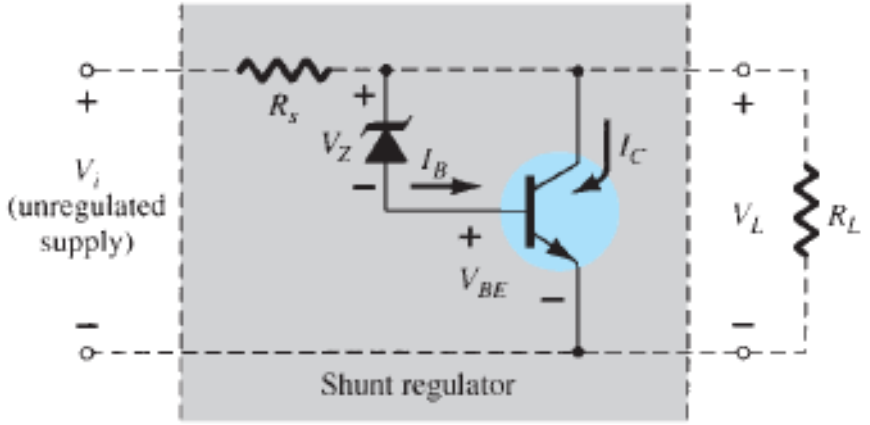


FIG. 15.21
Transistor shunt voltage regulator.

EXAMPLE 15.11 Determine the regulated voltage and circuit currents for the shunt regulator of Fig. 15.22.

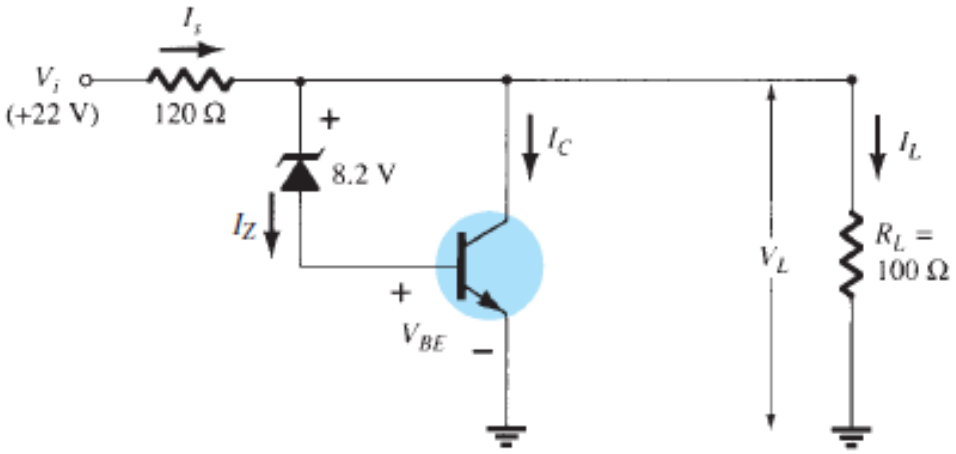


FIG. 15.22
Circuit for Example 15.11.

Solution: The load voltage is

$$\text{Eq. (15.19):} \quad V_L = 8.2\,\text{V} + 0.7\,\text{V} = \mathbf{8.9\,V}$$

For the given load,

$$I_L = \frac{V_L}{R_L} = \frac{8.9\,\text{V}}{100\,\Omega} = \mathbf{89\,mA}$$

With the unregulated input voltage at 22 V, the current through R_S is

$$I_S = \frac{V_i - V_L}{R_S} = \frac{22\,\text{V} - 8.9\,\text{V}}{120} = \mathbf{109\,mA}$$

so that the collector current is

$$I_C = I_S - I_L = 109\,\text{mA} - 89\,\text{mA} = \mathbf{20\,mA}$$