Analog Electronics (15EC32)

Module-2. Field Effect Transistors Class : III Sem

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Field Effect Transistors: Construction and Characteristics of JFETs, Transfer Characteristics, Depletion type MOSFET, Enhancement type MOSFET.
FET Amplifiers: JFET small signal model, Fixed bias configuration, Self bias configuration, Voltage divider configuration, Common Gate configuration. Source- Follower Configuration, Cascade configuration.

Objectives

- Become familiar with the construction and operating characteristics of Junction Field Effect (JFET), Metal-Oxide Semiconductor FET (MOSFET), and Metal-Semiconductor FET (MESFET) transistors.
- Be able to sketch the transfer characteristics from the drain characteristics of a JFET and MOSFET.
- Understand the vast amount of information provided on the specification sheet for each type of FET.
- Be aware of the differences between the dc analysis of the various types of FETs.

The field-effect transistor (FET) is a three-terminal device used for a variety of applications that match, to a large extent, those of the BJT transistor.
Although there are important differences between the two types of devices, there are also many similarities, which will be pointed out in the sections to follow. The primary difference between the two types of transistors is the fact that: ***The BJT transistor is a current-controlled device whereas the JFET transistor is a voltage-controlled device.BJT is a bipolar device whereas JFET is unipolar device. BJT has low input impedance here JFET has very high input impedance. Symbol of JFET is shown in fig 6.1***

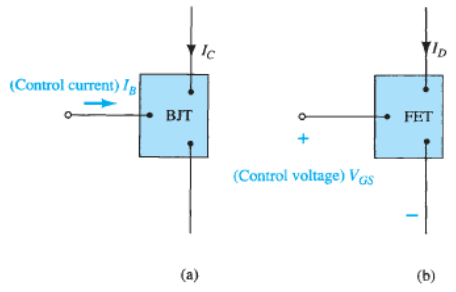


FIG. 6.1
(a) Current-controlled and (b) voltage-controlled amplifiers.

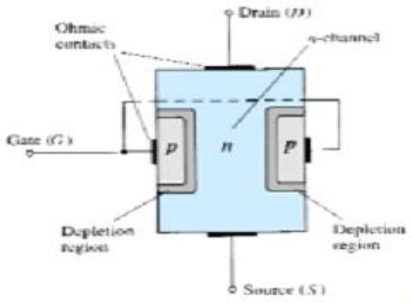


Figure 5.2 Junction field-effect transistor (JFET).

5.2 CONSTRUCTION AND CHARACTERISTICS OF JFETs

As indicated earlier, the JFET is a three-terminal device with one terminal capable of controlling the current between the other two. In our discussion of the BJT transistor the *npn* transistor was employed through the major part of the analysis and design sections, with a section devoted to the impact of using a *pnp* transistor. For the JFET transistor the *n*-channel device will appear as the prominent device, with paragraphs and sections devoted to the impact of using a *p*-channel JFET.

The basic construction of the *n*-channel JFET is shown in Fig. 5.2. Note that the major part of the structure is the *n*-type material that forms the channel between the embedded layers of *p*-type material. The top of the *n*-type channel is connected through an ohmic contact to a terminal referred to as the *drain (D),* while the lower end of the same material is connected through an ohmic contact to a terminal referred to as the *source (S)*. The two *p*-type materials are connected together and to the *gate (G)* terminal. In essence, therefore, the drain and source are connected to the ends of the *n*-type channel and the gate to the two layers of *p*-type material. In the absence of any applied potentials the JFET has two *p*-*n* junctions under no-bias conditions. The result is a depletion region at each junction as shown in Fig. 5.2 that resembles the same region of a diode under no-bias conditions. Recall also that a depletion region is that region void of free carriers and therefore unable to support conduction through the region.

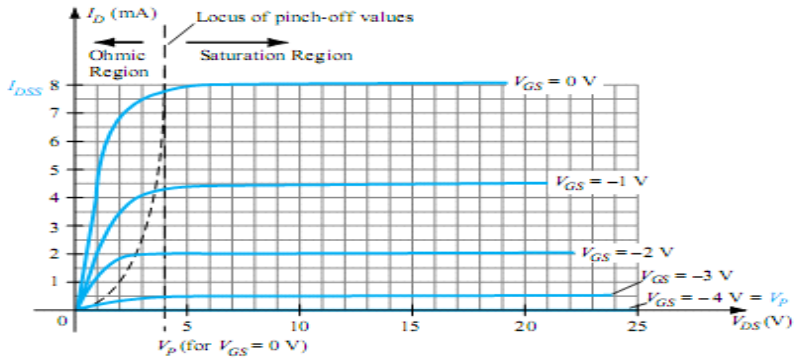
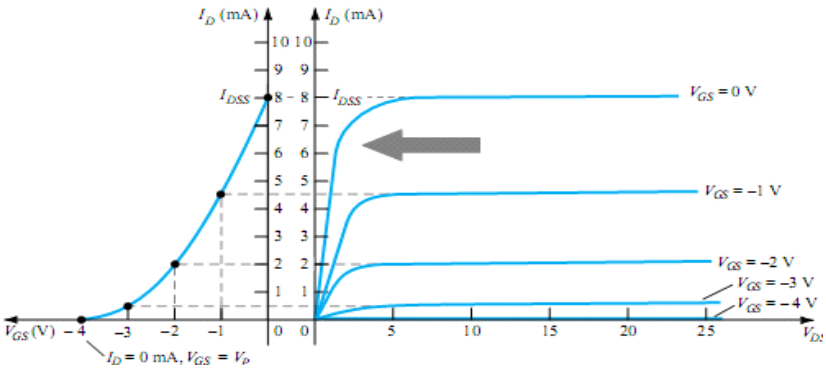


Figure 5.10 *n*-Channel JFET characteristics with $I_{DSS} = 8$ mA and $V_P = -4$ V.



Applying Shockley's Equation

The transfer curve of Fig. 5.15 can also be obtained directly from Shockley's equation (5.3) given simply the values of I_{DSS} and V_P. The levels of I_{DSS} and V_P define the limits of the curve on both axes and leave only the necessity of finding a few intermediate plot points. The validity of Eq. (5.3) as a source of the transfer curve of Fig. 5.15 is best demonstrated by examining a few specific levels of one variable and finding the resulting level of the other as follows:

Substituting $V_{GS} = 0$ V gives

$$\text{Eq. (5.3):} \quad I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= I_{DSS}\left(1 - \frac{0}{V_P}\right)^2 = I_{DSS}(1 - 0)^2$$

and

$$\boxed{I_D = I_{DSS} \mid V_{GS} = 0 \text{ V}} \tag{5.4}$$

Substituting $V_{GS} = V_P$ yields

$$I_D = I_{DSS}\left(1 - \frac{V_P}{V_P}\right)^2$$

$$= I_{DSS}(1 - 1)^2 = I_{DSS}(0)$$

$$\boxed{I_D = 0 \text{ A} \mid V_{GS} = V_P}$$

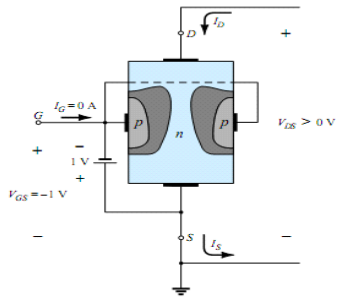


Figure 5.9 Application of a negative voltage to the gate of a JFET.

Symbols

The graphic symbols for the *n*-channel and *p*-channel JFETs are provided in Fig. 5.13. Note that the arrow is pointing in for the *n*-channel device of Fig. 5.13a to represent the direction in which I_G would flow if the *p*-*n* junction were forward-biased. For the *p*-channel device (Fig. 5.13b) the only difference in the symbol is the direction of the arrow.

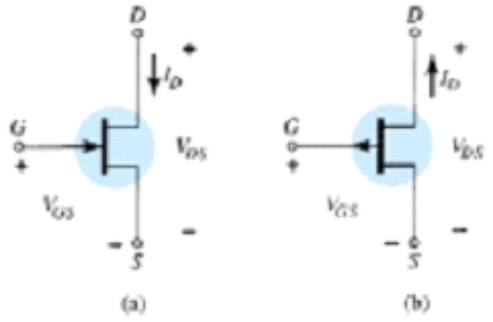


Figure 5.13 JFET symbols: (a) *n*-channel; (b) *p*-channel.

5.6 IMPORTANT RELATIONSHIPS

A number of important equations and operating characteristics have been introduced in the last few sections that are of particular importance for the analysis to follow for the dc and ac configurations. In an effort to isolate and emphasize their importance, they are repeated below next to a corresponding equation for the BJT transistor. The JFET equations are defined for the configuration of Fig. 5.22a, while the BJT equations relate to Fig. 5.22b.

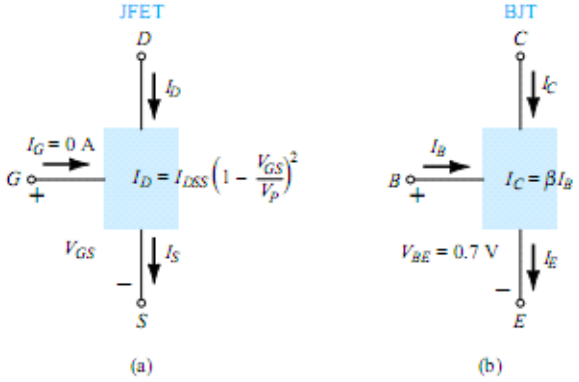


Figure 5.22 (a) JFET versus (b) BJT.

JFET		*BJT*
$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$	$\Leftrightarrow$	$I_C = \beta I_B$
$I_D = I_S$	$\Leftrightarrow$	$I_C \cong I_E$
$I_G \cong 0$ A	$\Leftrightarrow$	$V_{BE} \cong 0.7$ V

(5.10)

5.7 DEPLETION-TYPE MOSFET

Basic Construction

The basic construction of the *n*-channel depletion-type MOSFET is provided in Fig. 5.23. A slab of *p*-type material is formed from a silicon base and is referred to as the *substrate*. It is the foundation upon which the device will be constructed. In some cases the substrate is internally connected to the source terminal. However, many discrete devices provide an additional terminal labeled *SS*, resulting in a four-terminal device, such as that appearing in Fig. 5.23. The source and drain terminals are connected through metallic contacts to *n*-doped regions linked by an *n*-channel as shown in the figure. The gate is also connected to a metal contact surface but remains insulated from the *n*-channel by a very thin silicon dioxide (SiO_2) layer. SiO_2 is a particular type of insulator referred to as a *dielectric* that sets up opposing (as revealed by

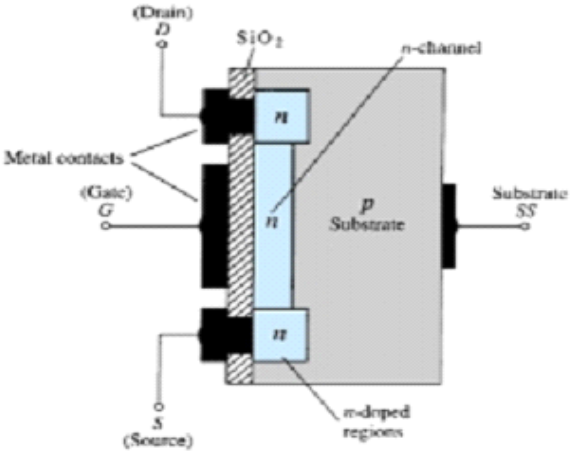


Figure 5.23 *n*-Channel depletion-type MOSFET.

the prefix *di-*) electric fields within the dielectric when exposed to an externally applied field. The fact that the SiO_2 layer is an insulating layer reveals the following fact:

There is no direct electrical connection between the gate terminal and the channel of a MOSFET.

In addition:

It is the insulating layer of SiO_2 in the MOSFET construction that accounts for the very desirable high input impedance of the device.

In fact, the input resistance of a MOSFET is often that of the typical JFET, even though the input impedance of most JFETs is sufficiently high for most applications. The very high input impedance continues to fully support the fact that the gate current (I_G) is essentially zero amperes for dc-biased configurations.

The reason for the label metal-oxide-semiconductor FET is now fairly obvious: *metal* for the drain, source, and gate connections to the proper surface—in particular, the gate terminal and the control to be offered by the surface area of the contact, the *oxide* for the silicon dioxide insulating layer, and the *semiconductor* for the basic structure on which the *n*- and *p*-type regions are diffused. The insulating layer between the gate and channel has resulted in another name for the device: *insulated-gate FET* or *IGFET,* although this label is used less and less in current literature.

Basic Operation and Characteristics

In Fig. 5.24 the gate-to-source voltage is set to zero volts by the direct connection from one terminal to the other, and a voltage V_{DS} is applied across the drain-to-source terminals. The result is an attraction for the positive potential at the drain by the *free* electrons of the *n*-channel and a current similar to that established through the channel of the JFET. In fact, the resulting current with $V_{GS} = 0$ V continues to be labeled I_{DSS}, as shown in Fig. 5.25.

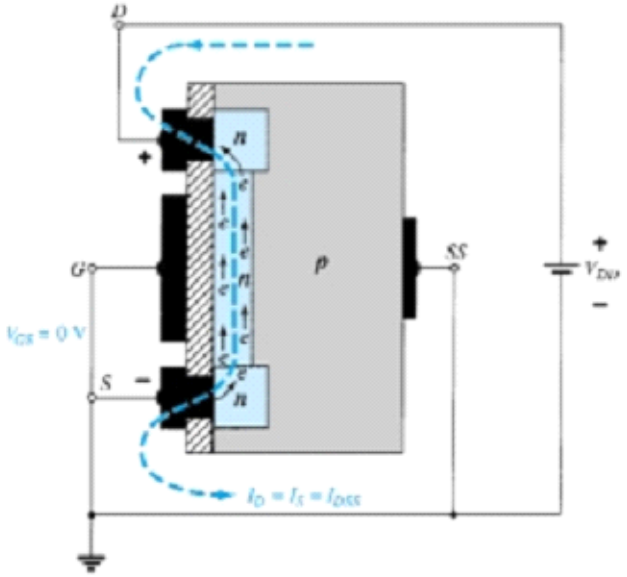


Figure 5.24 *n*-Channel depletion-type MOSFET with $V_{GS} = 0$ V and an applied voltage V_{DD}

In Fig. 5.26, V_{GS} has been set at a negative voltage such as -1 V. The negative potential at the gate will tend to pressure electrons toward the *p*-type substrate (like charges repel) and attract holes from the *p*-type substrate (opposite charges attract) as shown in Fig. 5.26. Depending on the magnitude of the negative bias established by V_{GS}, a level of recombination between electrons and holes will occur that will reduce the number of free electrons in the *n*-channel available for conduction. The more negative the bias, the higher the rate of recombination. The resulting level of drain current is therefore reduced with increasing negative bias for V_{GS} as shown in Fig. 5.25 for $V_{GS} = -1$ V, -2 V, and so on, to the pinch-off level of -6 V. The resulting levels of drain current and the plotting of the transfer curve proceeds exactly as described for the JFET.

For positive values of V_{GS}, the positive gate will draw additional electrons (free carriers) from the *p*-type substrate due to the reverse leakage current and establish new carriers through the collisions resulting between accelerating particles. As the gate-to-source voltage continues to increase in the positive direction, Fig. 5.25 reveals that the drain current will increase at a rapid rate for the reasons listed above. The

As revealed above, the application of a positive gate-to-source voltage has "enhanced" the level of free carriers in the channel compared to that encountered with $V_{GS} = 0$ V. For this reason the region of positive gate voltages on the drain or transfer characteristics is often referred to as the *enhancement region*, with the region between cutoff and the saturation level of I_{DSS} referred to as the *depletion region*.

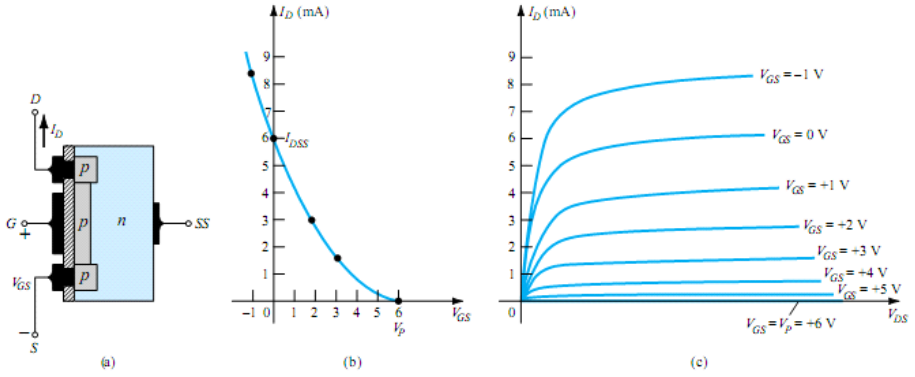


Figure 5.28 *p*-Channel depletion-type MOSFET with $I_{DSS} = 6$ mA and $V_P = +6$ V.

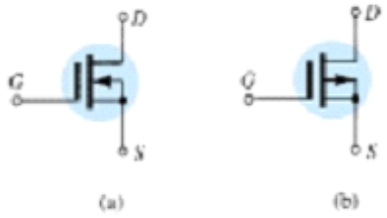


Figure 5.29 Graphic symbols for (a) *n*-channel depletion-type MOSFETs and (b) *p*-channel depletion-type MOSFETs.

5.8 ENHANCEMENT-TYPE MOSFET

Although there are some similarities in construction and mode of operation between depletion-type and enhancement-type MOSFETs, the characteristics of the enhancement-type MOSFET are quite different from anything obtained thus far. The transfer curve is not defined by Shockley's equation, and the drain current is now cut off until the gate-to-source voltage reaches a specific magnitude. In particular, current control in an *n*-channel device is now effected by a positive gate-to-source voltage rather than the range of negative voltages encountered for *n*-channel JFETs and *n*-channel depletion-type MOSFETs.

Basic Construction

The basic construction of the *n*-channel enhancement-type MOSFET is provided in Fig. 5.31. A slab of *p*-type material is formed from a silicon base and is again referred to as the substrate. As with the depletion-type MOSFET, the substrate is sometimes internally connected to the source terminal, while in other cases a fourth lead is made available for external control of its potential level. The source and drain terminals are again connected through metallic contacts to *n*-doped regions, but note in Fig. 5.31 the absence of a channel between the two *n*-doped regions. This is the primary difference between the construction of depletion-type and enhancement-type MOSFETs—the absence of a channel as a constructed component of the device. The SiO_2 layer is still present to isolate the gate metallic platform from the region between the drain and source, but now it is simply separated from a section of the *p*-type material. In summary, therefore, the construction of an enhancement-type MOSFET is quite similar to that of the depletion-type MOSFET, except for the absence of a channel between the drain and source terminals.

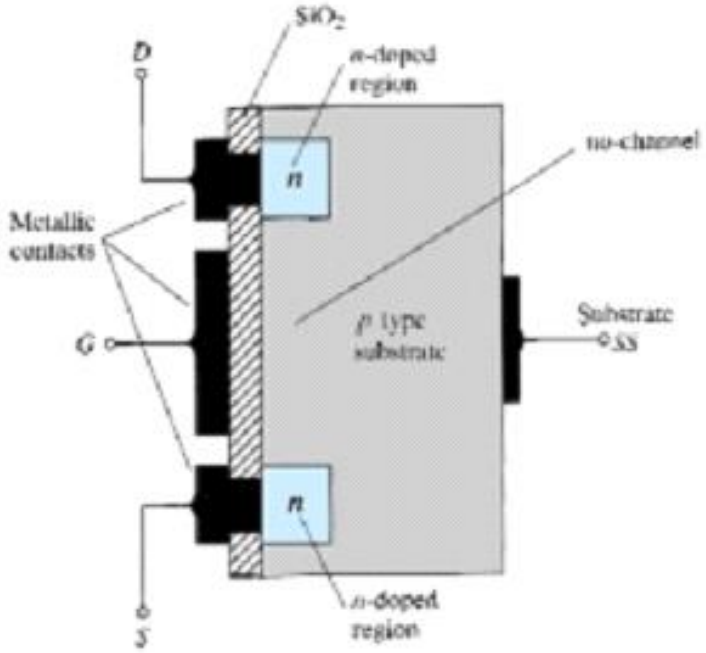


Figure 5.31 n-Channel enhancement-type MOSFET.

Basic Operation and Characteristics

If V_{GS} is set at 0 V and a voltage applied between the drain and source of the device of Fig. 5.31, the absence of an *n*-channel (with its generous number of free carriers) will result in a current of effectively zero amperes—quite different from the depletion-type MOSFET and JFET where $I_D = I_{DSS}$. It is not sufficient to have a large accumulation of carriers (electrons) at the drain and source (due to the *n*-doped regions) if a path fails to exist between the two. With V_{DS} some positive voltage, V_{GS} at 0 V, and terminal *SS* directly connected to the source, there are in fact two reverse-biased *p*-*n* junctions between the *n*-doped regions and the *p*-substrate to oppose any significant flow between drain and source.

In Fig. 5.32 both V_{DS} and V_{GS} have been set at some positive voltage greater than 0 V, establishing the drain and gate at a positive potential with respect to the source. The positive potential at the gate will pressure the holes (since like charges repel) in the *p*-substrate along the edge of the SiO_2 layer to leave the area and enter deeper regions of the *p*-substrate, as shown in the figure. The result is a depletion region near the SiO_2 insulating layer void of holes. However, the electrons in the *p*-substrate (the minority carriers of the material) will be attracted to the positive gate and accumulate in the region near the surface of the SiO_2 layer. The SiO_2 layer and its insulating qualities will prevent the negative carriers from being absorbed at the gate terminal. As V_{GS} increases in magnitude, the concentration of electrons near the SiO_2 surface increases until eventually the induced *n*-type region can support a measurable flow between drain and source. The level of V_{GS} that results in the significant increase in drain current is called the *threshold voltage* and is given the symbol V_T. On specification sheets it is referred to as $V_{GS(Th)}$, although V_T is less unwieldy and will be used in the analysis to follow. Since the channel is nonexistent with $V_{GS} = 0$ V and "enhanced" by the application of a positive gate-to-source voltage, this type of MOSFET is called an *enhancement-type MOSFET*. Both depletion- and enhancement-type MOSFETs have enhancement-type regions, but the label was applied to the latter since it is its only mode of operation.

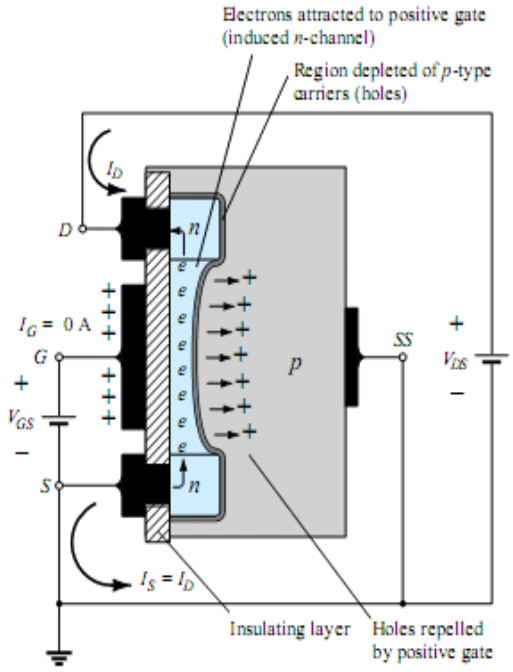


Figure 5.32 Channel formation in the *n*-channel enhancement-type MOSFET.

As V_{GS} is increased beyond the threshold level, the density of free carriers in the induced channel will increase, resulting in an increased level of drain current. However, if we hold V_{GS} constant and increase the level of V_{DS}, the drain current will eventually reach a saturation level as occurred for the JFET and depletion-type MOSFET. The leveling off of I_D is due to a pinching-off process depicted by the narrower channel at the drain end of the induced channel as shown in Fig. 5.33. Applying Kirchhoff's voltage law to the terminal voltages of the MOSFET of Fig. 5.33, we find that

$$V_{DG} = V_{DS} - V_{GS} \tag{5.11}$$

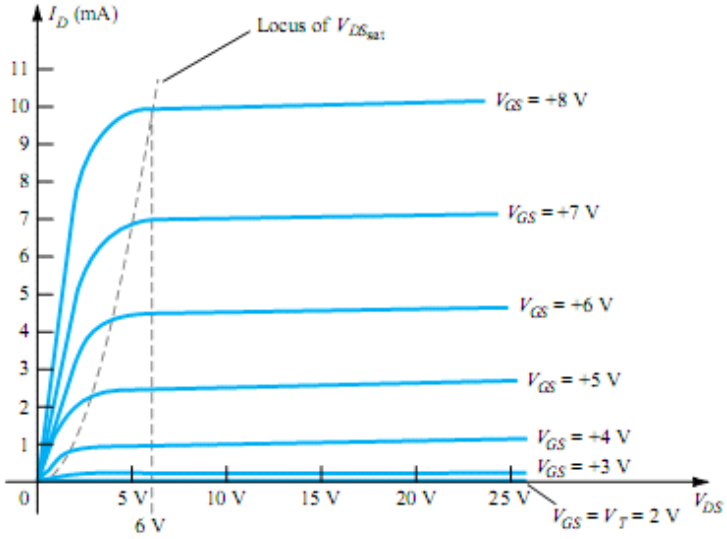


Figure 5.34 Drain characteristics of an *n*-channel enhancement-type MOSFET with $V_T = 2$ V and $k = 0.278 \times 10^{-3}$ A/V^2.

For levels of $V_{GS} > V_T$, the drain current is related to the applied gate-to-source voltage by the following nonlinear relationship:

$$I_D = k(V_{GS} - V_T)^2 \tag{5.13}$$

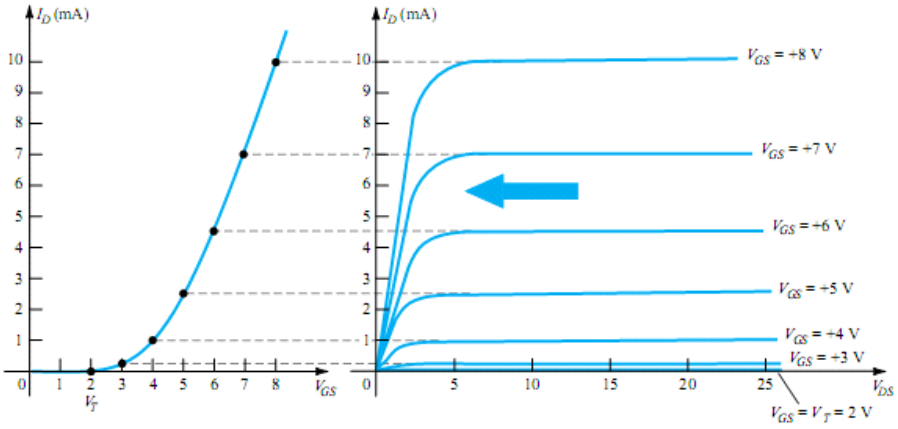


Figure 5.35 Sketching the transfer characteristics for an *n*-channel enhancement-type MOSFET from the drain characteristics.

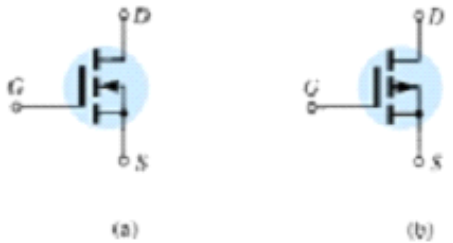


Figure 5.38 Symbols for (a) *n*-channel enhancement-type MOSFETs and (b) *p*-channel enhancement-type MOSFETs.

FET Biasing

The general relationships that can be applied to the dc analysis of all FET amplifiers are

$$I_G \cong 0 \text{ A} \tag{6.1}$$

and

$$I_D = I_S \tag{6.2}$$

For JFETS and depletion-type MOSFETs, Shockley's equation is applied to relate the input and output quantities:

$$I_D = I_{DSS}\left(\frac{1 - V_{GS}}{V_P}\right)^2 \tag{6.3}$$

For enhancement-type MOSFETs, the following equation is applicable:

$$I_D = k(V_{GS} - V_T)^2 \tag{6.4}$$

6.2 FIXED-BIAS CONFIGURATION

$$I_G \cong 0 \text{ A}$$

and

$$V_{R_G} = I_G R_G = (0 \text{ A})R_G = 0 \text{ V}$$

The zero-volt drop across R_G permits replacing R_G by a short-circuit equivalent, as appearing in the network of Fig. 6.2 specifically redrawn for the dc analysis.

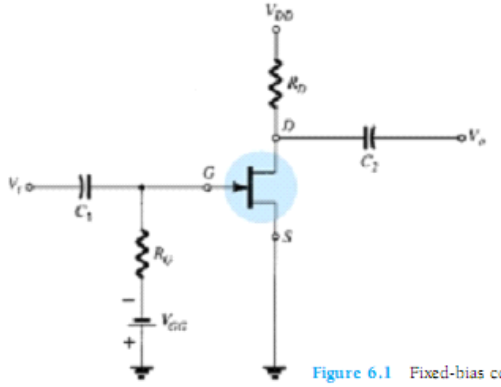


Figure 6.1 Fixed-bias configuration.

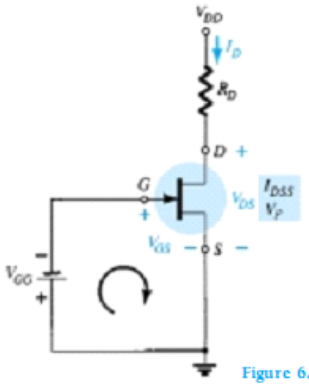


Figure 6.2 Network for dc analysis.

The fact that the negative terminal of the battery is connected directly to the defined positive potential of V_{GS} clearly reveals that the polarity of V_{GS} is directly opposite to that of V_{GG}. Applying Kirchhoff's voltage law in the clockwise direction of the indicated loop of Fig. 6.2 will result in

$$-V_{GG} - V_{GS} = 0$$

and

$$\boxed{V_{GS} = -V_{GG}} \tag{6.5}$$

Since V_{GG} is a fixed dc supply, the voltage V_{GS} is fixed in magnitude, resulting in the notation "fixed-bias configuration."

The resulting level of drain current I_D is now controlled by Shockley's equation:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Since V_{GS} is a fixed quantity for this configuration, its magnitude and sign can simply be substituted into Shockley's equation and the resulting level of I_D calculated. This is one of the few instances in which a mathematical solution to a FET configuration is quite direct.

A graphical analysis would require a plot of Shockley's equation as shown in Fig. 6.3. Recall that choosing $V_{GS} = V_P/2$ will result in a drain current of $I_{DSS}/4$ when plotting the equation. For the analysis of this chapter, the three points defined by I_{DSS}, V_P, and the intersection just described will be sufficient for plotting the curve.

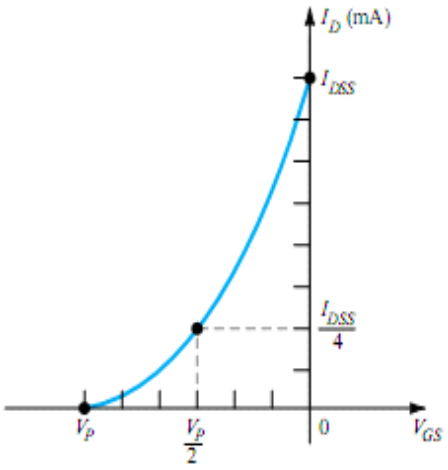


Figure 6.3 Plotting Shockley's equation.

The drain-to-source voltage of the output section can be determined by applying Kirchhoff's voltage law as follows:

$$+V_{DS} + I_D R_D - V_{DD} = 0$$

and

$$\boxed{V_{DS} = V_{DD} - I_D R_D} \tag{6.6}$$

Recall that single-subscript voltages refer to the voltage at a point with respect to ground. For the configuration of Fig. 6.2,

$$\boxed{V_S = 0\text{ V}} \tag{6.7}$$

Using double-subscript notation:

$$V_{DS} = V_D - V_S$$

or

$$V_D = V_{DS} + V_S = V_{DS} + 0\text{ V}$$

and

$$\boxed{V_D = V_{DS}} \tag{6.8}$$

In addition,

$$V_{GS} = V_G - V_S$$

or

$$V_G = V_{GS} + V_S = V_{GS} + 0\text{ V}$$

and

$$\boxed{V_G = V_{GS}} \tag{6.9}$$

6.3 SELF-BIAS CONFIGURATION

The self-bias configuration eliminates the need for two dc supplies. The controlling gate-to-source voltage is now determined by the voltage across a resistor R_S introduced in the source leg of the configuration as shown in Fig. 6.8.

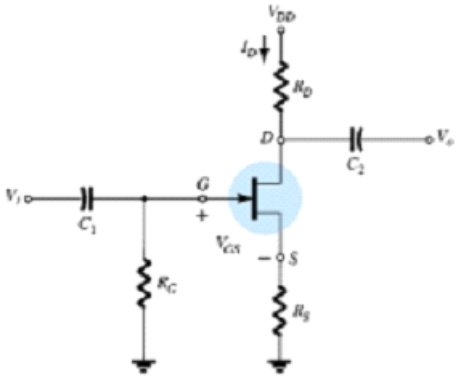
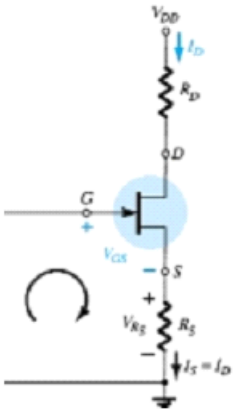


Figure 6.8 JFET self-bias configuration.



For the dc analysis, the capacitors can again be replaced by "open circuits" and the resistor R_G replaced by a short-circuit equivalent since $I_G = 0$ A. The result is the network of Fig. 6.9 for the important dc analysis.

The current through R_S is the source current I_S, but $I_S = I_D$ and

$$V_{R_S} = I_D R_S$$

For the indicated closed loop of Fig. 6.9, we find that

$$-V_{GS} - V_{R_S} = 0$$

and

$$V_{GS} = -V_{R_S}$$

or

$$\boxed{V_{GS} = -I_D R_S} \tag{6.10}$$

The level of V_{DS} can be determined by applying Kirchhoff's voltage law to the output circuit, with the result that

$$V_{R_S} + V_{DS} + V_{R_D} - V_{DD} = 0$$

and

$$V_{DS} = V_{DD} - V_{R_S} - V_{R_D} = V_{DD} - I_S R_S - I_D R_D$$

but

$$I_D = I_S$$

and

$$\boxed{V_{DS} = V_{DD} - I_D(R_S + R_D)} \tag{6.11}$$

In addition:

$$\boxed{V_S = I_D R_S} \tag{6.12}$$

$$\boxed{V_G = 0\,\text{V}} \tag{6.13}$$

and

$$\boxed{V_D = V_{DS} + V_S = V_{DD} - V_{R_D}} \tag{6.14}$$

6.4 VOLTAGE-DIVIDER BIASING

The voltage-divider bias arrangement applied to BJT transistor amplifiers is also applied to FET amplifiers as demonstrated by Fig. 6.20. The basic construction is exactly the same, but the dc analysis of each is quite different. $I_G = 0$ A for FET amplifiers, but the magnitude of I_B for common-emitter BJT amplifiers can affect the dc levels of current and voltage in both the input and output circuits. Recall that I_B provided the link between input and output circuits for the BJT voltage-divider configuration while V_{GS} will do the same for the FET configuration.

The network of Fig. 6.20 is redrawn as shown in Fig. 6.21 for the dc analysis. Note that all the capacitors, including the bypass capacitor C_S, have been replaced by an "open-circuit" equivalent. In addition, the source V_{DD} was separated into two equiv-

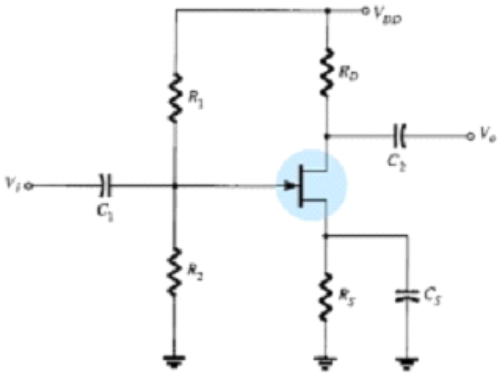


Figure 6.20 Voltage-divider bias arrangement.

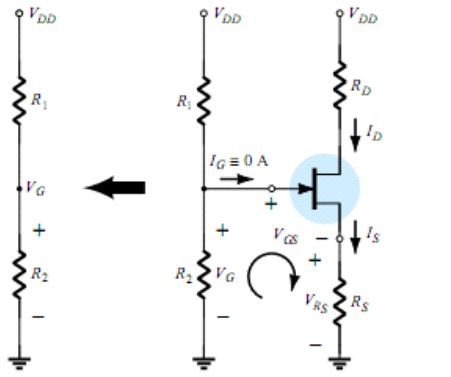


Figure 6.21 Redrawn network of Fig. 6.20 for dc analysis.

alent sources to permit a further separation of the input and output regions of the network. Since $I_G = 0$ A, Kirchhoff's current law requires that $I_{R_1} = I_{R_2}$ and the series equivalent circuit appearing to the left of the figure can be used to find the level of V_G. The voltage V_G, equal to the voltage across R_2, can be found using the voltage-divider rule as follows:

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2} \tag{6.15}$$

Applying Kirchhoff's voltage law in the clockwise direction to the indicated loop of Fig. 6.21 will result in

$$V_G - V_{GS} - V_{R_S} = 0$$

and

$$V_{GS} = V_G - V_{R_S}$$

Substituting $V_{R_s} = I_S R_S = I_D R_S$, we have

$$V_{GS} = V_G - I_D R_S \tag{6.16}$$

Once the quiescent values of I_{D_Q} and V_{GS_Q} are determined, the remaining network analysis can be performed in the usual manner. That is,

$$V_{DS} = V_{DD} - I_D(R_D + R_S) \tag{6.19}$$

$$V_D = V_{DD} - I_D R_D \tag{6.20}$$

$$V_S = I_D R_S \tag{6.21}$$

$$I_{R_1} = I_{R_2} = \frac{V_{DD}}{R_1 + R_2} \tag{6.22}$$

BJT	*FET*
1. Two types of carriers (electrons and holes) are required.	1. Only one type of carrier (electron or hole) is required.
2. Carriers move through the base by diffusion process.	2. Carriers move through the channel by drift process.
3. The BJT has a comparatively lower switching speed due to the diffusion process.	3. The FET has a higher switching speed due to the drift process; the drift of the carrier is faster than diffusion.
4. The BJT is not a thermally stable device.	4. The FET has a negative temperature coefficient at high-current operations, i.e., the current decreases as temperature increases Due to this particular feature, a uniform temperature distribution and protection against breakdown can be achieved.
5. In case of IC fabrication, the BJT requires more space than the FET.	5. In case of IC fabrication the FET requires lesser space than the BJT.
6. At audio frequencies the BJT offers less power gain.	6. At audio frequencies the FET offers greater power gain.
7. The BJT is a current-controlled device.	7. The FET is a voltage-controlled device.
8. The BJT offers low input impedance.	8. The FET offers high input impedance, therefore, it can be used as a buffer.
9. BJT is much noisier than FET.	9. FET is less noisy.
10. The BJT has offset voltage.	10. The FET has no offset voltage.
11. The BJT can also be used as a switch; it is taken to be in the OFF state when operating in the cut off region, and in the ON state when it is operating in the saturation region.	11. The FET is particularly useful for its operation as a controlled switch, operating in both the conducting and the non-conducting zones.

Small signal model of FET(Important)

9.2 FET SMALL-SIGNAL MODEL

The ac analysis of an FET configuration requires that a small-signal ac model for the FET be developed. A major component of the ac model will reflect the fact that an ac voltage applied to the input gate-to-source terminals will control the level of current from drain to source.

The gate-to-source voltage controls the drain-to-source (channel) current of an FET.

Recall from Chapter 6 that a dc gate-to-source voltage controlled the level of dc drain current through a relationship known as Shockley's equation: $I_D = I_{DSS}(1 - V_{GS}/V_P)^2$. The *change* in collector current that will result from a *change* in gate-to-source voltage can be determined using the transconductance factor g_m in the following manner:

$$\Delta I_D = g_m \, \Delta V_{GS} \tag{9.1}$$

The prefix *trans-* in the terminology applied to g_m reveals that it establishes a relationship between an output and input quantity. The root word *conductance* was chosen because g_m is determined by a voltage-to-current ratio similar to the ratio that defines the conductance of a resistor $G = 1/R = I/V$.

Solving for g_m in Eq. (9.1), we have:

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \tag{9.2}$$

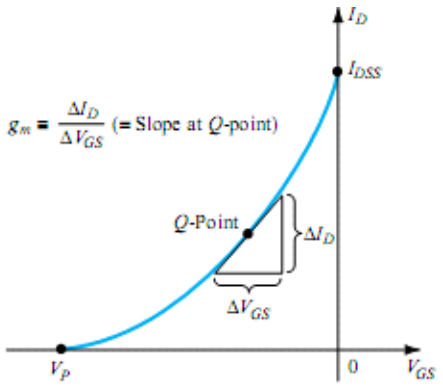


Figure 9.1 Definition of g_m using transfer characteristic.

find the dc resistance of a diode in Chapter 1, where it was stated that:

The derivative of a function at a point is equal to the slope of the tangent line drawn at that point.

If we therefore take the derivative of I_D with respect to V_{GS} (differential calculus) using Shockley's equation, an equation for g_m can be derived as follows:

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}\bigg|_{Q\text{-pt.}} = \frac{dI_D}{dV_{GS}}\bigg|_{Q\text{-pt.}} = \frac{d}{dV_{GS}}\left[I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2\right]$$

$$= I_{DSS}\frac{d}{dV_{GS}}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 2I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]\frac{d}{dV_{GS}}\left(1 - \frac{V_{GS}}{V_P}\right)$$

$$= 2I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]\left[\frac{d}{dV_{GS}}(1) - \frac{1}{V_P}\frac{dV_{GS}}{dV_{GS}}\right] = 2I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]\left[0 - \frac{1}{V_P}\right]$$

and

$$\boxed{g_m = \frac{2I_{DSS}}{|V_P|}\left[1 - \frac{V_{GS}}{V_P}\right]} \tag{9.4}$$

where $|V_P|$ denotes magnitude only to ensure a positive value for g_m.

It was mentioned earlier that the slope of the transfer curve is a maximum at $V_{GS} = 0$ V. Plugging in $V_{GS} = 0$ V into Eq. (9.4) will result in the following equation for the maximum value of g_m for a JFET in which I_{DSS} and V_P have been specified:

$$g_m = \frac{2I_{DSS}}{|V_P|}\left[1 - \frac{0}{V_P}\right]$$

and

$$\boxed{g_{m0} = \frac{2I_{DSS}}{|V_P|}} \tag{9.5}$$

where the added subscript 0 reminds us that it is the value of g_m when $V_{GS} = 0$ V. Equation (9.4) then becomes

For the JFET having the transfer characteristics of Example 9.1:
(a) Find the maximum value of g_m.
(b) Find the value of g_m at each operating point of Example 9.1 using Eq. (9.6) and compare with the graphical results.

Solution

(a) $g_{m0} = \dfrac{2I_{DSS}}{|V_P|} = \dfrac{2(8\text{ mA})}{4\text{ V}} = \mathbf{4\text{ mS}}$ (maximum possible value of g_m)

(b) At $V_{GS} = -0.5$ V,

$$g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_P}\right] = 4\text{ mS}\left[1 - \frac{-0.5\text{ V}}{-4\text{ V}}\right] = \mathbf{3.5\text{ mS}}$$ (versus 3.5 mS graphically)

Impact of I_D on g_m

A mathematical relationship between g_m and the dc bias current I_D can be de noting that Shockley's equation can be written in the following form:

$$1 - \frac{V_{GS}}{V_P} = \sqrt{\frac{I_D}{I_{DSS}}}$$

Substituting Eq. (9.8) into Eq. (9.6) will result in

$$g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_P}\right) = g_{m0}\sqrt{\frac{I_D}{I_{DSS}}}$$

FET Input Impedance Z_i

The input impedance of all commercially available FETs is sufficiently large to assume that the input terminals approximate an open circuit. In equation form,

$$Z_i \text{ (FET)} = \infty\ \Omega \tag{9.10}$$

For a JFET a practical value of $10^9\ \Omega$ (1000 MΩ) is typical, while a value of 10^{12} to $10^{15}\ \Omega$ is typical for MOSFETs.

FET Output Impedance Z_o

The output impedance of FETs is similar in magnitude to that of conventional BJTs. On FET specification sheets, the output impedance will typically appear as y_{os} with the units of μS. The parameter y_{os} is a component of an *admittance equivalent circuit,* with the subscript o signifying an *o*utput network parameter and s the terminal (source) to which it is attached in the model. For the JFET of Fig. 5.18, y_{os} has a range of 10 to 50 μS or 20 kΩ ($R = 1/G = 1/50\ \mu$S) to 100 kΩ ($R = 1/G = 1/10\ \mu$S).

In equation form,

$$Z_o \text{ (FET)} = r_d = \frac{1}{y_{os}} \tag{9.11}$$

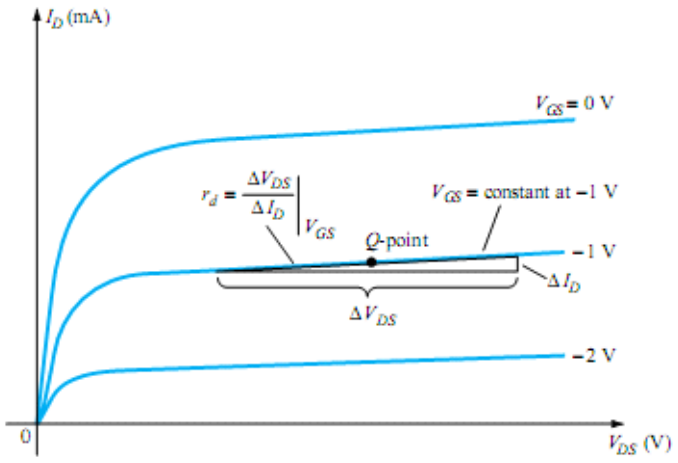


Figure 9.6 Definition of r_d using FET drain characteristics.

FET AC Equivalent Circuit

Now that the important parameters of an ac equivalent circuit have been introduced and discussed, a model for the FET transistor in the ac domain can be constructed. The control of I_d by V_{gs} is included as a current source $g_m V_{gs}$ connected from drain to source as shown in Fig. 9.8. The current source has its arrow pointing from drain to source to establish a 180° phase shift between output and input voltages as will occur in actual operation.

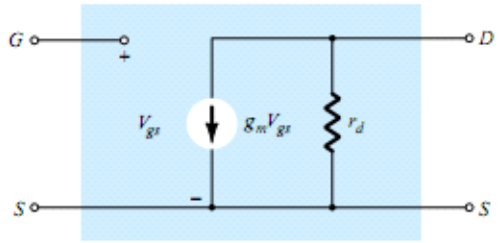


Figure 9.8 FET ac equivalent circuit.

The input impedance is represented by the open circuit at the input terminals and the output impedance by the resistor r_d from drain to source. Note that the gate to source voltage is now represented by V_{gs} (lower-case subscripts) to distinguish it from dc levels. In addition, take note of the fact that the source is common to both input and output circuits while the gate and drain terminals are only in "touch" through the controlled current source $g_m V_{gs}$.

Given $y_{fs} = 3.8$ mS and $y_{os} = 20\ \mu$S, sketch the FET ac equivalent model.

Solution

$$g_m = y_{fs} = 3.8 \text{ mS} \quad \text{and} \quad r_d = \frac{1}{y_{os}} = \frac{1}{20\ \mu\text{S}} = 50\ \text{k}\Omega$$

resulting in the ac equivalent model of Fig. 9.9.

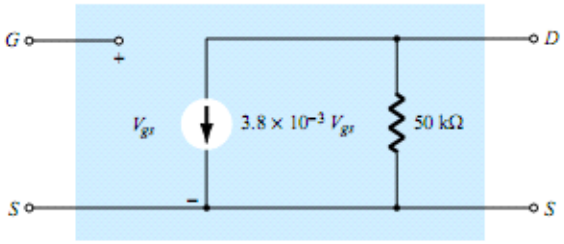


Figure 9.9 FET ac equivalent model for Example 9.6.

9.3 JFET FIXED-BIAS CONFIGURATION

Now that the FET equivalent circuit has been defined, a number of fundamental FET small-signal configurations will be investigated. The approach will parallel the ac analysis of BJT amplifiers with a determination of the important parameters of Z_i, Z_o, and A_v for each configuration.

The *fixed-bias* configuration of Fig. 9.10 includes the coupling capacitors C_1 and C_2 that isolate the dc biasing arrangement from the applied signal and load; they act as short-circuit equivalents for the ac analysis.

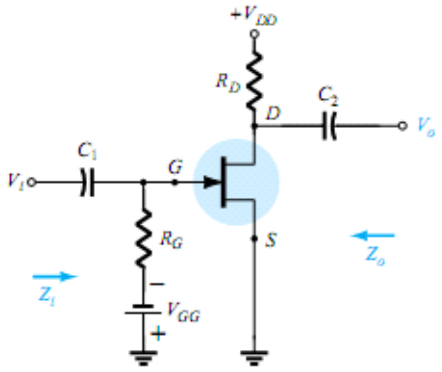


Figure 9.10 JFET fixed-bias configuration.

Once the level of g_m and r_d are determined from the dc biasing arrangement, specification sheet, or characteristics, the ac equivalent model can be substituted between the appropriate terminals as shown in Fig. 9.11. Note that both capacitors have the short-circuit equivalent because the reactance $X_C = 1/(2\pi fC)$ is sufficiently small compared to other impedance levels of the network, and the dc batteries V_{GG} and V_{DD} are set to zero volts by a short-circuit equivalent.

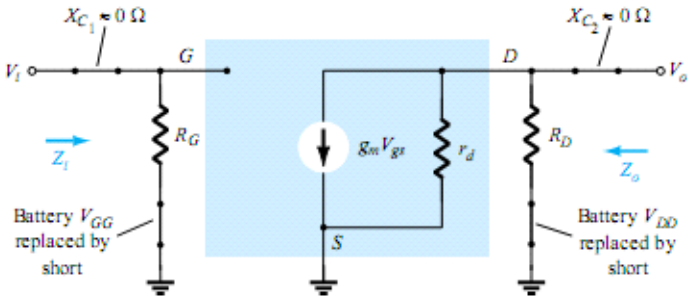


Figure 9.11 Substituting the JFET ac equivalent circuit unit into the network of Fig. 9.10.

The network of Fig. 9.11 is then carefully redrawn as shown in Fig. 9.12. Note the defined polarity of V_{gs}, which defines the direction of $g_m V_{gs}$. If V_{gs} is negative, the direction of the current source reverses. The applied signal is represented by V_i and the output signal across R_D by V_o.

Z_i: Figure 9.12 clearly reveals that

$$Z_i = R_G \tag{9.13}$$

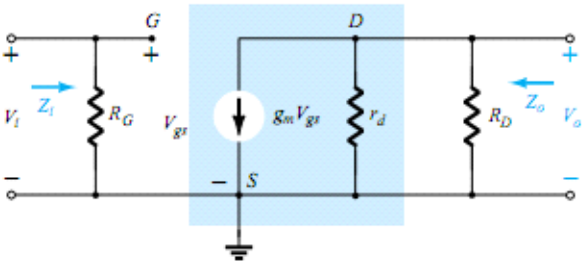


Figure 9.12 Redrawn network of Fig. 9.11.

Z_o: Setting $V_i = 0$ V as required by the definition of Z_o will establish V_{gs} as 0 V also. The result is $g_m V_{gs} = 0$ mA, and the current source can be replaced by an open-circuit equivalent as shown in Fig. 9.13. The output impedance is

$$Z_o = R_D \| r_d \tag{9.14}$$

If the resistance r_d is sufficiently large (at least 10:1) compared to R_D, the approximation $r_d \| R_D \cong R_D$ can often be applied and

$$Z_o \cong R_D \qquad r_d \geq 10R_D \tag{9.15}$$

A_v: Solving for V_o in Fig. 9.12, we find

$$V_o = -g_m V_{gs}(r_d \| R_D)$$

but $$V_{gs} = V_i$$

and $$V_o = -g_m V_i(r_d \| R_D)$$

so that

$$A_v = \frac{V_o}{V_i} = -g_m(r_d \| R_D) \tag{9.16}$$

If $r_d \geq 10R_D$:

$$A_v = \frac{V_o}{V_i} = -g_m R_D \tag{9.17}$$

$r_d \geq 10R_D$

Phase Relationship: The negative sign in the resulting equation for A_v clearly reveals a phase shift of 180° between input and output voltages.

EXAMPLE 9.7

The fixed-bias configuration of Example 6.1 had an operating point defined by $V_{GS_Q} = -2$ V and $I_{D_Q} = 5.625$ mA, with $I_{DSS} = 10$ mA and $V_P = -8$ V. The network is redrawn as Fig. 9.14 with an applied signal V_i. The value of y_{os} is provided as 40 μS.

(a) Determine g_m.
(b) Find r_d.
(c) Determine Z_i.
(d) Calculate Z_o.
(e) Determine the voltage gain A_v.
(f) Determine A_v ignoring the effects of r_d.

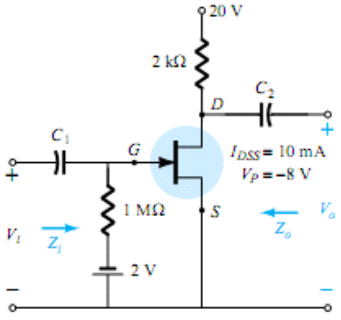


Figure 9.14 JFET configuration for Example 9.7.

Solution

(a) $g_{m0} = \dfrac{2I_{DSS}}{|V_P|} = \dfrac{2(10\text{ mA})}{8\text{ V}} = 2.5\text{ mS}$

$$g_m = g_{m0}\left(1 - \frac{V_{GS_Q}}{V_P}\right) = 2.5\text{ mS}\left(1 - \frac{(-2\text{ V})}{(-8\text{ V})}\right) = \mathbf{1.88\text{ mS}}$$

(b) $r_d = \dfrac{1}{y_{os}} = \dfrac{1}{40\ \mu\text{S}} = \mathbf{25\ k\Omega}$

(c) $Z_i = R_G = \mathbf{1\ M\Omega}$

(d) $Z_o = R_D \| r_d = 2\text{ k}\Omega \| 25\text{ k}\Omega = \mathbf{1.85\ k\Omega}$

(e) $A_v = -g_m(R_D \| r_d) = -(1.88\text{ mS})(1.85\text{ k}\Omega)$
$= \mathbf{-3.48}$

(f) $A_v = -g_m R_D = -(1.88\text{ mS})(2\text{ k}\Omega) = \mathbf{-3.76}$

9.4 JFET SELF-BIAS CONFIGURATION

Bypassed R_S

The fixed-bias configuration has the distinct disadvantage of requiring two dc voltage sources. The *self-bias* configuration of Fig. 9.15 requires only one dc supply to establish the desired operating point.

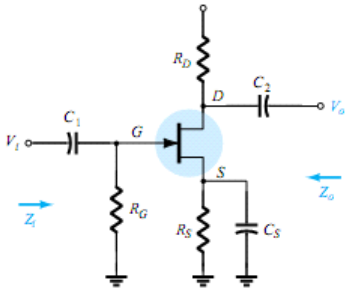


Figure 9.15 Self-bias JFET configuration.

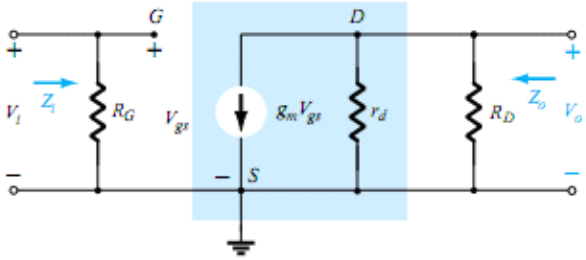


Figure 9.17 Redrawn network of Fig. 9.16.

Since the resulting configuration is the same as appearing in Fig. 9.12, the resulting equations Z_i, Z_o, and A_v will be the same.

$\boldsymbol{Z_i}$:

$$\boxed{Z_i = R_G} \tag{9.18}$$

$\boldsymbol{Z_o}$:

$$\boxed{Z_o = r_d \| R_D} \tag{9.19}$$

If $r_d \geq 10R_D$,

$$\boxed{Z_o \cong R_D}_{r_d \geq 10R_D} \tag{9.20}$$

$\boldsymbol{A_v}$:

$$\boxed{A_v = -g_m(r_d \| R_D)} \tag{9.21}$$

If $r_d \geq 10R_D$,

$$\boxed{A_v = -g_m R_D}_{r_d \geq 10R_D} \tag{9.22}$$

Phase relationship: The negative sign in the solutions for A_v again indicates a phase shift of 180° between V_i and V_o.

Unbypassed R_S

If C_S is removed from Fig 9.15, the resistor R_S will be part of the ac equivalent circuit as shown in Fig. 9.18. In this case, there is no obvious way to reduce the network to lower its level of complexity. In determining the levels of Z_i, Z_o, and A_v, one must simply be very careful with notation and defined polarities and direction. Initially, the resistance r_d will be left out of the analysis to form a basis for comparison.

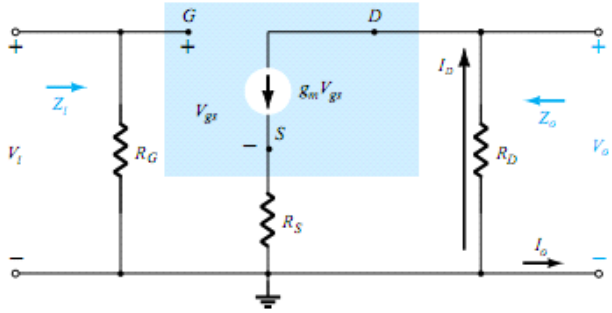


Figure 9.18 Self-bias JFET configuration including the effects of R_S with $r_d = \infty\Omega$.

Z_i: Due to the open-circuit condition between the gate and output network, the input remains the following:

$$\boxed{Z_i = R_G} \tag{9.23}$$

Z_o: The output impedance is defined by

$$Z_o = \left.\frac{V_o}{I_o}\right|_{V_i = 0}$$

Setting $V_i = 0$ V in Fig. 9.18 will result in the gate terminal being at ground potential (0 V). The voltage across R_G is then 0 V, and R_G has been effectively "shorted out" of the picture.

Applying Kirchhoff's current law will result in:

$$I_o + I_D = g_m V_{gs}$$

with $$V_{gs} = -(I_o + I_D)R_S$$

so that $$I_o + I_D = -g_m (I_o + I_D)R_S = -g_m I_o R_S - g_m I_D R_S$$

or $$I_o[1 + g_m R_S] = -I_D[1 + g_m R_S]$$

and $I_o = -I_D$ (the controlled current source $g_m V_{gs} = 0$ A for the applied conditions)

Since $$V_o = -I_D R_D$$

then $$V_o = -(-I_o)R_D = I_o R_D$$

and

$$\boxed{Z_o = \left.\frac{V_o}{I_o} = R_D\right|_{r_d = \infty\Omega}} \tag{9.24}$$

If r_d is included in the network, the equivalent will appear as shown in Fig. 9.19.

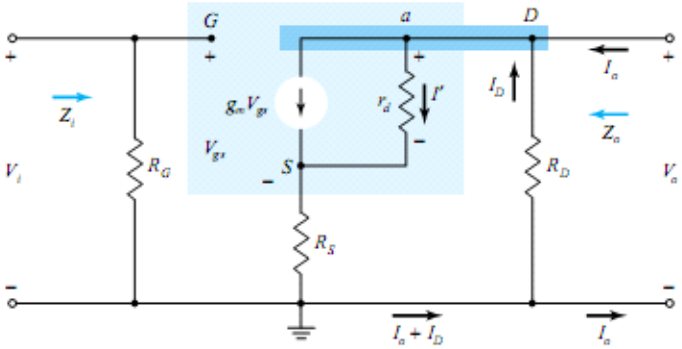


Figure 9.19 Including the effects of r_d in the self-bias JFET configuration.

Since
$$Z_o = \left.\frac{V_o}{I_o}\right|_{V_i = 0\text{ V}} = -\frac{I_D R_D}{I_o}$$

we should try to find an expression for I_o in terms of I_D.

Applying Kirchhoff's current law:

$$I_o = g_m V_{gs} + I_{r_d} - I_D$$

but
$$V_{r_d} = V_o + V_{gs}$$

and
$$I_o = g_m V_{gs} + \frac{V_o + V_{gs}}{r_d} - I_D$$

or
$$I_o = \left(g_m + \frac{1}{r_d}\right) V_{gs} - \frac{I_D R_D}{r_d} - I_D \text{ using } V_o = -I_D R_D$$

Now,
$$V_{gs} = -(I_D + I_o) R_S$$

so that
$$I_o = -\left(g_m + \frac{1}{r_d}\right)(I_D + I_o) R_S - \frac{I_D R_D}{r_d} - I_D$$

with the result that
$$I_o\left[1 + g_m R_s + \frac{R_S}{r_d}\right] = -I_D\left[1 + g_m R_S + \frac{R_S}{r_d} + \frac{R_D}{r_d}\right]$$

or
$$I_o = \frac{-I_D\left[1 + g_m R_S + \frac{R_S}{r_d} + \frac{R_D}{r_d}\right]}{1 + g_m R_S + \frac{R_S}{r_d}}$$

and $$Z_o = \frac{V_o}{I_o} = \frac{-I_D R_D}{\dfrac{-I_D\left(1 + g_m R_s + \dfrac{R_s}{r_d} + \dfrac{R_D}{r_d}\right)}{1 + g_m R_S + \dfrac{R_S}{r_d}}}$$

and finally, $$\boxed{Z_o = \frac{\left[1 + g_m R_S + \dfrac{R_S}{r_d}\right]}{\left[1 + g_m R_S + \dfrac{R_S}{r_d} + \dfrac{R_D}{r_d}\right]} R_D} \qquad (9.25a)$$

For $r_d \geq 10\, R_D$, $\left(1 + g_m R_S + \dfrac{R_S}{r_d}\right) >> \dfrac{R_D}{r_d}$ and $1 + g_m R_S + \dfrac{R_S}{r_d} + \dfrac{R_D}{r_d}$ $\cong 1 + g_m R_S + \dfrac{R_S}{r_d}$ and

$$\boxed{Z_o = R_D}_{r_d \geq 10 R_D} \qquad (9.25b)$$

A_v: For the network of Fig. 9.19, an application of Kirchhoff's voltage law on the input circuit will result in

$$V_i - V_{gs} - V_{R_S} = 0$$

$$V_{gs} = V_i - I_D R_S$$

The voltage across r_d using Kirchhoff's voltage law is

$$V_o - V_{R_S}$$

and

$$I' = \frac{V_o - V_{R_S}}{r_d}$$

so that an application of Kirchhoff's current law will result in

$$I_D = g_m V_{gs} + \frac{V_o - V_{R_S}}{r_d}$$

Substituting for V_{gs} from above and substituting for V_o and V_{R_S} we have

$$I_D = g_m[V_i - I_D R_S] + \frac{(-I_D R_D) - (I_D R_S)}{r_d}$$

so that

$$I_D\left[1 + g_m R_S + \frac{R_D + R_S}{r_d}\right] = g_m V_i$$

or

$$I_D = \frac{g_m V_i}{1 + g_m R_S + \frac{R_D + R_S}{r_d}}$$

The output voltage is then

$$V_o = -I_D R_D = -\frac{g_m R_D V_i}{1 + g_m R_S + \frac{R_D + R_S}{r_d}}$$

and

$$\boxed{A_v = \frac{V_o}{V_i} = -\frac{g_m R_D}{1 + g_m R_S + \frac{R_D + R_S}{r_d}}} \qquad (9.26)$$

Again, if $r_d \geq 10(R_D + R_S)$,

$$\boxed{A_v = \frac{V_o}{V_i} = -\frac{g_m R_D}{1 + g_m R_S}}_{r_d \geq 10(R_D + R_S)} \qquad (9.27)$$

Phase Relationship: The negative sign in Eq. (9.26) again reveals that a 180° phase shift will exist between V_i and V_o.

The self-bias configuration of Example 6.2 has an operating point defined by $V_{GS_Q} = -2.6$ V and $I_{D_Q} = 2.6$ mA, with $I_{DSS} = 8$ mA and $V_P = -6$ V. The network is redrawn as Fig. 9.20 with an applied signal V_i. The value of y_{os} is given as 20 μS.

(a) Determine g_m.
(b) Find r_d.
(c) Find Z_i.
(d) Calculate Z_o with and without the effects of r_d. Compare the results.
(e) Calculate A_v with and without the effects of r_d. Compare the results.

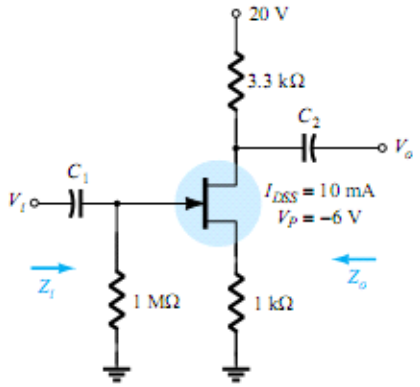


Figure 9.20 Network for Example 9.8.

Solution

(a) $g_{m0} = \dfrac{2I_{DSS}}{|V_P|} = \dfrac{2(8\text{ mA})}{6\text{ V}} = 2.67\text{ mS}$

$$g_m = g_{m0}\left(1 - \frac{V_{GS_Q}}{V_P}\right) = 2.67\text{ mS}\left(1 - \frac{(-2.6\text{ V})}{(-6\text{ V})}\right) = \mathbf{1.51\ mS}$$

(b) $r_d = \dfrac{1}{y_{os}} = \dfrac{1}{20\ \mu\text{S}} = \mathbf{50\ k\Omega}$

(c) $Z_i = R_G = \mathbf{1\ M\Omega}$

(d) With r_d:

$$r_d = 50\text{ k}\Omega > 10\,R_D = 33\text{ k}\Omega$$

Therefore,

$$Z_o = R_D = \mathbf{3.3\ k\Omega}$$

If $r_d = \infty\ \Omega$

$$Z_o = R_D = \mathbf{3.3\ k\Omega}$$

(e) With r_d:

$$A_v = \frac{-g_m R_D}{1 + g_m R_S + \dfrac{R_D + R_S}{r_d}} = \frac{-(1.51\text{ mS})(3.3\text{ k}\Omega)}{1 + (1.51\text{ mS})(1\text{ k}\Omega) + \dfrac{3.3\text{ k}\Omega + 1\text{ k}\Omega}{50\text{ k}\Omega}}$$

$$= \mathbf{-1.92}$$

Without r_d:

$$A_v = \frac{-g_m R_D}{1 + g_m R_S} = \frac{-(1.51\text{ mS})(3.3\text{ k}\Omega)}{1 + (1.51\text{ mS})(1\text{ k}\Omega)} = \mathbf{-1.98}$$

9.5 JFET VOLTAGE-DIVIDER CONFIGURATION

The popular voltage-divider configuration for BJTs can also be applied to JFETs as demonstrated in Fig. 9.21.

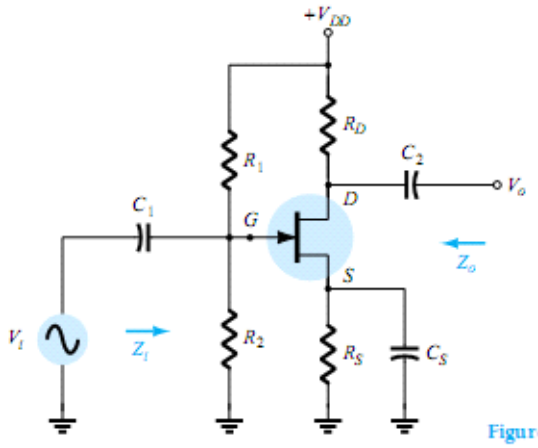


Figure 9.21 JFET voltage-divider configuration.

Substituting the ac equivalent model for the JFET will result in the configuration of Fig. 9.22. Replacing the dc supply V_{DD} by a short-circuit equivalent has grounded one end of R_1 and R_D. Since each network has a common ground, R_1 can be brought down in parallel with R_2 as shown in Fig. 9.23. R_D can also be brought down to ground but in the output circuit across r_d. The resulting ac equivalent network now has the basic format of some of the networks already analyzed.

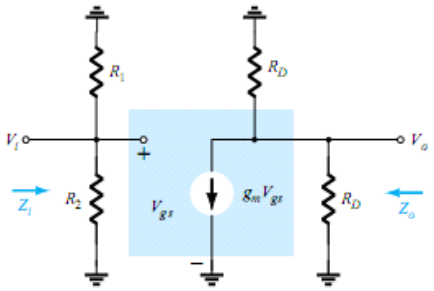


Figure 9.22 Network of Fig. 9.21 under ac conditions.

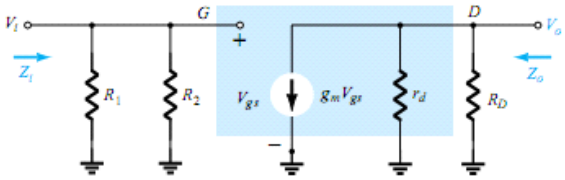


Figure 9.23 Redrawn network of Fig. 9.22.

Z_i: R_1 and R_2 are in parallel with the open-circuit equivalence of the JFET resulting in

$$\boxed{Z_i = R_1 \| R_2} \tag{9.28}$$

Z_o: Setting $V_i = 0$ V will set V_{gs} and $g_m V_{gs}$ to zero and

$$\boxed{Z_o = r_d \| R_D} \tag{9.29}$$

For $r_d \geq 10R_D$,

$$\boxed{Z_o \cong R_D}_{r_d \geq 10R_D} \tag{9.30}$$

A_v:

$$V_{gs} = V_i$$

and

$$V_o = -g_m V_{gs}(r_d \| R_D)$$

so that

$$A_v = \frac{V_o}{V_i} = \frac{-g_m V_{gs}(r_d \| R_D)}{V_{gs}}$$

and

$$\boxed{A_v = \frac{V_o}{V_i} = -g_m(r_d \| R_D)} \tag{9.31}$$

If $r_d \geq 10R_D$,

$$\boxed{A_v = \frac{V_o}{V_i} \cong -g_m R_D}_{r_d \geq 10R_D} \tag{9.32}$$

Note that the equations for Z_o and A_v are the same as obtained for the fixed-bias and self-bias (with bypassed R_S) configurations. The only difference is the equation for Z_i, which is now sensitive to the parallel combination of R_1 and R_2.

9.6 JFET SOURCE-FOLLOWER (COMMON-DRAIN) CONFIGURATION

The JFET equivalent of the BJT emitter-follower configuration is the source-follower configuration of Fig. 9.24. Note that the output is taken off the source terminal and, when the dc supply is replaced by its short-circuit equivalent, the drain is grounded (hence, the terminology common-drain).

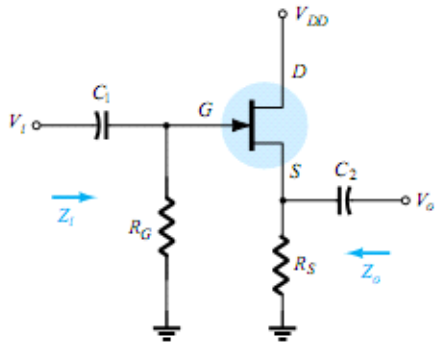


Figure 9.24 JFET source-follower configuration.

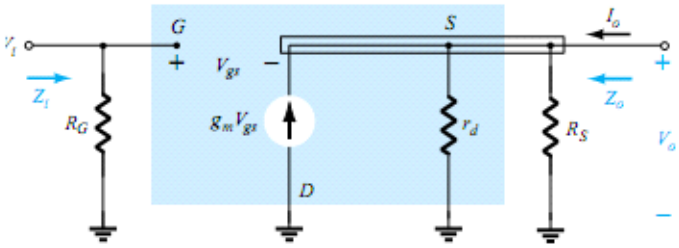


Figure 9.26 Network of Fig. 9.25 redrawn.

Z_i: Figure 9.26 clearly reveals that Z_i is defined by

$$\boxed{Z_i = R_G} \tag{9.33}$$

Z_o: Setting $V_i = 0$ V will result in the gate terminal being connected directly to ground as shown in Fig. 9.27. The fact that V_{gs} and V_o are across the same parallel network results in $V_o = -V_{gs}$.

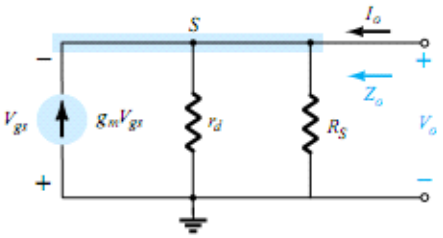


Figure 9.27 Determining Z_o for the network of Fig. 9.24.

Applying Kirchhoff's current law at node s,

$$I_o + g_m V_{gs} = I_{r_d} + I_{R_S}$$

$$= \frac{V_o}{r_d} + \frac{V_o}{R_S}$$

The result is

$$I_o = V_o\left[\frac{1}{r_d} + \frac{1}{R_S}\right] - g_m V_{gs}$$

$$= V_o\left[\frac{1}{r_d} + \frac{1}{R_S}\right] - g_m[-V_o]$$

$$= V_o\left[\frac{1}{r_d} + \frac{1}{R_S} + g_m\right]$$

and $$Z_o = \frac{V_o}{I_o} = \frac{V_o}{V_o\left[\frac{1}{r_d} + \frac{1}{R_S} + g_m\right]} = \frac{1}{\frac{1}{r_d} + \frac{1}{R_S} + g_m} = \frac{1}{\frac{1}{r_d} + \frac{1}{R_S} + \frac{1}{1/g_m}}$$

which has the same format as the total resistance of three parallel resistors. Therefore,

$$\boxed{Z_o = r_d \| R_S \| 1/g_m} \tag{9.34}$$

For $r_d \geq 10R_S$,

$$\boxed{Z_o \cong R_S \| 1/g_m}_{r_d \geq 10R_S} \tag{9.35}$$

A_v: The output voltage V_o is determined by

$$V_o = g_m V_{gs}(r_d \| R_S)$$

and applying Kirchhoff's voltage law around the perimeter of the network of Fig. 9.26 will result in

$$V_i = V_{gs} + V_o$$

and $$V_{gs} = V_i - V_o$$

so that $$V_o = g_m(V_i - V_o)(r_d \| R_S)$$

or $$V_o = g_m V_i(r_d \| R_S) - g_m V_o(r_d \| R_S)$$

and $$V_o[1 + g_m(r_d \| R_S)] = g_m V_i(r_d \| R_S)$$

so that $$\boxed{A_v = \frac{V_o}{V_i} = \frac{g_m(r_d \| R_S)}{1 + g_m(r_d \| R_S)}} \tag{9.36}$$

In the absence of r_d or if $r_d \geq 10R_S$,

$$\boxed{A_v = \frac{V_o}{V_i} \cong \frac{g_m R_S}{1 + g_m R_S}}_{r_d \geq 1}$$

lower BJT network).

Phase Relationship: Since A_v of Eq. (9.36) is a positive quantity, V_o and V_i are in phase for the JFET source-follower configuration.

EXAMPLE 9

A dc analysis of the source-follower network of Fig. 9.28 will result in $V_{GS_Q} = -2.86$ V and $I_{D_Q} = 4.56$ mA.

(a) Determining g_m.
(b) Find r_d.
(c) Determine Z_i.
(d) Calculate Z_o with and without r_d. Compare results.
(e) Determine A_v with and without r_d. Compare results.

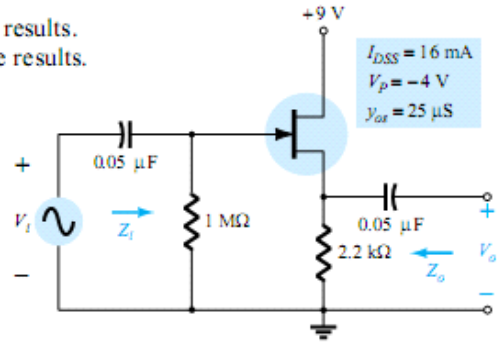


Figure 9.28 Network to be analyzed in Example 9.9.

(a) $g_{m0} = \dfrac{2I_{DSS}}{|V_P|} = \dfrac{2(16\text{ mA})}{4\text{ V}} = 8\text{ mS}$

$$g_m = g_{m0}\left(1 - \frac{V_{GS_Q}}{V_P}\right) = 8\text{ mS}\left(1 - \frac{(-2.86\text{ V})}{(-4\text{ V})}\right) = \mathbf{2.28\ mS}$$

(b) $r_d = \dfrac{1}{y_{os}} = \dfrac{1}{25\ \mu\text{S}} = \mathbf{40\ k\Omega}$

(c) $Z_i = R_G = \mathbf{1\ M\Omega}$

(d) With r_d:

$$\begin{aligned} Z_o = r_d \| R_S \| 1/g_m &= 40\text{ k}\Omega \| 2.2\text{ k}\Omega \| 1/2.28\text{ mS} \\ &= 40\text{ k}\Omega \| 2.2\text{ k}\Omega \| 438.6\ \Omega \\ &= \mathbf{362.52\ \Omega} \end{aligned}$$

revealing that Z_o is often relatively small and determined primarily by $1/g_m$. Without r_d:

$$Z_o = R_S \| 1/g_m = 2.2\text{ k}\Omega \| 438.6\ \Omega = \mathbf{365.69\ \Omega}$$

revealing that r_d typically has little impact on Z_o.

(e) With r_d:

$$A_v = \frac{g_m(r_d \| R_S)}{1 + g_m(r_d \| R_S)} = \frac{(2.28\text{ mS})(40\text{ k}\Omega \| 2.2\text{ k}\Omega)}{1 + (2.28\text{ mS})(40\text{ k}\Omega \| 2.2\text{ k}\Omega)}$$

$$\frac{(2.28\text{ mS})(2.09\text{ k}\Omega)}{1 + (2.28\text{ mS})(2.09\text{ k}\Omega)} = \frac{4.77}{1 + 4.77} = \mathbf{0.83}$$

which is less than 1 as predicted above.
Without r_d:

$$A_v = \frac{g_m R_S}{1 + g_m R_S} = \frac{(2.28\text{ mS})(2.2\text{ k}\Omega)}{1 + (2.28\text{ mS})(2.2\text{ k}\Omega)}$$

$$= \frac{5.02}{1 + 5.02} = \mathbf{0.83}$$

9.7 JFET COMMON-GATE CONFIGURATION

The last JFET configuration to be analyzed in detail is the common-gate configuration of Fig. 9.29, which parallels the common-base configuration employed with BJT transistors.

Substituting the JFET equivalent circuit will result in Fig. 9.30. Note the continuing requirement that the controlled source $g_m V_{gs}$ be connected from drain to source with r_d in parallel. The isolation between input and output circuits has obviously been lost since the gate terminal is now connected to the common ground of the network. In addition, the resistor connected between input terminals is no longer R_G but the resistor R_S connected from source to ground. Note also the location of the controlling voltage V_{gs} and the fact that it appears directly across the resistor R_S.

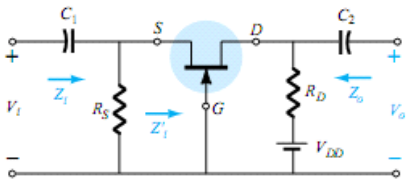


Figure 9.29 JFET common-gate configuration.

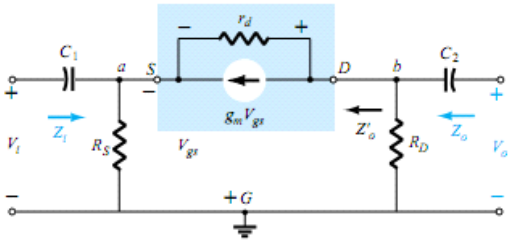


Figure 9.30 Network of Fig. 9.29 following substitution of JFET ac equivalent model.

Z_i: The resistor R_S is directly across the terminals defining Z_i. Let us therefore find the impedance Z_i' of Fig. 9.29, which will simply be in parallel with R_S when Z_i is defined.

The network of interest is redrawn as Fig. 9.31. The voltage $V' = -V_{gs}$. Applying Kirchhoff's voltage law around the output perimeter of the network will result in

$$V' - V_{r_d} - V_{R_D} = 0$$

and

$$V_{r_d} = V' - V_{R_D} = V' - I'R_D$$

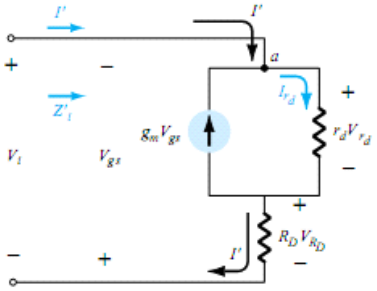


Figure 9.31 Determining Z_i' for the network of Fig. 9.29.

Applying Kirchhoff's current law at node a results in

$$I' + g_m V_{gs} = I_{r_d}$$

and

$$I' = I_{r_d} - g_m V_{gs} = \frac{(V' - I'R_D)}{r_d} - g_m V_{gs}$$

or

$$I' = \frac{V'}{r_d} - \frac{I'R_D}{r_d} - g_m[-V']$$

so that

$$I'\left[1 + \frac{R_D}{r_d}\right] = V'\left[\frac{1}{r_d} + g_m\right]$$

and

$$Z_i' = \frac{V'}{I'} = \frac{\left[1 + \frac{R_D}{r_d}\right]}{\left[g_m + \frac{1}{r_d}\right]} \tag{9.38}$$

or

$$Z_i' = \frac{V'}{I'} = \frac{r_d + R_D}{1 + g_m r_d}$$

and

$$Z_i = R_S \| Z_i'$$

results in

$$\boxed{Z_i = R_S \left\| \left[\frac{r_d + R_D}{1 + g_m r_d}\right]\right.} \tag{9.39}$$

If $r_d \geq 10R_D$, Eq. (9.38) permits the following approximation since $R_D/r_d \ll 1$ and $1/r_d \ll g_m$:

$$Z_i' = \frac{\left[1 + \frac{R_D}{r_d}\right]}{\left[g_m + \frac{1}{r_d}\right]} \cong \frac{1}{g_m}$$

and

$$\boxed{Z_i \cong R_S \| 1/g_m}_{r_d \geq 10R_D} \tag{9.40}$$

$\boldsymbol{Z_o}$: Substituting $V_i = 0$ V in Fig. 9.30 will "short-out" the effects of R_S and set V_{gs} to 0 V. The result is $g_m V_{gs} = 0$, and r_d will be in parallel with R_D. Therefore,

$$\boxed{Z_o = R_D \| r_d} \tag{9.41}$$

For $r_d \geq 10R_D$,

$$\boxed{Z_o \cong R_D}_{r_d \geq 10R_D} \tag{9.42}$$

A_v: Figure 9.30 reveals that

$$V_i = -V_{gs}$$

and

$$V_o = I_D R_D$$

The voltage across r_d is

$$V_{r_d} = V_o - V_i$$

and

$$I_{r_d} = \frac{V_o - V_i}{r_d}$$

Applying Kirchhoff's current law at node b in Fig. 9.30 results in

$$I_{r_d} + I_D + g_m V_{gs} = 0$$

and

$$I_D = -I_{rd} - g_m V_{gs}$$

$$= -\left[\frac{V_o - V_i}{r_d}\right] - g_m[-V_i]$$

$$I_D = \frac{V_i - V_o}{r_d} + g_m V_i$$

so that

$$V_o = I_D R_D = \left[\frac{V_i - V_o}{r_d} + g_m V_i\right] R_D$$

$$= \frac{V_i R_D}{r_d} - \frac{V_o R_D}{r_d} + g_m$$

and

$$V_o\left[1 + \frac{R_D}{r_d}\right] = V_i\left[\frac{R_D}{r_d} + g_m R_D\right]$$

with

$$\boxed{A_v = \frac{V_o}{V_i} = \frac{\left[g_m R_D + \frac{R_D}{r_d}\right]}{\left[1 + \frac{R_D}{r_d}\right]}} \tag{9.43}$$

For $r_d \geq 10R_D$, the factor R_D/r_d of Eq. (9.43) can be dropped as a good approximation and

$$\boxed{A_v = g_m R_D}_{r_d \geq 10R_D} \tag{9.44}$$

Phase Relationship: The fact that A_v is a positive number will result in an *in-phase* relationship between V_o and V_i for the common-gate configuration.

Although the network of Fig. 9.32 may not initially appear to be of the common-gate variety, a close examination will reveal that it has all the characteristics of Fig. 9.29. If $V_{GS_Q} = -2.2$ V and $I_{D_Q} = 2.03$ mA:

(a) Determine g_m.
(b) Find r_d.
(c) Calculate Z_i with and without r_d. Compare results.
(d) Find Z_o with and without r_d. Compare results.
(e) Determine V_o with and without r_d. Compare results.

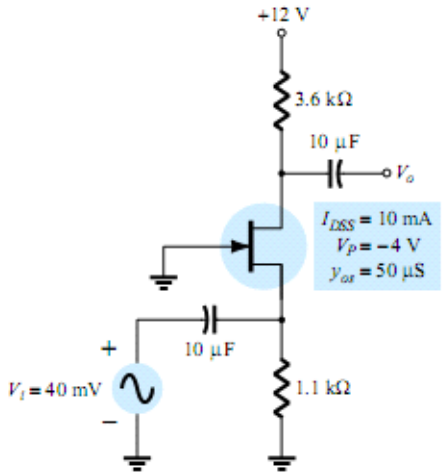


Figure 9.32 Network for Example 9.10.

(a) $g_{m0} = \dfrac{2I_{DSS}}{|V_P|} = \dfrac{2(10\text{ mA})}{4\text{ V}} = 5\text{ mS}$

$$g_m = g_{m0}\left(1 - \frac{V_{GS_Q}}{V_P}\right) = 5\text{ mS}\left(1 - \frac{(-2.2\text{ V})}{(-4\text{ V})}\right) = \mathbf{2.25\ mS}$$

(b) $r_d = \dfrac{1}{y_{os}} = \dfrac{1}{50\ \mu\text{S}} = \mathbf{20\ k\Omega}$

(c) With r_d:

$$Z_i = R_S \| \left[\frac{r_d + R_D}{1 + g_m r_d}\right] = 1.1\text{ k}\Omega \| \left[\frac{20\text{ k}\Omega + 3.6\text{ k}\Omega}{1 + (2.25\text{ ms})(20\text{ k}\Omega)}\right]$$
$$= 1.1\text{ k}\Omega \| 0.51\text{ k}\Omega = \mathbf{0.35\ k\Omega}$$

Without r_d:

$$Z_i = R_S \| 1/g_m = 1.1\ \text{k}\Omega \| 1/2.25\ \text{ms} = 1.1\ \text{k}\Omega \| 0.44\ \text{k}\Omega$$
$$= \mathbf{0.31\ k\Omega}$$

Even though the condition,

$$r_d \geq 10R_D = > 20\ \text{k}\Omega \geq 10(3.6\ \text{k}\Omega) = > 20\ \text{k}\Omega \geq 36\ \text{k}\Omega$$

is *not* satisfied, both equations result in essentially the same level of impedance. In this case, $1/g_m$ was the predominant factor.

(d) With r_d:

$$Z_o = R_D \| r_d = 3.6\ \text{k}\Omega \| 20\ \text{k}\Omega = \mathbf{3.05\ k\Omega}$$

Without r_d:

$$Z_o = R_D = \mathbf{3.6\ k\Omega}$$

Again the condition $r_d \geq 10R_D$ is *not* satisfied, but both results are reasonably close. R_D is certainly the predominant factor in this example.

(e) With r_d:

$$A_v = \frac{\left[g_m R_D + \dfrac{R_D}{r_d}\right]}{\left[1 + \dfrac{R_D}{r_d}\right]} = \frac{\left[(2.25\ \text{mS})(3.6\ \text{k}\Omega) + \dfrac{3.6\ \text{k}\Omega}{20\ \text{k}\Omega}\right]}{\left[1 + \dfrac{3.6\ \text{k}\Omega}{20\ \text{k}\Omega}\right]}$$
$$= \frac{8.1 + 0.18}{1 + 0.18} = \mathbf{7.02}$$

and $$A_v = \frac{V_o}{V_i} = \blacktriangleright\ V_o = A_v V_i = (7.02)(40\ \text{mV}) = \mathbf{280.8\ mV}$$

Without r_d:

$$A_v = g_m R_D = (2.25\ \text{mS})(3.6\ \text{k}\Omega) = \mathbf{8.1}$$

with $$V_o = A_v V_i = (8.1)(40\ \text{mV}) = \mathbf{324\ mV}$$

9.8 DEPLETION-TYPE MOSFETs

The fact that Shockley's equation is also applicable to depletion-type MOSFETs results in the same equation for g_m. In fact, the ac equivalent model for D-MOSFETs is exactly the same as that employed for JFETs as shown in Fig. 9.33.

The only difference offered by D-MOSFETs is that V_{GS_Q} can be positive for *n*-channel devices and negative for *p*-channel units. The result is that g_m can be greater than g_{m0} as demonstrated by the example to follow. The range of r_d is very similar to that encountered for JFETs.

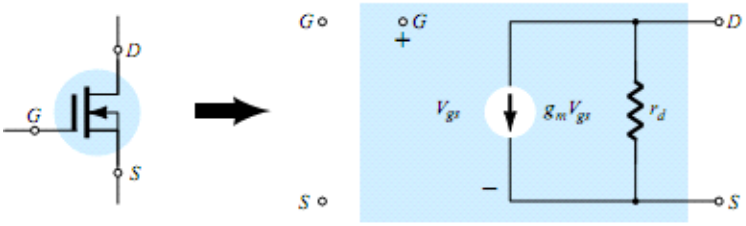
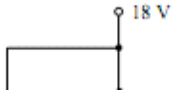
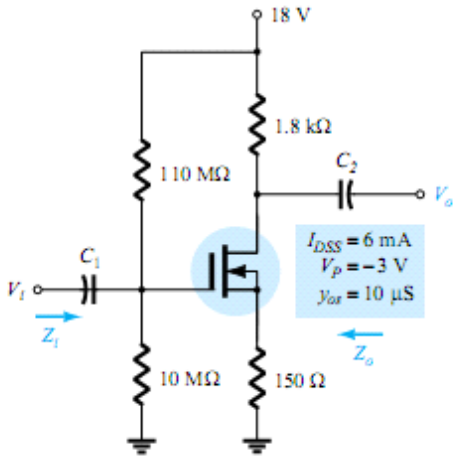


Figure 9.33 D-MOSFET ac equivalent model.

The network of Fig. 9.34 was analyzed as Example 6.8, resulting in $V_{GS_Q} = 0.35$ V and $I_{D_Q} = 7.6$ mA.

(a) Determine g_m and compare to g_{m0}.
(b) Find r_d.
(c) Sketch the ac equivalent network for Fig. 9.34.
(d) Find Z_i.
(e) Calculate Z_o.
(f) Find A_v.





(a) $g_{m0} = \dfrac{2I_{DSS}}{|V_P|} = \dfrac{2(6\text{ mA})}{3\text{ V}} = 4\text{ mS}$

$$g_m = g_{m0}\left(1 - \frac{V_{GS_Q}}{V_P}\right) = 4\text{ mS}\left(1 - \frac{(+0.35\text{ V})}{(-3\text{ V})}\right) = 4\text{ mS}(1 + 0.117) = \mathbf{4.47\text{ mS}}$$

(b) $r_d = \dfrac{1}{y_{os}} = \dfrac{1}{10\ \mu S} = \mathbf{100\ k\Omega}$

(c) See Fig. 9.35. Note the similarities with the network of Fig. 9.23. Equations (9.28) through (9.32) are therefore applicable.

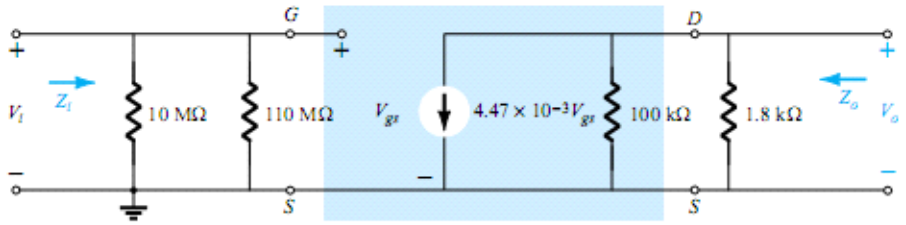


Figure 9.35 AC equivalent circuit for Fig. 9.34.

(d) Eq. (9.28): $Z_i = R_1 \| R_2 = 10\text{ M}\Omega \| 110\text{ M}\Omega = \mathbf{9.17\text{ M}\Omega}$

(e) Eq. (9.29): $Z_o = r_d \| R_D = 100\text{ k}\Omega \| 1.8\text{ k}\Omega = \mathbf{1.77\text{ k}\Omega} \cong R_D = \mathbf{1.8\text{ k}\Omega}$

(f) $r_d \geq 10R_D \rightarrow 100\text{ k}\Omega \geq 18\text{ k}\Omega$

Eq. (9.32): $A_v = -g_m R_D = -(4.47\text{ mS})(1.8\text{ k}\Omega) = \mathbf{8.05}$

9.9 ENHANCEMENT-TYPE MOSFETs

The enhancement-type MOSFET can be either an *n*-channel (*n*MOS) or *p*-channel (*p*MOS) device, as shown in Fig. 9.36. The ac small-signal equivalent circuit of either device is shown in Fig. 9.36, revealing an open-circuit between gate and drain-source channel and a current source from drain to source having a magnitude dependent on the gate-to-source voltage. There is an output impedance from drain to source r_d, which is usually provided on specification sheets as an admittance y_{os}. The device transconductance, g_m, is provided on specification sheets as the forward transfer admittance, y_{fs}.

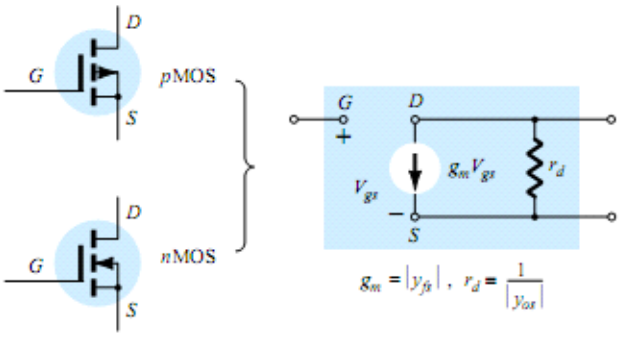


Figure 9.36 Enhancement MOSFET ac small-signal model.

In our analysis of JFETs, an equation for g_m was derived from Shockley's equation. For E-MOSFETs, the relationship between output current and controlling voltage is defined by

$$I_D = k(V_{GS} - V_{GS(\text{Th})})^2$$

Since g_m is still defined by

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

we can take the derivative of the transfer equation to determine g_m as an operating point. That is,

$$g_m = \frac{dI_D}{dV_{GS}} = \frac{d}{dV_{GS}} k(V_{GS} - V_{GS(\text{Th})})^2 = k\frac{d}{dV_{GS}}(V_{GS} - V_{GS(\text{Th})})^2$$

$$= 2k(V_{GS} - V_{GS(\text{Th})})\frac{d}{dV_{GS}}(V_{GS} - V_{GS(\text{Th})}) = 2k(V_{GS} - V_{GS(\text{Th})})(1 - 0)$$

and

$$\boxed{g_m = 2k(V_{GS_Q} - V_{GS(\text{Th})})} \tag{9.45}$$

Recall that the constant k can be determined from a given typical operating point on a specification sheet. In every other respect, the ac analysis is the same as that employed for JFETs or D-MOSFETs. Be aware, however, that the characteristics of an E-MOSFET are such that the biasing arrangements are somewhat limited.

9.10 E-MOSFET DRAIN-FEEDBACK CONFIGURATION

The E-MOSFET drain-feedback configuration appears in Fig. 9.37. Recall from dc calculations that R_G could be replaced by a short-circuit equivalent since $I_G = 0$ A and therefore $V_{R_G} = 0$ V. However, for ac situations it provides an important high impedance between V_o and V_i. Otherwise, the input and output terminals would be connected directly and $V_o = V_i$.

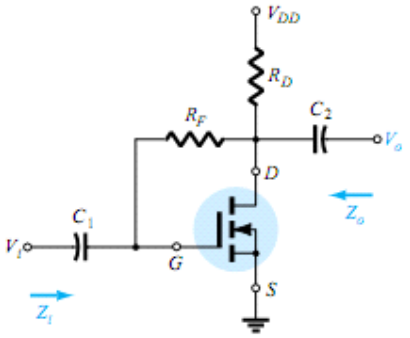


Figure 9.37 E-MOSFET drain-feedback configuration.

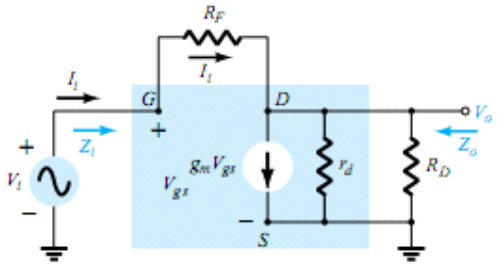


Figure 9.38 AC equivalent of the network of Fig. 9.37.

Substituting the ac equivalent model for the device will result in the network of Fig. 9.38. Note that R_F is not within the shaded area defining the equivalent model of the device but does provide a direct connection between input and output circuits.

Z_i: Applying Kirchhoff's current law to the output circuit (at node D in Fig. 9.38) results in

$$I_i = g_m V_{gs} + \frac{V_o}{r_d \| R_D}$$

and $$V_{gs} = V_i$$

so that $$I_i = g_m V_i + \frac{V_o}{r_d \| R_D}$$

or $$I_i - g_m V_i = \frac{V_o}{r_d \| R_D}$$

Therefore, $$V_o = (r_d \| R_D)(I_i - g_m V_i)$$

with $$I_i = \frac{V_i - V_o}{R_F} = \frac{V_i - (r_d \| R_D)(I_i - g_m V_i)}{R_F}$$

and $$I_i R_F = V_i - (r_d \| R_D) I_i + (r_d \| R_D) g_m V_i$$

so that $$V_i[1 + g_m(r_d \| R_D)] = I_i[R_F + r_d \| R_D]$$

and finally,

$$\boxed{Z_i = \frac{V_i}{I_i} = \frac{R_F + r_d \| R_D}{1 + g_m(r_d \| R_D)}} \tag{9.46}$$

A_v: Applying Kirchhoff's current law at node D of Fig. 9.38 will result in

$$I_i = g_m V_{gs} + \frac{V_o}{r_d \| R_D}$$

but

$$V_{gs} = V_i \text{ and } I_i = \frac{V_i - V_o}{R_F}$$

so that

$$\frac{V_i - V_o}{R_F} = g_m V_i + \frac{V_o}{r_d \| R_D}$$

and

$$\frac{V_i}{R_F} - \frac{V_o}{R_F} = g_m V_i + \frac{V_o}{r_d \| R_D}$$

so that

$$V_o\left[\frac{1}{r_d \| R_D} + \frac{1}{R_F}\right] = V_i\left[\frac{1}{R_F} - g_m\right]$$

and

$$A_v = \frac{V_o}{V_i} = \frac{\left[\frac{1}{R_F} - g_m\right]}{\left[\frac{1}{r_d \| R_D} + \frac{1}{R_F}\right]}$$

Typically, $R_F \gg r_d \| R_D$, so that

$$Z_i \cong \frac{R_F}{1 + g_m(r_d \| R_D)}$$

For $r_d \geq 10R_D$,

$$\boxed{Z_i \cong \frac{R_F}{1 + g_m R_D}}_{R_F \gg r_d \| R_D,\ r_d \geq 10R_D} \tag{9.47}$$

Z_o: Substituting $V_i = 0$ V will result in $V_{gs} = 0$ V and $g_m V_{gs} = 0$, with a short-circuit path from gate to ground as shown in Fig. 9.39. R_F, r_d, and R_D are then in parallel and

$$\boxed{Z_o = R_F \| r_d \| R_D} \tag{9.48}$$

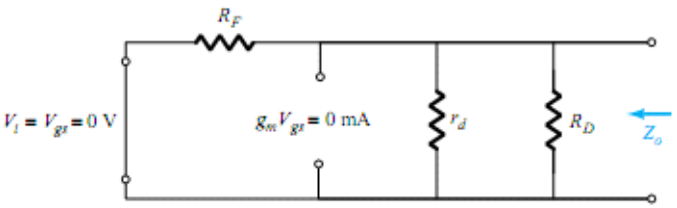


Figure 9.39 Determining Z_o for the network of Fig. 9.37.

Normally, R_F is so much larger than $r_d \| R_D$ that

$$Z_o \cong r_d \| R_D$$

and with $r_d \geq 10R_D$,

$$\boxed{Z_o \cong R_D}_{R_F \gg r_d \| R_D,\ r_d \geq 10R_D} \tag{9.49}$$

but
$$\frac{1}{r_d \| R_D} + \frac{1}{R_F} = \frac{1}{R_F \| r_d \| R_D}$$

and
$$g_m \gg \frac{1}{R_F}$$

so that
$$A_v = -g_m(R_F \| r_d \| R_D) \tag{9.50}$$

Since R_F is usually $>> r_d \| R_D$ and if $r_d \geq 10R_D$,

$$A_v \cong -g_m R_D \quad R_F \gg r_d \| R_D,\ r_d \geq 10R_D \tag{9.51}$$

Phase Relationship: The negative sign for A_v reveals that V_o and V_i are out of phase by 180°.

The E-MOSFET of Fig. 9.40 was analyzed in Example 6.11, with the result that $k = 0.24 \times 10^{-3}$ A/V^2, $V_{GS_Q} = 6.4$ V, and $I_{D_Q} = 2.75$ mA.

(a) Determine g_m.
(b) Find r_d.
(c) Calculate Z_i with and without r_d. Compare results.
(d) Find Z_o with and without r_d. Compare results.
(e) Find A_v with and without r_d. Compare results.

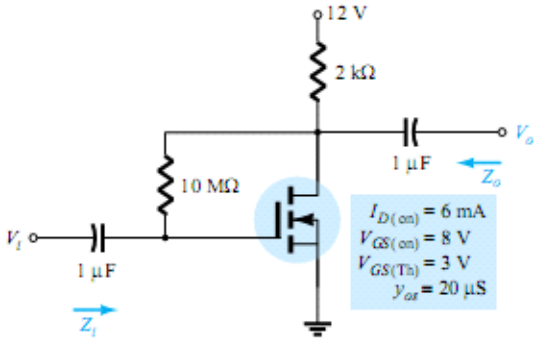


Figure 9.40 Drain-feedback amplifier from Example 6.11.

Solution

(a) $g_m = 2k(V_{GS_Q} - V_{GS(\text{Th})}) = 2(0.24 \times 10^{-3}\ \text{A/V}^2)(6.4\ \text{V} - 3\ \text{V})$

$$= \mathbf{1.63\ mS}$$

(b) $r_d = \dfrac{1}{y_{os}} = \dfrac{1}{20\ \mu\text{S}} = \mathbf{50\ k\Omega}$

(c) With r_d:

$$Z_i = \frac{R_F + r_d \| R_D}{1 + g_m(r_d \| R_D)} = \frac{10\ \text{M}\Omega + 50\ \text{k}\Omega \| 2\ \text{k}\Omega}{1 + (1.63\ \text{mS})(50\ \text{k}\Omega \| 2\ \text{k}\Omega)}$$

$$= \frac{10\ \text{M}\Omega + 1.92\ \text{k}\Omega}{1 + 3.13} = \mathbf{2.42\ M\Omega}$$

Without r_d:

$$Z_i \cong \frac{R_F}{1 + g_m R_D} = \frac{10\ \text{M}\Omega}{1 + (1.63\ \text{mS})(2\ \text{k}\Omega)} = \mathbf{2.53\ M\Omega}$$

revealing that since the condition $r_d \geq 10R_D = 50\ \text{k}\Omega \geq 40\ \text{k}\Omega$ is satisfied, the results for Z_o with or without r_d will be quite close.

(d) With r_d:

$$Z_o = R_F \| r_d \| R_D = 10\ \text{M}\Omega \| 50\ \text{k}\Omega \| 2\ \text{k}\Omega = 49.75\ \text{k}\Omega \| 2\ \text{k}\Omega$$

$$= \mathbf{1.92\ k\Omega}$$

Without r_d:

$$Z_o \cong R_D = \mathbf{2\ k\Omega}$$

again providing very close results.

(e) With r_d:

$$A_v = -g_m(R_F \| r_d \| R_D)$$

$$= -(1.63\ \text{mS})(10\ \text{M}\Omega \| 50\ \text{k}\Omega \| 2\ \text{k}\Omega)$$

$$= -(1.63\ \text{mS})(1.92\ \text{k}\Omega)$$

$$= \mathbf{-3.21}$$

Without r_d:

$$A_v = -g_m R_D = -(1.63\ \text{mS})(2\ \text{k}\Omega)$$

$$= \mathbf{-3.26}$$

which is very close to the above result.

9.12 DESIGNING FET AMPLIFIER NETWORKS

Design problems at this stage are limited to obtaining a desired dc bias condition or ac voltage gain. In most cases, the various equations developed are used "in reverse" to define the parameters necessary to obtain the desired gain, input impedance, or output impedance. To avoid unnecessary complexity during the initial stages of the design, the approximate equations are often employed because some variation will occur when calculated resistors are replaced by standard values. Once the initial design is completed, the results can be tested and refinements made using the complete equations.

Throughout the design procedure be aware that although superposition permits a separate analysis and design of the network from a dc and an ac viewpoint, a parameter chosen in the dc environment will often play an important role in the ac response. In particular, recall that the resistance R_G could be replaced by a short-circuit equivalent in the feedback configuration because $I_G \cong 0$ A for dc conditions, but for the ac analysis, it presents an important high impedance path between V_o and V_i. In addition, recall that g_m is larger for operating points closer to the I_D axis ($V_{GS} = 0$ V), requiring that R_S be relatively small. In the unbypassed R_S network, a small R_S will also contribute to a higher gain, but for the source-follower, the gain is reduced from its maximum value of 1. In total, simply keep in mind that network parameters can affect the dc and ac levels in different ways. Often a balance must be made between a particular operating point and its impact on the ac response.

In most situations, the available dc supply voltage is known, the FET to be employed has been determined, and the capacitors to be employed at the chosen frequency are defined. It is then necessary to determine the resistive elements necessary to establish the desired gain or impedance level. The next three examples will determine the required parameters for a specific gain.

EXAMPLE 9.13 Design the fixed-bias network of Fig. 9.43 to have an ac gain of 10. That is, determine the value of R_D.

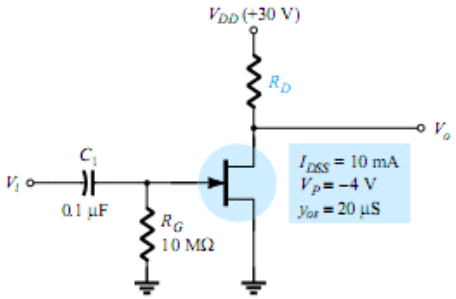


Figure 9.43 Circuit for desired voltage gain in Example 9.13.

Solution

Since $V_{GS_Q} = 0$ V, the level of g_m is g_{m0}. The gain is therefore determined by

$$A_v = -g_m(R_D \| r_d) = -g_{m0}(R_D \| r_d)$$

with

$$g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{2(10 \text{ mA})}{4 \text{ V}} = 5 \text{ mS}$$

The result is

$$-10 = -5 \text{ mS}(R_D \| r_d)$$

and

$$R_D \| r_d = \frac{10}{5 \text{ mS}} = 2 \text{ k}\Omega$$

From the device specifications,

$$r_d = \frac{1}{y_{os}} = \frac{1}{20 \times 10^{-6} \text{ S}} = 50 \text{ k}\Omega$$

Substituting, we find

$$R_D \| r_d = R_D \| 50 \text{ k}\Omega = 2 \text{ k}\Omega$$

and

$$\frac{R_D(50 \text{ k}\Omega)}{R_D + 50 \text{ k}\Omega} = 2 \text{ k}\Omega$$

or

$$50R_D = 2(R_D + 50 \text{ k}\Omega) = 2R_D + 100 \text{ k}\Omega$$

with

$$48R_D = 100 \text{ k}\Omega$$

and

$$R_D = \frac{100 \text{ k}\Omega}{48} \cong 2.08 \text{ k}\Omega$$

The closest standard value is **2 kΩ** (Appendix C), which would be employed for this design.

The resulting level of V_{DS_Q} would then be determined as follows:

$$V_{DS_Q} = V_{DD} - I_{D_Q}R_D = 30 \text{ V} - (10 \text{ mA})(2 \text{ k}\Omega) = \mathbf{10 \text{ V}}$$

The levels of Z_i and Z_o are set by the levels of R_G and R_D, respectively. That is,

$$Z_i = R_G = \mathbf{10 \text{ M}\Omega}$$

$$Z_o = R_D \| r_d = 2 \text{ k}\Omega \| 50 \text{ k}\Omega = \mathbf{1.92 \text{ k}\Omega} \cong R_D = 2 \text{ k}\Omega.$$

Choose the values of R_D and R_S for the network of Fig. 9.44 that will result in a gain of 8 using a relatively high level of g_m for this device defined at $V_{GS_Q} = \frac{1}{4}V_P$.

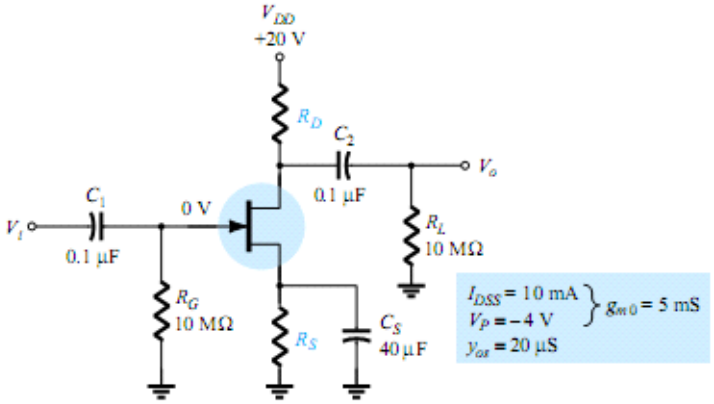


Figure 9.44 Network for desired voltage gain in Example 9.14.

The operating point is defined by

$$V_{GS_Q} = \frac{1}{4}V_P = \frac{1}{4}(-4\text{ V}) = -1\text{ V}$$

and $$I_D = I_{DSS}\left(1 - \frac{V_{GS_Q}}{V_P}\right)^2 = 10\text{ mA}\left(1 - \frac{(-1\text{ V})}{(-4\text{ V})}\right)^2 = 5.625\text{ mA}$$

Determining g_m,

$$g_m = g_{m0}\left(1 - \frac{V_{GS_Q}}{V_P}\right)$$

$$= 5\text{ mS}\left(1 - \frac{(-1\text{ V})}{(-4\text{ V})}\right) = 3.75\text{ mS}$$

The magnitude of the ac voltage gain is determined by

$$|A_v| = g_m(R_D \| r_d)$$

Substituting known values will result in

$$8 = (3.75\text{ mS})(R_D \| r_d)$$

so that $$R_D \| r_d = \frac{8}{3.75\text{ mS}} = 2.13\text{ k}\Omega$$

The level of r_d is defined by

$$r_d = \frac{1}{y_{os}} = \frac{1}{20\ \mu\text{S}} = 50\text{ k}\Omega$$

and $$R_D \| 50\text{ k}\Omega = 2.13\text{ k}\Omega$$

with the result that

$$R_D = \mathbf{2.2\ k\Omega}$$

which is a standard value.

The level of R_S is determined by the dc operating conditions as follows:

$$V_{GS_Q} = -I_D R_S$$

$$-1\text{ V} = -(5.625\text{ mA})R_S$$

and $$R_S = \frac{1\text{ V}}{5.625\text{ mA}} = 177.8\ \Omega$$

The closest standard value is 180 Ω. In this example, R_S does not appear in the ac design because of the shorting effect of C_S.

Determine R_D and R_S for the network of Fig. 9.44 to establish a gain of 8 if the bypass capacitor C_S is removed.

Solution

V_{GS_Q} and I_{D_Q} are still -1 V and 5.625 mA, and since the equation $V_{GS} = -I_D R_S$ has not changed, R_S continues to equal the standard value of **180 Ω** obtained in Example 9.14.

The gain of an unbypassed self-bias configuration is

$$A_v = -\frac{g_m R_D}{1 + g_m R_S}$$

For the moment it is assumed that $r_d \geq 10(R_D + R_S)$. Using the full equation for A_v at this stage of the design would simply complicate the process unnecessarily.

Substituting (for the specified magnitude of 8 for the gain),

$$|8| = \left| \frac{-(3.75 \text{ mS})R_D}{1 + (3.75 \text{ mS})(180\ \Omega)} \right| = \frac{(3.75 \text{ mS})R_D}{1 + 0.675}$$

and

$$8(1 + 0.675) = (3.75 \text{ mS})R_D$$

so that

$$R_D = \frac{13.4}{3.75 \text{ mS}} = 3.573 \text{ k}\Omega$$

with the closest standard value at **3.6 kΩ.**

We can now test the condition:

$$r_d \geq 10(R_D + R_S)$$

$$50 \text{ k}\Omega \geq 10(3.6 \text{ k}\Omega + 0.18 \text{ k}\Omega) = 10(3.78 \text{ k}\Omega)$$

and

$$50 \text{ k}\Omega \geq 37.8 \text{ k}\Omega$$

which is satisfied—the solution stands!