S J P N Trust's

HirasugarInstitute ofTechnology, Nidasoshi.

Inculcating Values, Promoting Prosperity

Approved by AICTE, Recognized by Govt. of Karnataka and Affiliated to VTU Belagavi.

EEE Dept.

Exam.

Internal Assessment

ODD SEM(2018-19

FIRST INTERNAL ASSESSMENT

Sem :V
Date:18/09/2018

Sub: Microcontroller
Time: 11:00AM-12.00PM

Sub. Code: 15EE52
Max. Marks: 25

Note: Answer two full questions, draw sketches wherever necessary.

Q. No		Discription of Question	Marks	CO	RBT Level
1	a	With neat block diagram, explain the function of each block of 8051 microcontroller architecture.	7	302.1	L1
	b	Explain the addressing modes of 8051 microcontroller with an example.	6	302.1	L1
		OR			
2	a	Discuss the need of Stack memory in 8051 microcontroller. How stack is operated in 8051 miccrocontroller? What is the default location of stack?	7	302.1	L2
	b	Draw the pin diagram of 8051. Also describe the role of I/O ports.	6	302.1	L2
3	a	Explain the following instructions of 8051 with examples. i) XCHD A,@Ri ii) ADD A, @Ri iii) MOVC A, @A+DPTR iv) CJNE A,iram addr, rel addr	6	302.2	L2
	b	Differentiate between LJMP, AJMP and SJMP instructions.	6	302.2	L2
		OR			
4	a	Write an ALP to exchange 06 numbers from 50H to 60H internal memory locations.	6	302.2	L3

	b	Analyze the program and write the comment line on every instruction.
		MOV R5, #30H
		MOV A, #44H
		ADD A, R5
		MOV R4, A
		PUSH 4
		PUSH 5
		POP 6
			6	302.2	L3

8.9.18

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E & E Dept | Exam | IA Scheme | 2018-19 (Odd)

SCHEME OF EVALUATION IA - FIRST

SEM: V | SUBJECT: Microcontroller | SUBJECT CODE: 15EE52 | DATE: 15/9/2018

Q.No.	Bits	DESCRIPTION	Marks	CO's
		Scheme		
1	(a)	For neat correct block diagram ———	03	
		for Explanation ———	04	
			07	
	(b)	For Register addressing mode Explanation with Ex -	01	
		For Immediate " " " " " " -	01	
		For Direct " " " " " " -	01	
		For Indirect " " " " " " -	01	
		For Indexed " " " " " " -	02	
2	(a)	Need of stack memory in 8051 ———	06	
		Operation of stack Explanation ———	02	
		Default location of stack pointer ———	04	
			01	
	(b)	For the Pin diagram of 8051 ———	07	
		Role of each I/O port ———	03	
			03	
			06M	
3.	(a)	For Every instruction Explanation 1.5M x 4	06M	
	(b)	At least two points regarding AJMP, LJMP, SJMP 02x3 = 06M	06M	
4	(a)	For correct input and output ———	01M	
		For complete correct program ———	05M	
			06M	
	(b)	For Every correct instruction Explanation 1M 01x6 = 6M	06M	

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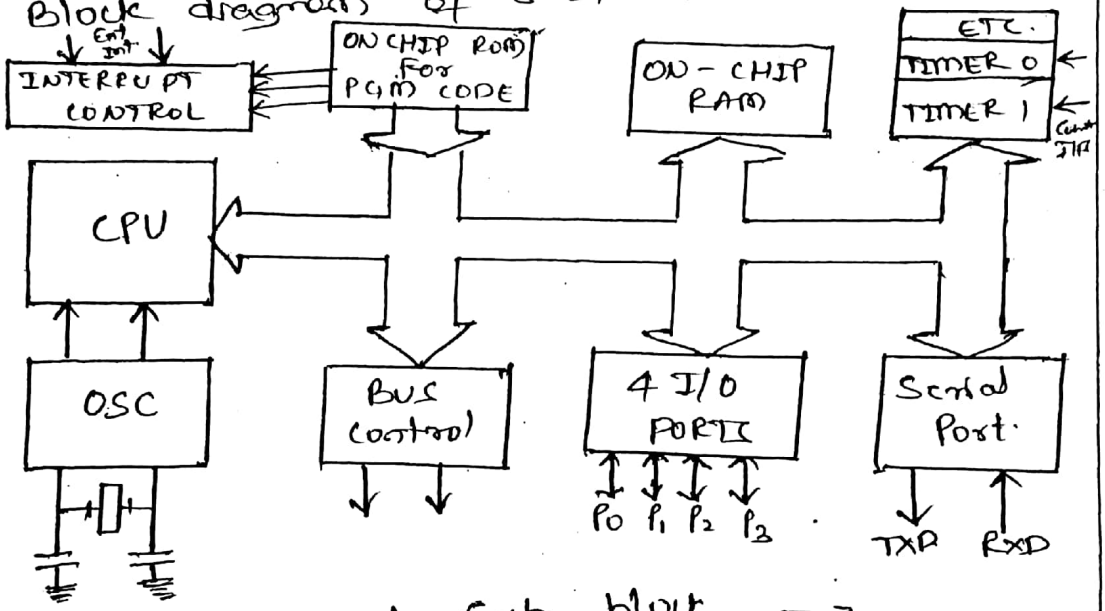
SCHEME OF EVALUATION IA - FIRST

SEM: V | SUBJECT: Microcontroller | SUBJECT CODE: 15EE52 | DATE: 15/9/18

Q.No.	Bits	DESCRIPTION	Marks	CO's

Solution

1 (a) Block diagram of 8051 Microcontroller.



Explanation of each block →

(b) Addressing Modes of 8051

(1) Immediate addressing mode → MOV R0, #05H
(2) Register " " → MOV A, R3
(3) Direct " " → MOV A, 50H
(4) Indirect " " → MOV A, @R1
(5) Indexed " " → MOVC A, @A+PC

2) (a) Need of stack memory

As CPU of 8051 has limited number of registers to store the information temporarily stack memory is used.

Default address of stack pointer is 07.

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SCHEME OF EVALUATION IA -

SEM: V | SUBJECT: Microcontroller | SUBJECT CODE: 15EE52 | DATE: 15/9/18

Q.No.	Bits	DESCRIPTION	Marks	CO's

Stack Operation

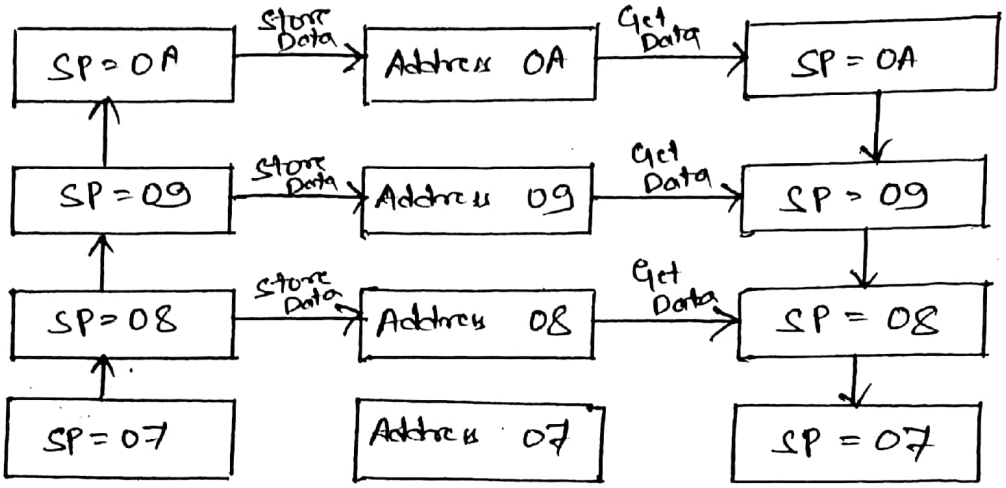

fig:- Stack Operation

2 (b)

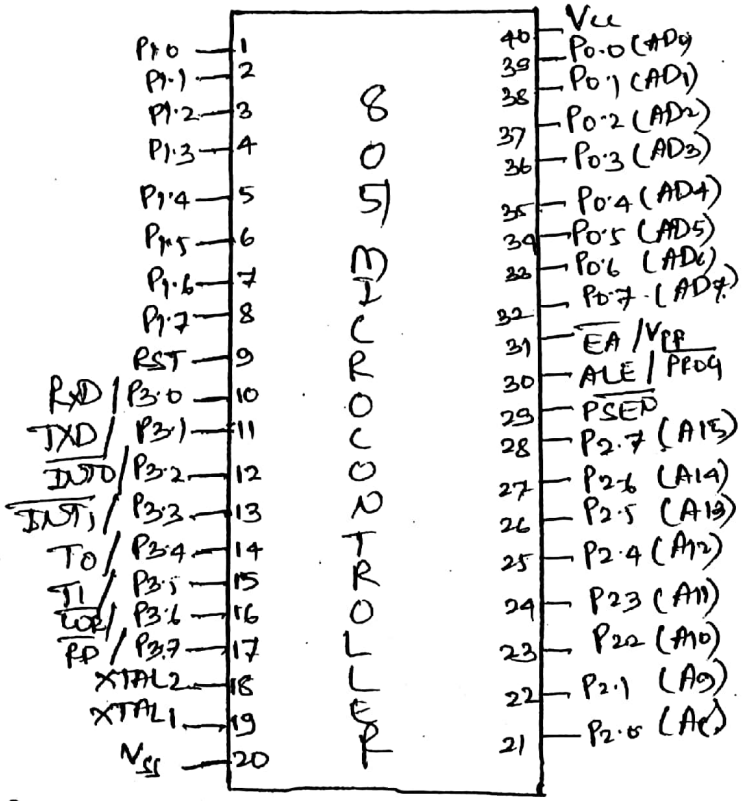

fig: Pin Diagram of 8051

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SCHEME OF EVALUATION IA -

SEM: | SUBJECT: | SUBJECT CODE: | DATE: | Page No : 3 / 6

Q.No.	Bits	DESCRIPTION	Marks	CO's
2	(b)	continued Port 0:- Is used as multiplexed address & data by Port 1:- General purpose port. All the pins of Port1 can be used for general purpose (interfacing) Port 2:- It is high order address bus where all the pins are also used as IO pins Port 3:- Its a special purpose port. where every pin of port 3 are used for one specific task.		
3	(a)			
	(i)	XCHD A, @Ri → Exchang digit. Exchanges lower nibble of accumulator with indirectly addressed register bit. Higher nibble is unaffected. Ex:- XCHD A, @R0		
	(ii)	ADD A, @Ri → Add the content of accumulator with content of indirectly address register (memory) & result is again saved in accumulator Ex ADD A, @R1		
	(iii)	MOVC A, @A+DPTR Here content of A is added with the DPTR content of DPTR that result is taken as address the source data. The content of that address transferred to accumulator		
	(iv)	CJNE A, iram addr, rel addr. The content of internal ram address and relative address are compared & if not equal then jumps to specified location otherwise jumps to next inst. Ex CJNE A, 50, 30H.		

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SCHEME OF EVALUATION IA -

SEM: V | SUBJECT: Microcontroller | SUBJECT CODE: 15EE52 | DATE: 15/9/18 | Page No : 5/6

Q.No.	Bits	DESCRIPTION	Marks	CO's
3	b) (5)	Difference between LJMP, AJMP, SJMP		

LJMP	AJMP	SJMP
1) Long Jump.	1) Absolute jump	1) Short jump
2) Jumps Anywhere from memory	2) Jumps within 2K byte of m/m	2) Jumps within -128 - +128 bytes of m/m
3) Range - ~~only 2K~~ bytes 0000H-FFFFH	3) Range - 2K bytes of memory	3) -128 to +127 bytes

4 (a) ALP to Exchange 06 numbers from 50H to 60H memory locations.

```
        ORG 0000H
        LJMP 8000H
        ORG 8000H
        MOV R0, #50H
        MOV R1, #60H
        MOV R4, #06H
UP:     MOV A, @R0
        MOV R6, A
        MOV A, @R1
        MOV @R0, A
        MOV A, R6
        MOV @R1, A
        INC R0
        INC R1
        DJNZ R4, UP
        LCALL 0003H.
```

I/P

50H = 05H, 60H = 2H
51H = 08H, 61H = 06H
52H = 0AH, 62H = 0BH
53H = 23H, 63H = A3H
54H = 65H, 64H = B5H
55H = 35H, 65H = C5H

O/P

50H = 2H	60H = 05H
51H = 6H	61H = 08H
52H = B4	62H = 0AH
53H = A3H	63H = 23H
54H = B5H	64H = 65H
55H = C5H	65H = 35H

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SCHEME OF EVALUATION IA -

SEM: V | SUBJECT: Microcontroller | SUBJECT CODE: 15EE52 | DATE: 15/9/18

Q.No.	Bits	DESCRIPTION	Marks	CO's
4	(b)	Comment on Every instruction		

MOV R_5, #30H || * 30H is loaded into R_0
$R_0 = 30H$

MOV A, #44H || * 44H is loaded into accumulator
$A = 44H$

ADD A, R_5 || * Content of accumulator is added with content of R_5
$A = A + R_5$

MOV R_4, A || * Content of accumulator is copied into register R_4

PUSH 4 || * Push the content of R_4 on top of stack SP = 08H
08H = 74H

PUSH 5 || * Push the content of R_5 on top of stack SP = 09H
09H = 30H.

POP 6 || * Pop the top content of stack i.e 09H = 30H into register R_6 = 30H.

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