S J P N Trust's

HirasugarInstituteofTechnology, Nidasoshi.

Inculcating Values, Promoting Prosperity

Approved by AICTE, Recognized by Govt. of Karnataka and Affiliated to VTU Belagavi.

E & E Dept.
Exam.
Internal Assessment
Even Sem(2017-18)

FIRST INTERNAL ASSESSMENT

Sem: IV | Sub: Operastional Amplifier & IC's | Sub. Code: 15EE46

Date: 07/03/2018 | Time: 03:00 PM to 04:00 PM | Max. Marks: 25

Note: Answer two full questions, draw sketches wherever necessary.

Q. No		Discription of Question	Marks	CO	RBT Level
1	a	An op-amp inverting amplifier has resistors of R_F= 22KΩ and R_1= 270Ω, calculate the output voltage produced by a 50mV input.	3	214.1	L2
	b	With circuit diagram, explain the operation of difference amplifier. Also show that the output is difference between two inputs with the help of equations.	5	214.1	L1,L2
	c	It is observed that when the op-amp is connected in non-inverting mode the voltage at feedback terminal is zero. Discuss the concept with a neat sketch.	5	214.1	L2
		OR			
2	a	For a non-inverting amplifier configuration make certain adjustments such that the output of the circuit should be same as that of input signal applied. Draw the circuit and discuss in brief.	3	214.1	L1,L2
	b	A Capacitor coupled non-inverting amplifier is to have A_v= 90 and V_0= 3V. The load resistance is 10KΩ and the lower cutoff frequency is to be 70 Hz. Design a suitable circuit.	4	214.1	L3
	c	With neat circuit diagram and waveforms explain the operation of op-amp in two different modes.	6	214.1	L2
3	a	Draw the block diagram of op-amp and explain in brief.	6	214.1	L1,L2
	b	Draw and explain capacitor coupled non inverting amplifier. Also suggest the suitable modifications to get high Zin for the same circuit.	6	214.1	L2
		OR			
4	a	Derive the closed loop voltage gain equation for the voltage series feedback amplifier.	6	214.1	L2
	b	For the non-inverting amplifier using single supply Ria = 50Ω = RO, Ci = C1 = 0.1μF. R1 = R2= R3= 100kΩ, Rf = 1MΩ, Vcc = +15V, Af = 11, uGB = 1MHz. Calculate bandwidth of amplifier. Draw the circuit diagram.	6	214.1	L2,L3

Course Coordinator **Module Coordinator** **HOD**

SCHEME OF EVALUATION

Sem : 4 | Subject : OALI | Sub Code : 15EE46 | Date : 04.03.18.

Q. No.	Bit	Description	Marks	CO's
1	a.	output voltage — 1M. circuit — 2M.		
	b.	Diff. amplr. circuit — 2M op's — 1M o/p eq^n — 2M		
	c.	virtual ground + opr + circuit 2+1+2M.		
2	a.	voltage follower circuit + op^n 1+2M		
	b.	calculation of element value + circuit 3+1M.		
	c.	inv mode Non-inv. circuit + op^n + w/f. 2+2+2M		
3	a.	Block Diagram + op^n 2+4M.		
	b.	cap coupled non-inv amp — 4M — High Z_{in} — 2M.		
4	a.	Voltage - series Fb. amp. — Gain — 6M		
	b.	Band width — 5M Circuit — 1M		

—— × ——

1(a) $R_F = 22K\Omega$ $R_1 = 270\Omega$

$V_i = 50mV$.

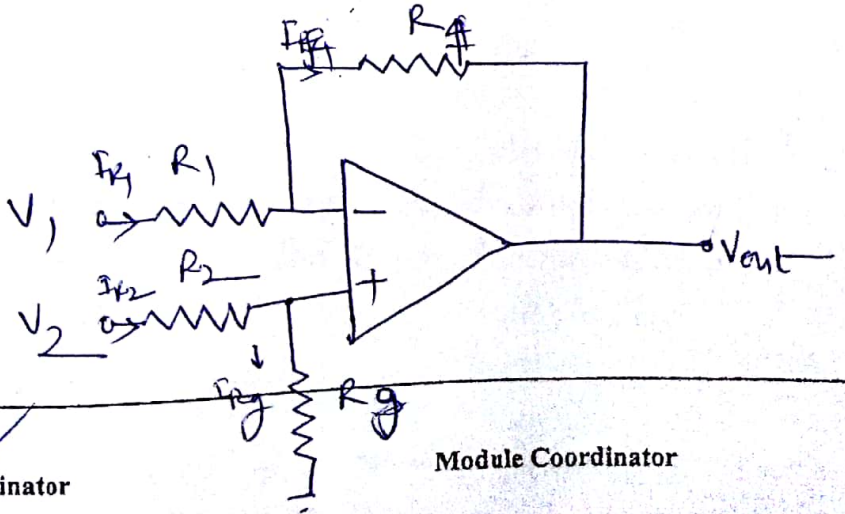
$\therefore V_{out} = Gain \cdot V_{in}$.

For inverting amplifier — $Gain = -\frac{R_f}{R_1} =$

$\therefore Gain = -22K/270 = 81.48$

$\therefore V_{out} = 81.48 * 50m = 4.07V$

(b)



Course Coordinator | Module Coordinator | HOD

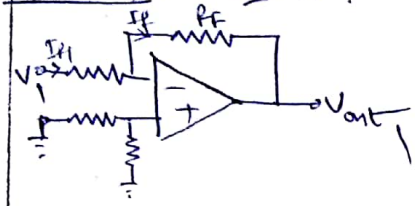
SCHEME OF EVALUATION

Sem : | Subject : | Sub Code : | Date :

Q. No.	Bit	Description	Marks	CO's

Using Superposition Theorem;

case(i): $V_2 = 0$

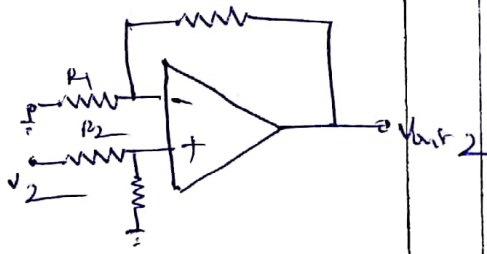


Here $I_{R_1} = I_{RF}$

$\therefore \frac{V_1}{R_1} = \frac{0 - V_{out_1}}{R_F}$

$\therefore V_{out_1} = -\frac{R_F}{R_1} \cdot V_1$

case (ii): $V_1 = 0$



using Vg divider rule

$V_- = V_{out_2} * \frac{R_1}{R_1 + R_F}$

$V_+ = V_2 * \frac{R_g}{R_2 + R_g}$

WKT $V_+ = V_-$ $\therefore$

$\therefore V_{out_2} = \frac{R_1 + R_F}{R_1} \cdot \frac{R_g}{R_2 + R_g} \cdot V_2$

$\therefore V_{out} = V_{out_1} + V_{out_2}$

$\therefore V_{out} = V_2 \frac{R_g}{R_2 + R_g} \cdot \frac{R_1 + R_f}{R_1} - \frac{R_F}{R_1} \cdot V_1$

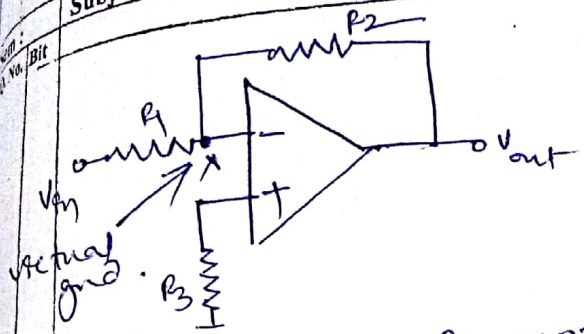
IF $R_1 = R_2 = R_f = R_g$

$\therefore V_{out} = V_2 - V_1$

(c) Virtual Grounding.

when op-amp is connected in ~~non~~ inv. mode the non-inv terminal is directly connected to gnd.

Course Coordinator | Module Coordinator | HOD



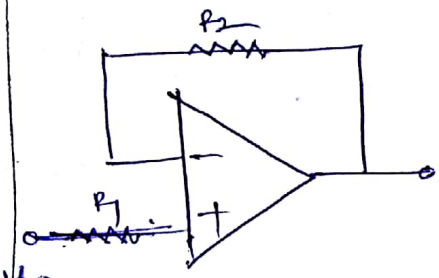
as $V_+ = V_-$

the V_{in} @ inv terminal is also zero.

the terminal is not connected to gnd but still V_{in} @ that part is zero so called virtual gnd.

→

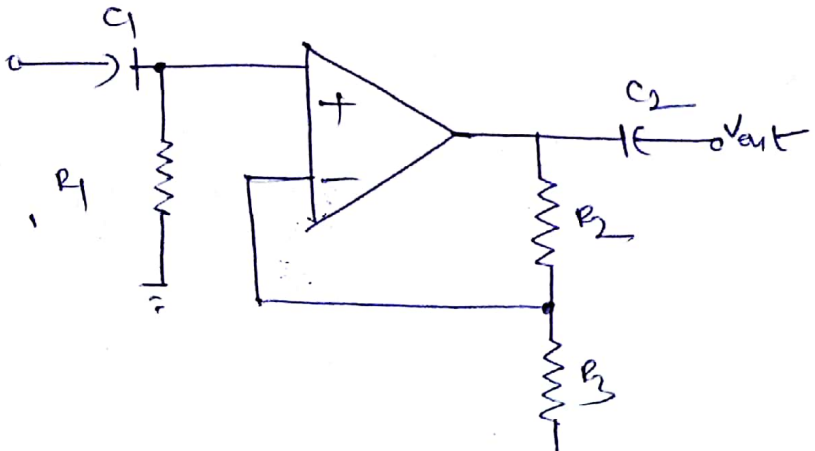
2 (a) It is voltage follower ckt.



* It is a non-inv amp.
* here $R_1 = R_2 = 0$.
* ckt directly short circuited to V_{in}.
* as the gain is 1. $\therefore V_o = V_{in}$

→

(b) Capacitor coupled Non-inv. amp.



W.K.T. $R_{1(max)} = \frac{0.1 V_{BE}}{I_{max}} = \frac{0.1 * 0.7}{500\mu} = 140\Omega$

Std 120Ω

Course Coordinator | Module Coordinator | HOD

SCHEME OF EVALUATION

Sem : | Subject : | Sub Code : | Date :

Q. No.	Bit	Description	Marks	CO's

we have $V_o = A_v \cdot V_i$

$\therefore V_i = \frac{V_o}{A_v} = \frac{3}{90} = 33.33mV$

$R_3 = \frac{V_i}{I_2}$

$\therefore R_3 = \frac{33.33m}{50\mu} = 667\Omega$ | 670Ω

$\therefore I_2 = \frac{V_i}{R_3} = \frac{33.33m}{670} = 49.75\mu A$

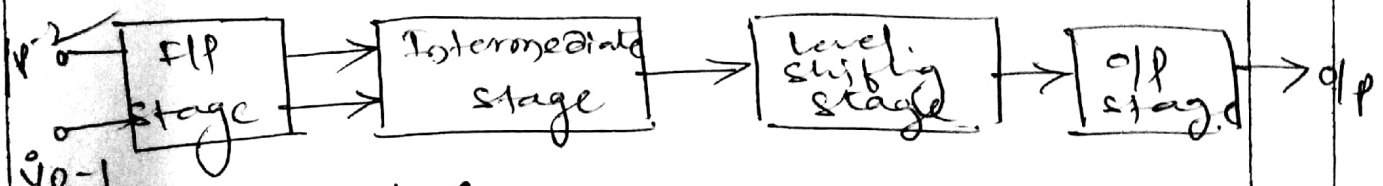
$\therefore R_2 + R_3 = \frac{V_o}{I_2} \Rightarrow R_2 = \frac{3}{50\mu} - R_3 = 59.33K\Omega$ | 5.6KΩ or 68KΩ

$C_1 = \frac{1}{2\pi f(\frac{R_1}{10})} = 0.19\mu F$ | $C_1 = 0.18\mu F$

$C_2 = \frac{1}{2\pi f R_L} = 0.23\mu F$ | $C_2 = 0.22\mu F$

—X—

3 (a) Block Diagram:



I/P stage → It is a Differential Amplifier

Intermediate → multistage amplifier it provides additional voltage gain.

SCHEME OF EVALUATION

Subject : | Sub Code : | Date :

Description	Marks	CO's

we have $V_i = V_s - V_f$ or $V_s = V_i + V_f$

$$A_f = \frac{V_o}{V_s} = \frac{V_o}{V_i + V_f}$$

Dividing N^r & D^r by V_i

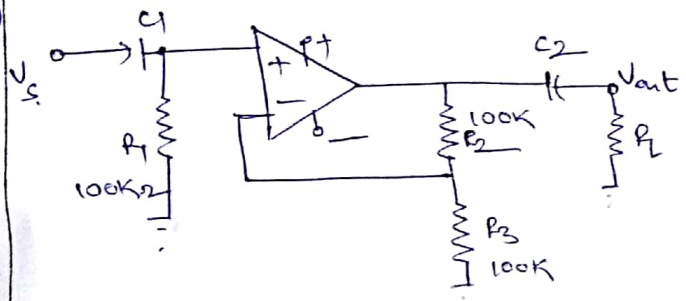
$$A_f = \frac{V_o/V_i}{V_i/V_i + V_f/V_i} = \frac{A}{1 + V_f/V_i} = \frac{A}{1 + \left(\frac{V_f}{V_o} * \frac{V_o}{V_i}\right)}$$

($\frac{V_f}{V_o} = \beta$)

$$\boxed{A_f = \frac{A}{1 + \beta A}}$$

→

(b)



for IC 741
K = 0.909.

$$f_H = \frac{(GB)K}{A_f} = \frac{1MHz.(0.909)}{11} = 82.64\,KHz.$$

$$f_L = \frac{1}{2\pi C_1[R_{if} + R_{in}]} = \frac{1}{2\pi(0.1\mu)\cdot[50 + 0]}$$ (not given)

$$= 31.83\,KHz.$$

Bandwidth $B_W = f_H - f_L$

$= 82.64K - 31.83K$

$$\boxed{= 50.8\,KHz.}$$

→

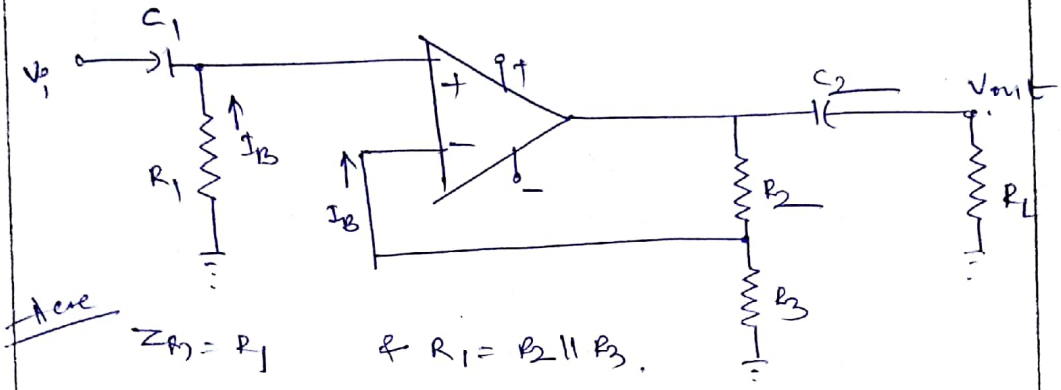
Course Coordinator | Module Coordinator | HOD

SCHEME OF EVALUATION

Sem :	Subject :	Sub Code :	Date :

Q. No.	Bit	Description	Marks	CO's

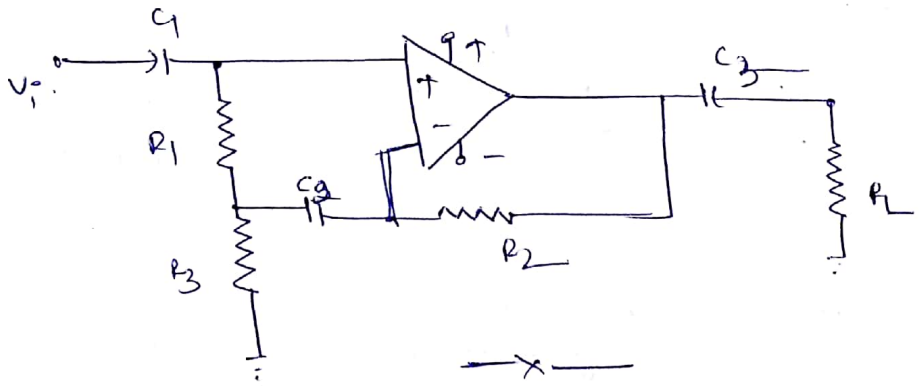
3 (b). Cap- coupled non-inv. amp.



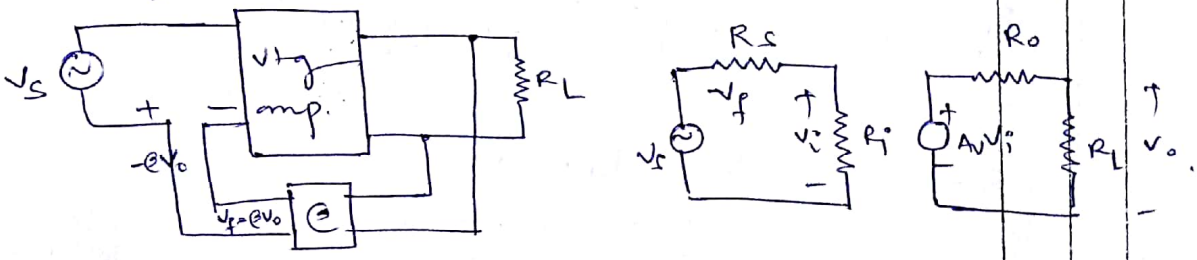
Here $Z_{R_1} = R_1$ & $R_1 = R_2 \| R_3$.

$X_{C_1} = Z_{R_1}/10$ @ f_1. $X_{C_2} = R_L$ @ f_1.

modified ckt.



4 (a) Voltage- series feedback amplifier.



$A = \frac{V_o}{V_i}$ ← Tfr gain without feedback

$A_F = V_o/V_s$ ← Tfr gain with feedback

Course Coordinator | Module Coordinator | HOD

S J P N Trust's

HirasugarInstituteofTechnology, Nidasoshi.

Inculcating Values, Promoting Prosperity

Approved by AICTE, Recognized by Govt. of Karnataka and Affiliated to VTU Belagavi.

E & E Dept.

Exam.

Internal Assessment

Even Sem(2017-18

SECOND INTERNAL ASSESSMENT

Sem: IV | Sub: Operastional Amplifiers & Linear IC's | Sub. Code: 15EE46

Date: 13/04/2018 | Time: 03:00 PM to 04:00 PM | Max. Marks: 25

Note: Answer two full questions, draw sketches wherever necessary.

Q. No		Discription of Question	Marks	CO	RBT Level
1	a	With diagram, explain the adjustable output regulator.	5	214.2	L2
	b	An LM 317 regulator is to provide 6V output from 15V supply. The load current is 200mA. Design the circuit,calculate the power dissipation. Draw the circuit diagram. Select I1=1mA.Vref =1.25V.	5	214.2	L3
	c	Define Line Regulation, Load Regulation and Ripple Rejection.	3	214.2	L1
		OR			
2	a	Explain the working of second order High Pass Filter. Draw its frequency response.	4	214.2	L1,L2
	b	Design a wide band pass filter with FL = 200Hz, FH = 1KHz and pass band gain is equal to 4. Assume capacitor value for high pass section = 0.05μF and for low pass section = 0.01μF. Also calculate the value of Q-factor for the filter and centre frequemcy. Draw the circuit diagram.	4	214.2	L3
	c	Design a Low Pass Filter at a cut off frequency of 15.9KHz with a passband gain of 15.	5	214.2	L3
3	a	Explain the working of Schmitt trigger in inverting mode. Draw its hysteresis curve.	6	214.3	L2
	b	Design a non-inverting Schmitt trigger circuit to have UTP = +3V and LTP = -5V. Use 741 op-amp with VCC = ±15V.	6	214.3	L3
		OR			
4	a	Explain the oscillator amplitude stabilization with necessary figures.	4	214.3	L2
	b	Explain the working of voltage to current converter with grounded load.	4	214.3	L2
	c	Design a RC phase shift oscillator using op-amp. Assume C = 0.1 μF, frequency of oscillation = 200Hz. Draw the circuit.	4	214.3	L3

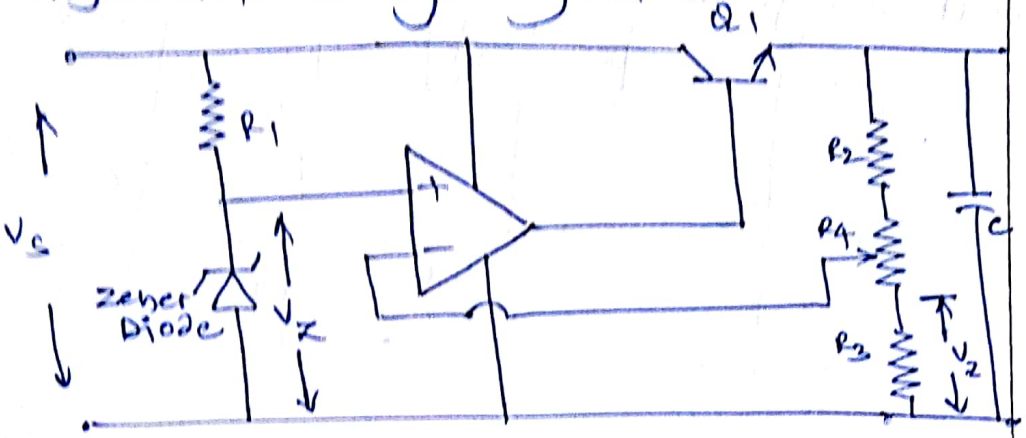
H. O. D.
Electrical & Electronics Engg
Hirasugar Institute of Technology
NIDASOSHI-591236.

SCHEME OF EVALUATION

Sem : 4 | Subject : OALI | Sub Code : 15EE46 | Date : 11.04.2018

Q. No.	sub	Description	Marks	CO's

1 (a) Adjustable Voltage Regulator.



→ Here o/p vtg can be greater than or less than the zener voltage V_z.

→ V_{R3} ← vtg across R_3 when o/p vtg falls below V_z, the op-amp o/p moves in the direction till $V_{R3} = V_z$.

→ $V_o = V_z \left(\frac{R_2 + R_3}{R_3}\right)$.

—×—

(b) Given $I_f = 1mA$ &1P.

$\therefore R_1 = \frac{V_{ref}}{I_f} = \frac{1.25}{1m} = 1.2K\Omega$ **1.2KΩ**

&1P

With $R_2 = \frac{V_o - V_{ref}}{I_f} = \frac{6 - 1.25}{1m} = 4750\Omega$ **4.7KΩ**

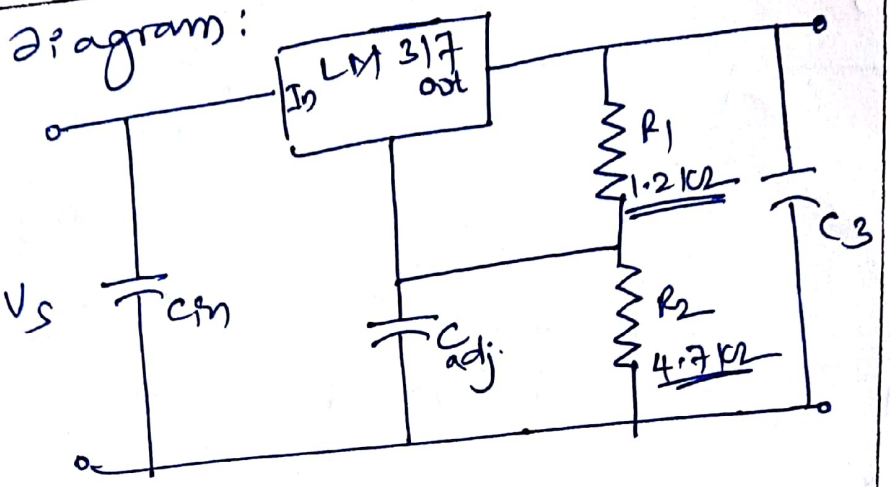
Power Dissipation.

$P_D = (V_o - V_c) I_L$

$= (15 - 6) \cdot 200m = 1.8$ watts

Course Coordinator | Module Coordinator | HOD

circuit diagram:

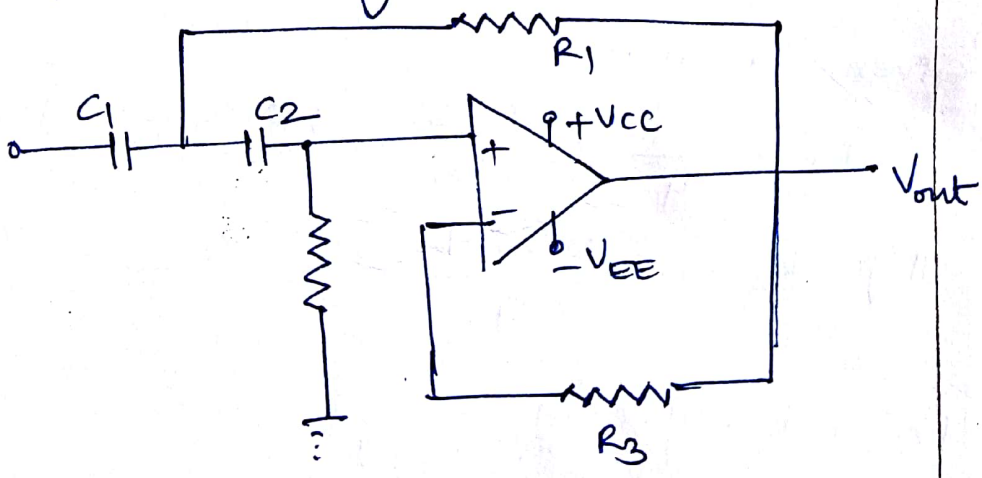


(c) Line Regulation → $\frac{(\Delta V_o \text{ for a } 10\% \text{ change in } V_s)}{V_o} * 10$

Load Regulation → $\frac{(\Delta V_o \text{ for } \Delta I_{L(max)})}{V_o} * 100.$

Ripple Rejection → $20 \log\left(\frac{V_{rs}}{V_{oo}}\right)$.

2 (a) Second order High Pass filter



SCHEME OF EVALUATION

Subject : OALI | Sub Code : | Date : 11.04.2018

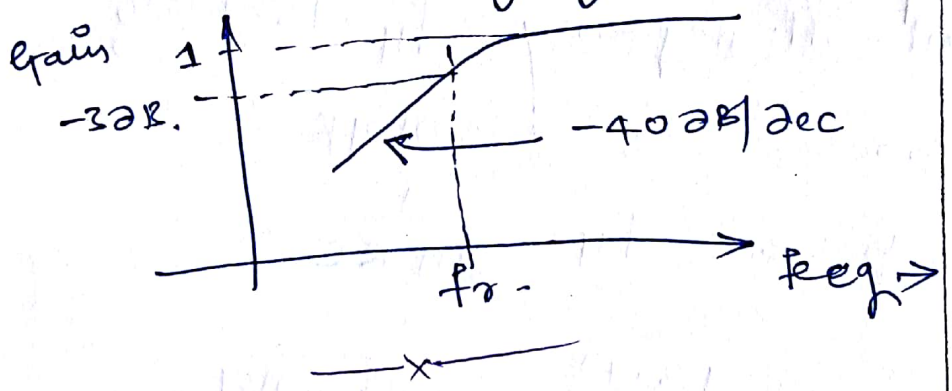
Description	Marks	CO's

→ @ lower frequency C_2 & R_1 causes a fall off rate of −20 dB/dec

→ another −20 dB/dec is introduced by C_1 & R_2.

→ @ higher frequencies X_{C_1} & X_{C_2} are much smaller than R_1 & R_2 hence they have no effect on the circuit.

i.e Ag gain is equal to 1.



—x—

(b) We have $X_{C_2} = R_2$ at f_2

$\therefore C_2 = \frac{1}{2\pi f_2 R_2}$ $\quad \therefore R_2 = \frac{1}{2\pi (1K\Omega)\, 0.05\mu} = 3182\,\Omega$ ≈ 3.3 KΩ

For $A_V = 4$ $\quad \therefore R_1 = \frac{R_2}{4} = 825\,\Omega$ ≈ 820 Ω

For Q-factor we have, $Q = f_0/BW$

$\therefore f_0 = \sqrt{f_1 f_2} = \sqrt{200 * 1000} = 447.2\,Hz$

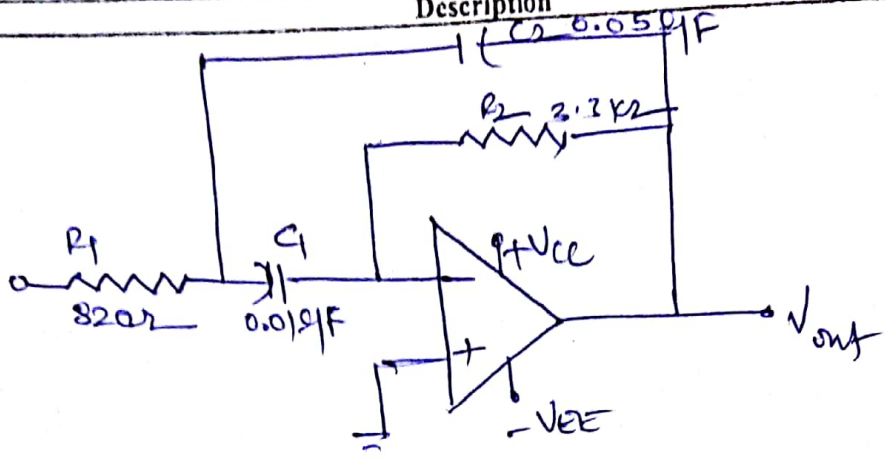
$BW = f_2 - f_1 = 1000 - 200 = 800\,Hz$

$\therefore Q = \frac{447.2}{800} = 0.559 \simeq 0.6$

SCHEME OF EVALUATION

Sem :	Subject :	Sub Code :	Date :

Q. No.	Bit	Description	Marks	CO



(c) Given,

cut-off frequency $f_H = 15.9\ KHz$.

choose $C = 0.001\mu F$

we have $f_H = \frac{1}{2\pi RC}$

$\therefore 15.9K = \frac{1}{2\pi R \cdot 0.01\mu}$

$\therefore \boxed{R = 10K\Omega}$ Ans.

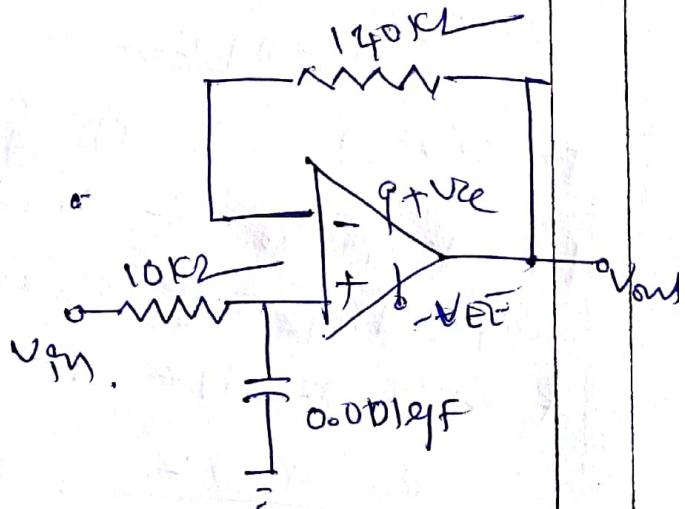
Given $A_f = 15$

$\therefore A_f = 1 + \frac{R_F}{R_1}$

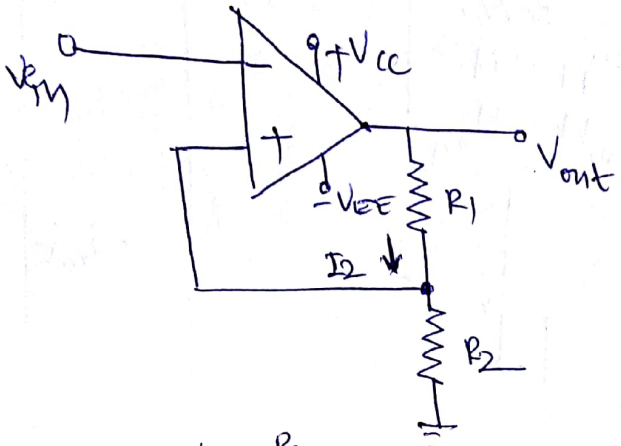
$\therefore \frac{R_F}{R_1} = 14$

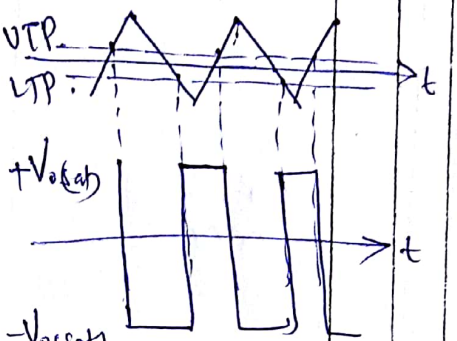
$\therefore R_F = 14 \cdot R_1$

$\therefore \boxed{R_F = 140K\Omega}$

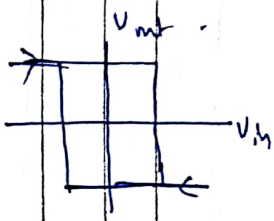


(a) Schmitt Trigger in inverting mode.





$$UTP = +V_o \frac{R_2}{R_1+R_2} \qquad LTP = -V_o \cdot \frac{R_2}{R_1+R_2}$$



—×—

(b) Non-Inv. Schmitt circuit

$$UTP + LTP = \frac{2R_1}{R_1+R_2} * V_{ref}$$

$$UTP - LTP = \frac{2R_1}{R_1+R_2} * V_{sat}.$$

$V_{sat} = 90\%$ of V_{cc}

i.e. $= 0.9 *$

$= $

$\therefore V_{ref} = 0.$

$$UTP = \frac{R_2}{R_1+R_2} * V_{sat} \qquad LTP = \frac{R_2}{R_1+R_2} * -V_{sat}.$$

$$\therefore UTP - LTP = \frac{R_2}{R_1+R_2} \cdot 2V_{sat} = \underset{UTP}{3} - \underset{LTP}{(-5)} = 8V$$

$V_{sat} = 14V$

~~Assume R_2~~ $\therefore \frac{R_2}{R_1+R_2} \cdot 2(14) = 8$

$$\frac{R_2}{R_1+R_2} = 0.285$$

$0.285R_1 + 0.285R_2 = R_2$

$0.285R_1 = 0.715R_2$

$\therefore R_1 = 2.5R_2$

Assume $R_2 = 1k\Omega$ $\therefore R_1 = 2.5k\Omega$

std $3.3k\Omega$

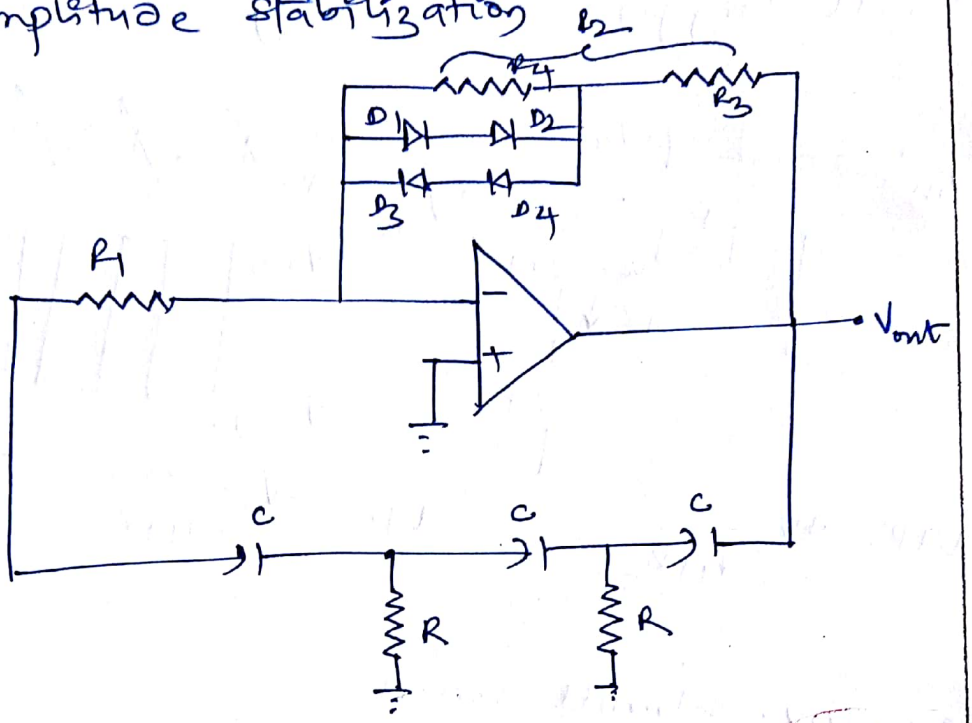
—×—

Course Coordinator | Module Coordinator | HOD

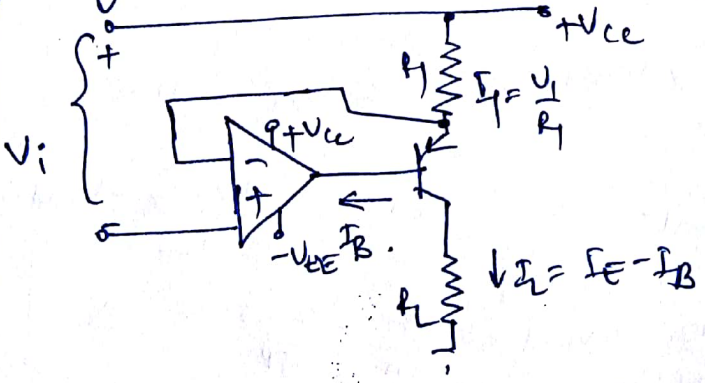
SCHEME OF EVALUATION

Sem : | Subject : | Sub Code : | Date :

Q. No.	Bit	Description	Marks	CO's
4	(a)	Amplitude stabilization		



(b) V-f to f-V converter with grounded load.

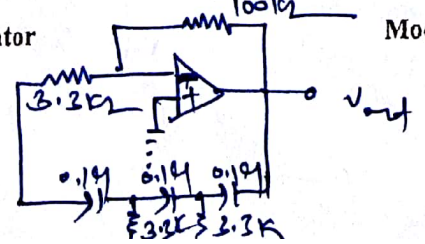


(c) $C = 0.1\mu F$ $f_o = 200Hz$.

we have $f = \frac{1}{2\pi RC\sqrt{6}}$

$\therefore R = \frac{1}{2\pi(0.1\mu)(200)\cdot\sqrt{6}} = 3248\Omega$

$3.3K\Omega$



as we know,

$A_{vf} > 29$

$\therefore \frac{R_f}{R_1} > 29$

$\therefore R_f = 29 \cdot R_1$

$R_f = 100K\Omega$

Course Coordinator | Module Coordinator | HOD

	S J P N Trust's **HirasugarInstituteofTechnology, Nidasoshi.** *Inculcating Values, Promoting Prosperity* Approved by AICTE, Recognized by Govt. of Karnataka and Affiliated to VTU Belagavi.	E & E Dept. Exam. Internal Assessment Even Sem(2017-18)

THIRD INTERNAL ASSESSMENT

Sem: IV | Sub: **Operastional Amplifier & IC's** | Sub. Code: 15EE46

Date: 07/03/2018 | Time: 03:00 PM to 04:00 PM | Max. Marks: 25

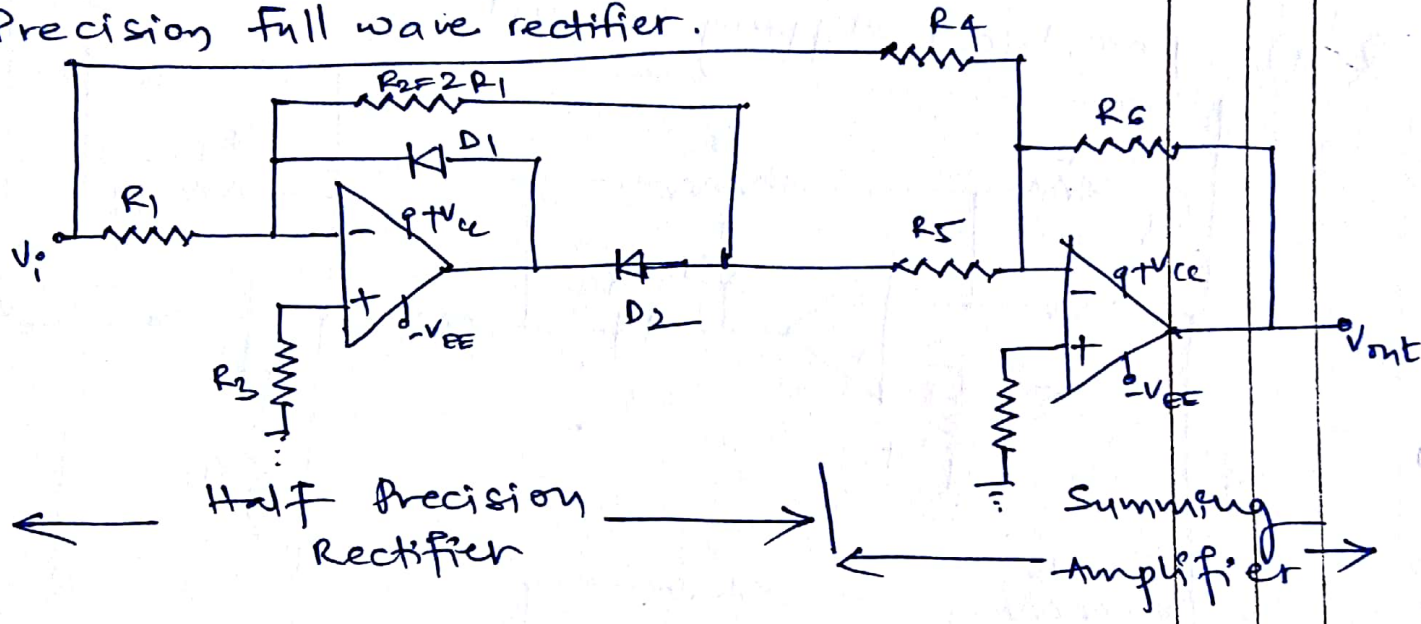
Note: Answer two full questions, draw sketches wherever necessary.

Q. No		Discription of Question	Marks	CO	RBT Level
1	a	Explain the precision full wave rectifier circuit as a combination of half wave rectifier and summing circuit.	6	214.4	L2
	b	With diagram explain the working of op-amp sample and hold circuit.	4	214.4	L3
	c	Draw and briefly explain working of dual slope ADC.	3	214.4	L1
		OR			
2	a	Draw the circuit diagram for symmetrical clipping circuit consisting of two dead zone circuit and a summing circuit. (draw only)	3	214.4	L2
	b	Draw and explain the circuit of peak detector. Draw the waveforms.	5	214.4	L3
	c	With neat circuit explain three bit R-2R DAC.	5	214.4	L2
3	a	With block diagram, explain Phase Locked Loop in detail.	5	214.5	L2
	b	Explain PLL IC 565 application as frequency multiplier.	4	214.5	L3
	c	Explain the function ofvarious pins of IC 555 timer.	3	214.5	L2
		OR			
4	a	A monostable mulivibrator circuit uses a 5V supply. Determine suitable component values to produce a 700µsec output pulse when the circuit is triggered.	6	214.5	L3
	b	An astable multivibrator is to be designed for getting rectangular waveform for tON = 0.6ms. Total time period = 1ms. Assume C = 0.1µF draw the circuit diagram.	6	214.5	L3

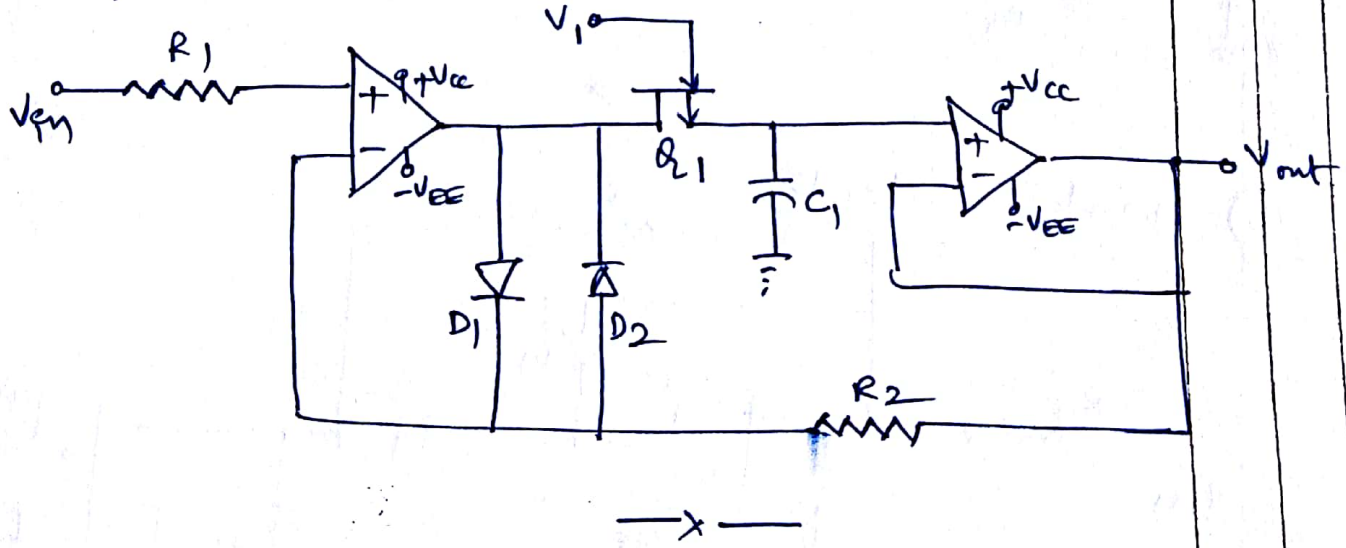
SCHEME OF EVALUATION

Sem : IV | Subject : DALI | Sub Code : 15EE46 | Date : 17.05.2018

Q. No.	Bit	Description	Marks	CO's
I	ⓐ	Precision full wave rectifier.	4	



ⓑ Sample & Hold circuit.



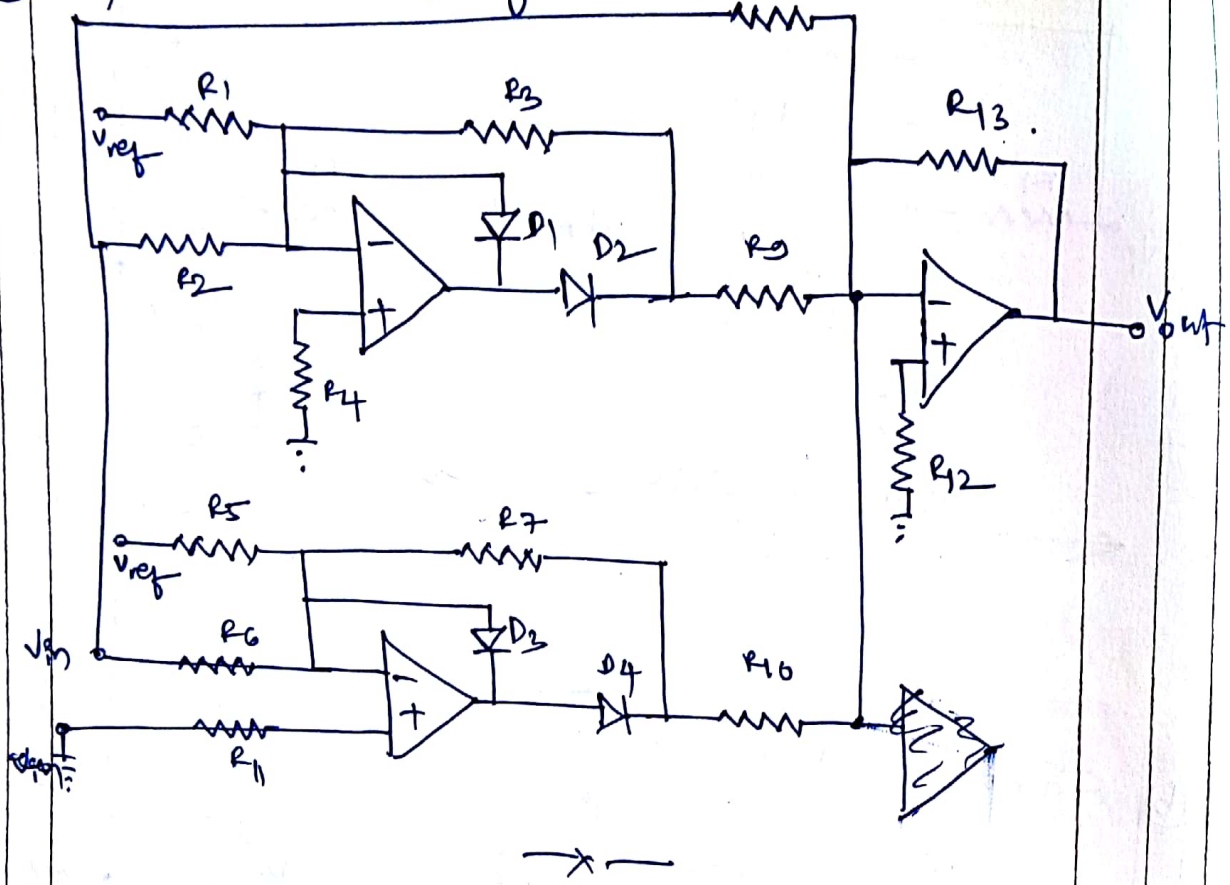
ⓒ Dual Slope ADC.

SCHEME OF EVALUATION

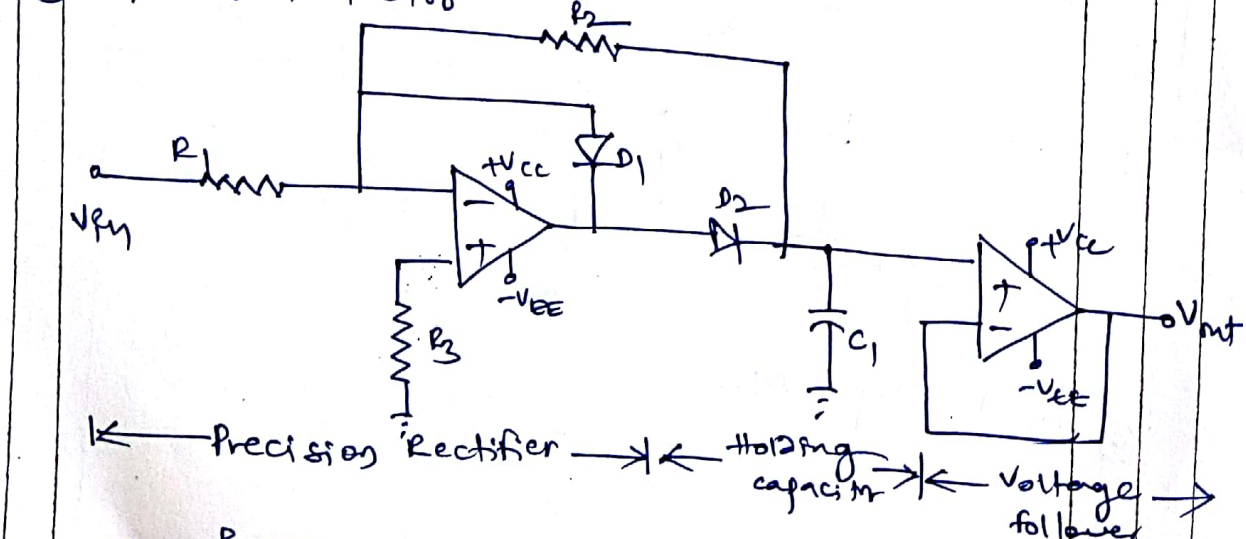
Sem :	Subject :	Sub Code :	Date :

Q. No.	Blt	Description	Marks	CO's

2 (a) Symmetrical clipping circuit.



(b) Peak Detector



← Precision Rectifier → ← Holding capacitor → ← Voltage follower →

wave form :

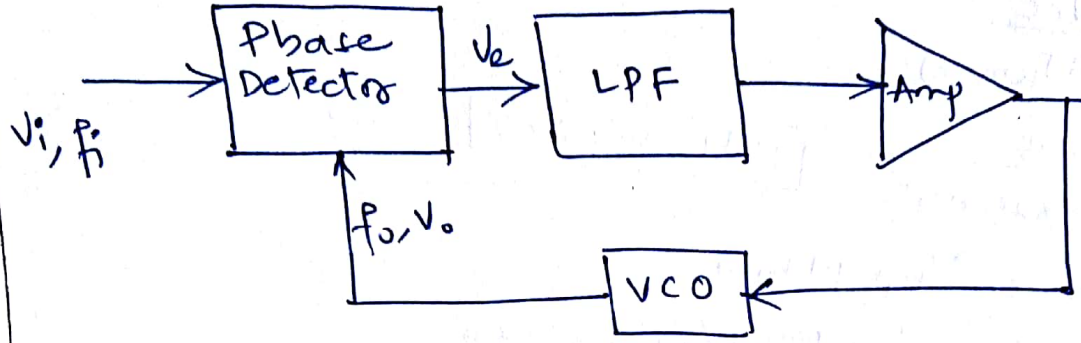
Course Coordinator | Module Coordinator | HOD

SCHEME OF EVALUATION

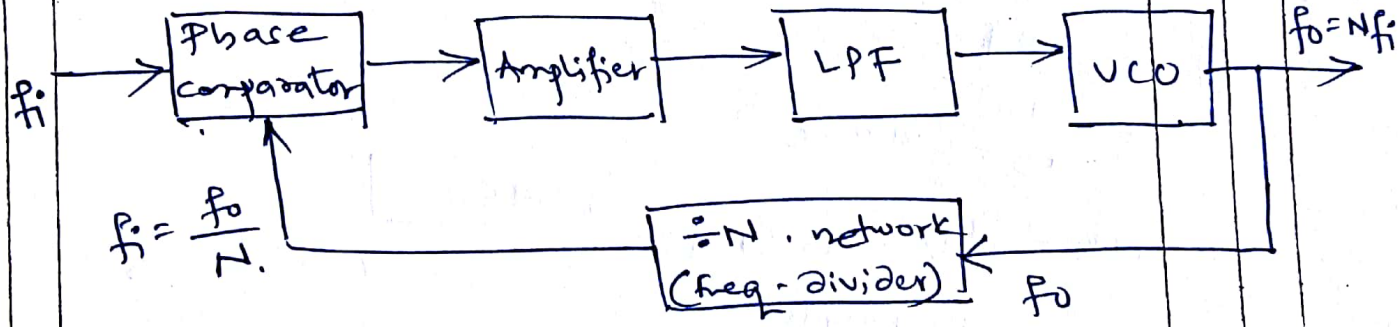
Sem : Subject : Sub Code : Date :

Q. No.	Bit	Description	Marks	CO's

3 (a) Phase Locked Loop —



(b) Frequency multiplier using PLL.



(c) Pin Diagram of IC-555.