9945109480, Sagar.S.Pujarade AP.EEE

Third Semester B.E Degree Examination, June/July-2015.

ANALOG ELECTRONIC CIRCUITS

PART-A

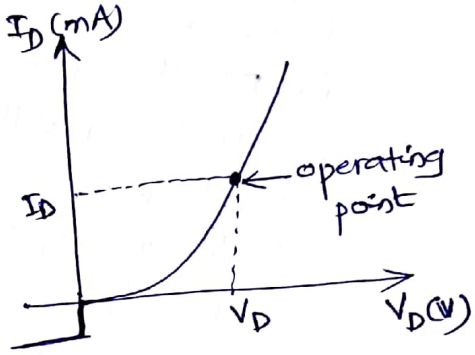
1.g) State and explain the various resistance levels of the semiconductor diode. [06 Marks]

→ Three resistance levels of the diode are,
(i) DC or static Resistance
(ii) AC or Dynamic Resistance
(iii) Average ac Resistance

(i) DC or Static Resistance:

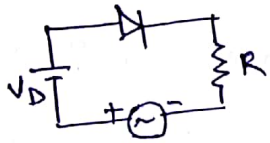
For a circuit containing diode if dc voltage is applied, dc cln flows. The opposition offered by the circuit to the flow of dc current is called DC or static Resistance

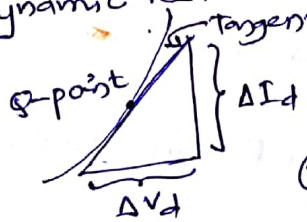
$$R_D = \frac{V_D}{I_D}$$



(ii) AC or Dynamic Resistance:

The resistance of the diode to the flow of ac current is called the ac or dynamic resistance.



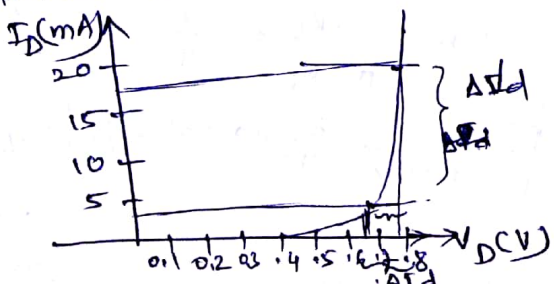


$$r_d = \frac{\Delta V_d}{\Delta I_d}$$

@ here:
ΔV_d ← change in ac diode vtg.
ΔI_d ← corresponding change in ac diode cln.

(iii) Average AC Resistance:

The AC or Dynamic resistance is measured under small signal operation. If AC input signal is large it produces a broad swing about Q-point. The resistance associated with the device under large signal opn is called the average ac res.

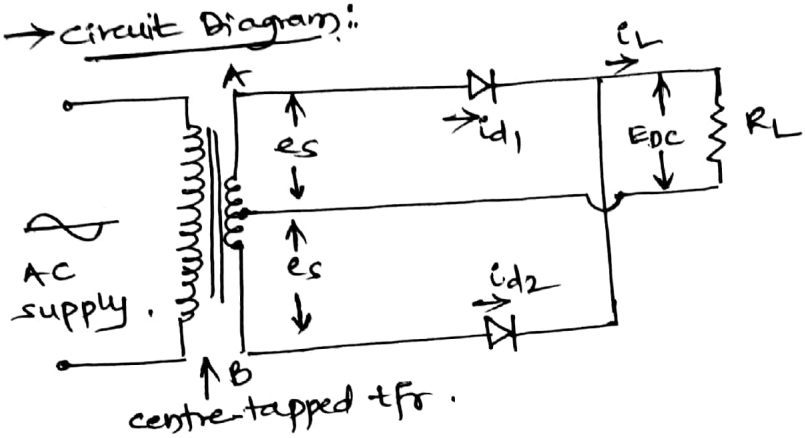


$$r_{avg} = \frac{\Delta V_d}{\Delta I_d}$$ point to point

c)

b) Expain the working of a full wave centre tapped rectifier. Also determine Ripple factor, efficiency and voltage regulation. (10 Marks)

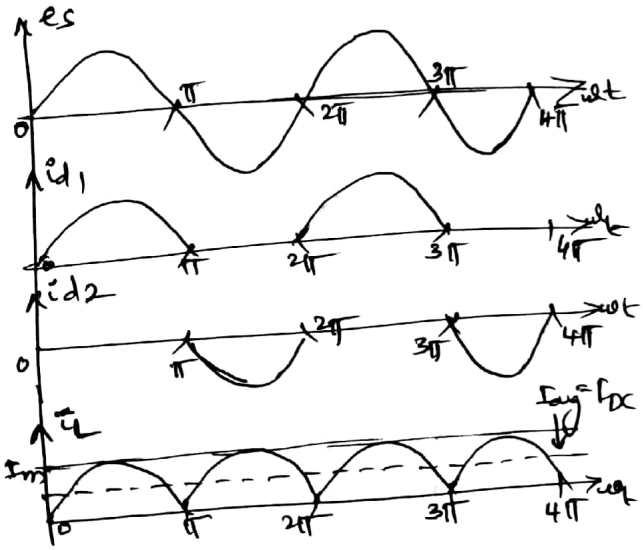
→ Circuit Diagram:



* The FWR conducts during both +ve & -ve half cycles of AC input.
* Two diodes are used here, both feed a common load R_L.

Working:

* During +ve half cycle: terminal A is positive & terminal B is -ve. ie diode D_1 will be froward biased & hence will conduct
* Diode D_1 supplies the load c/t ie $i_L = i_{d1}$;
* During -ve half cycle the polarity reverses ie B is +ve & A is -ve. The diode D_2 conducts which D_1 is reverse biased.
* now, D_2 supplies load c/t
  ∴ $i_L = i_{d2}$
* It should be noted that during both cases c/t flows in same d/r.



* Ripple Factor:

$$R.F = \sqrt{\left[\frac{I_{RMS}}{I_{DC}}\right]^2 - 1}$$

For FWR $I_{RMS} = \frac{I_m}{\sqrt{2}}$

$I_{DC} = \frac{2I_m}{\pi}$

$$\therefore RF = \sqrt{\left[\frac{I_m/\sqrt{2}}{2I_m/\pi}\right]^2 - 1} = \sqrt{\frac{I_m^2/2}{4I_m^2/\pi} - 1} = \sqrt{\frac{\pi^2}{8} - 1}$$

$$= 0.48$$

* Efficiency:

$$\eta = \frac{P_{DC\ output}}{P_{AC\ input}} = \frac{\frac{4}{\pi^2} I_m^2 R_L}{\frac{I_m^2 (R_f + R_s + R_L)}{2}}$$

But if $R_f + R_s \ll R_L$

$$\therefore \eta = \frac{8R_L}{\pi^2 R_L} = \frac{8}{\pi^2}$$

$$\therefore \eta_{max} = \frac{8}{\pi^2} \times 100 = 81.2\%$$

* Voltage Regulation:

for FWR:

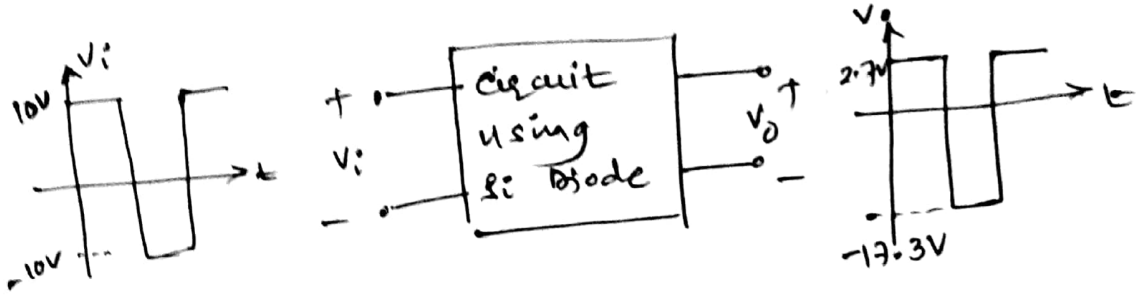
$(V_{dc})_{NL} = \frac{2E_m}{\pi}$

$(V_{dc})_{FL} = I_{DC} R_L$

$$\%Reg = \frac{(V_{dc})_{NL} - (V_{dc})_{FL}}{(V_{dc})_{FL}} \times 100$$

$$\%R = \frac{R_f}{R_L} \times 100$$

c) Design a suitable circuit represented by the box shown below, which has the input and output waveforms as indicated. (04 Marks)



→ Solution:

Given $V_m = 10V$ as diode is made of Si

$V_K = 0.7V$

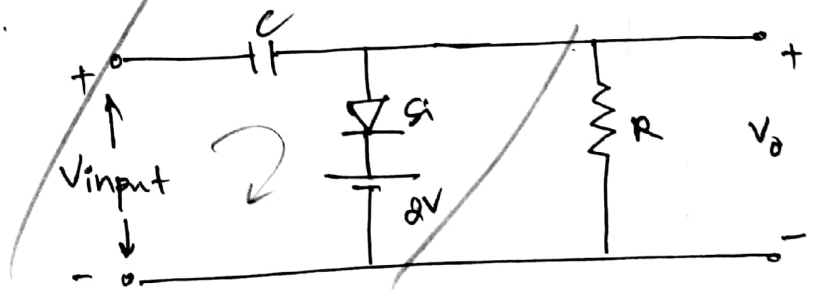
We have $V_o = -2V_m + V_K$

$= -2 * 10 + 0.7$

$= -20 + 0.7 = \underline{-19.3V}$

$\therefore \quad -19.3 + V_R = -17.3$

$\therefore \quad V_R = \underline{2V}$



(a) we have for -ve clamper ckt

$V_o = V_{in} - V_K$

$V_o = -2 + 0.7 - V_{in}$

$= -10 + 2.7$

$V_o = -7.3$

Hence

for $V_{in} = +10V$

$V_o = V_{in} - V_o$

$= 10 - 7.3$

$= 2.7V$

for $V_{in} = -10V$

$V_o = V_{in} - V_o$

$= -10 - 7.3$

$= -17.3V$

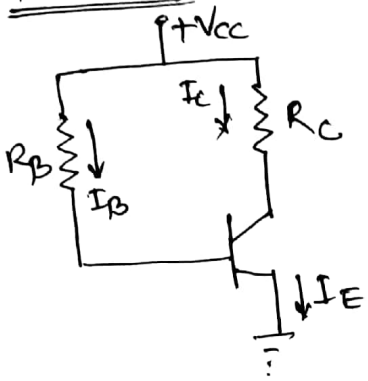
—x—

2) Name different biasing methods of transistor. With circuit diagram analyze the fixed bias circuit, with effect of variation in I_B, R_C and V_{CC} on Q-pt of load. (10 Marks)

→ Different biasing methods:

(i) Fixed Bias (ii) Emitter Bias
(iii) Voltage Divider Bias (iv) collector feedback Bias.

FIXED BIAS:



Applying KVL to base circuit,

$$V_{CC} - I_B R_B - V_{BE} = 0 \quad \text{---(1)}$$

$$\therefore I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

or $$I_B \simeq \frac{V_{CC}}{R_B}$$

WKT, $I_C = \beta I_B$

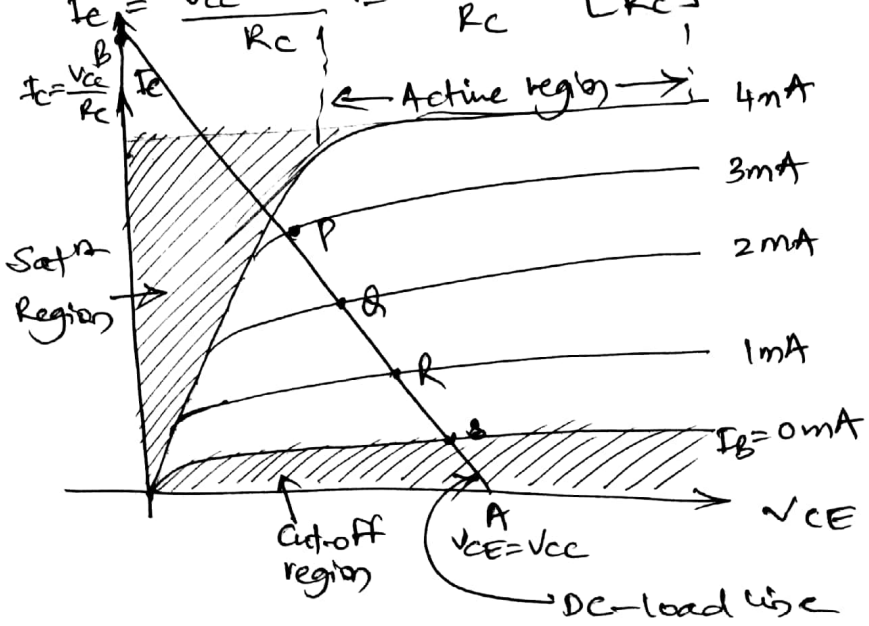
$$\therefore V_{CC} = V_{CE} + I_C R_C \qquad \therefore I_C = \frac{V_{CC} - V_{CE}}{R_C}$$

& $$I_{C(sat)} = \frac{V_{CC}}{R_C}.$$

Load line analysis:

For fixed bias circuit we have,

$$I_C = \frac{V_{CC} - V_{CE}}{R_C} = \frac{V_{CC}}{R_C} - \left[\frac{1}{R_C}\right] V_{CE} = -\left[\frac{1}{R_C}\right] V_{CE} + \frac{V_{CC}}{R_C}$$



Comparing the eqn of I_C with straight line eqn
ie $y = mx + c$ where $m \leftarrow$ slope & $c \leftarrow$ pt of intercept on Y axis.

Then draw a line on the graph of I_C V/s V_{CE} which is having slope $-1/R_C$ & Y-intercept @ $\frac{V_{CC}}{R_C}$.

To determine these points assume,

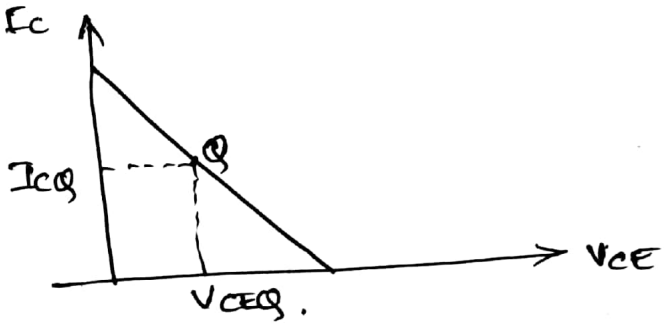
$V_{CE} = V_{CC}$ & $V_{CE} = 0$.

$\therefore$ when $V_{CE} = V_{CC}$; $I_C = 0$ $\leftarrow$ we get point A.

$V_{CE} = 0$; $I_C = \frac{V_{CC}}{R_C}$ $\leftarrow$ we get point B.

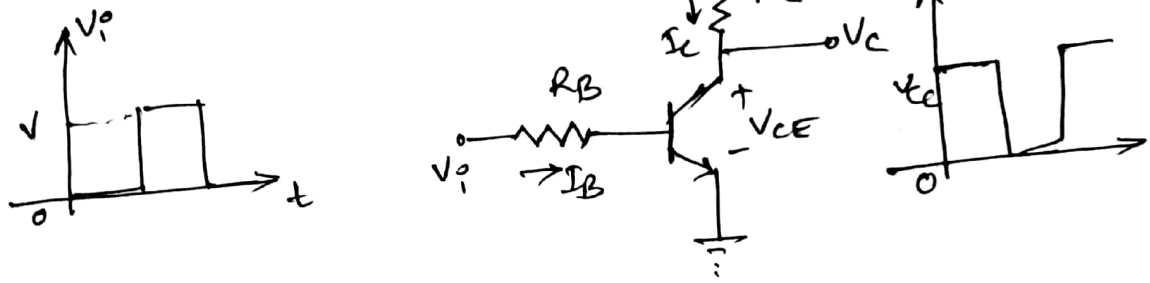
In load line fig:

The line AB — is called DC LOAD LINE.
(only dc condns are considered)



b) Explain the circuit of a transistor switch being used as an inverter. (04 Marks)

→ When biased in the middle of active region, transistor works as a faithfull amplifier. When operated between cut-off and saturation, transistor works as a switch or an inverter.



KVL to Base-Emitter circuit,

$$V_i = I_B R_B + V_{BE}$$

$$\therefore I_B = \frac{V_i - V_{BE}}{R_B}$$

KVL to collector-emitter circuit,

$$\therefore I_C = \frac{V_{CC} - V_{CE}}{R_C}$$

@ saturation — $V_{CE} = V_{CE(sat)}$
$V_i = V$ $I_C = I_{C(sat)}$

$$R_{C(sat)} = \frac{V_{CE(sat)}}{I_{C(sat)}}$$

But $V_{CE(sat)} = 0$ & $I_{C(sat)} = 0$ $\therefore R_{C(sat)} = 0\,\Omega$

@ cut-off — $R_{cut\text{-}off} = \frac{V_{CE}}{I_{CE}}$
$V_i = 0V$

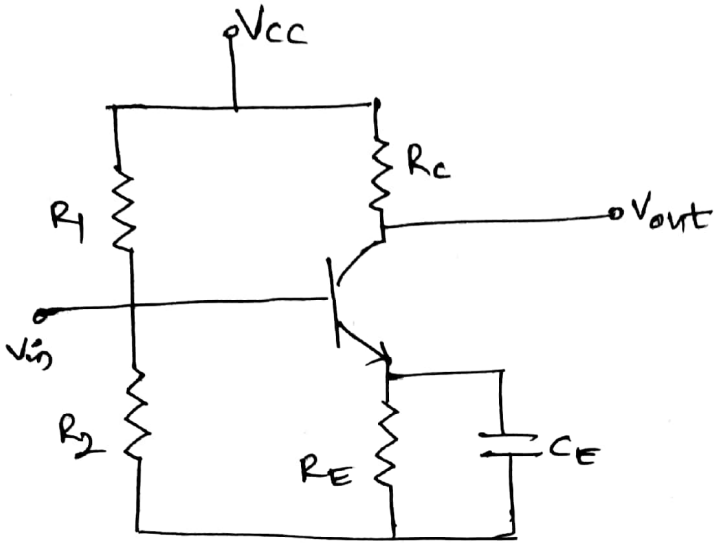
$V_{CE} = V_{CE(cut\text{-}off)} = V_{CC}$

& $I_{CE} = 0$

$\therefore R_{cut\text{-}off} = \infty\,\Omega$ [open ckt between C & E when operated in cut-off].

5) c) In a voltage divider bias circuit of BJT. $V_{CC} = 20V$, $R_C = 10K\Omega$, $R_E = 1.5K\Omega$, $R_1 = 40K\Omega$, $R_2 = 4K\Omega$. Assume silicon transistor with $\beta = 150$. Find I_C, V_{CE} and $I_{C(sat)}$ using exact analysis. (06 Marks)

→ Solution



Given:

$V_{CC} = 20V$, $R_C = 10K\Omega$

$R_E = 1.5K\Omega$, $R_1 = 40K$

$R_2 = 4K\Omega$, $\beta = 150$.

$R_{Th} = R_1 \parallel R_2$

$= \frac{40K\Omega * 4K\Omega}{40K\Omega + 4K\Omega} = 3.63K\Omega$

We know that, $V_{Th} = V_{CC} \cdot \frac{R_2}{R_1 + R_2}$

$= 20 \cdot \frac{4}{40K+4K} = 1.82V$

$I_B = \frac{V_{Th} - V_{BE}}{R_{Th} + (1+\beta)R_E} = 4.869\mu A$

We have, $I_E = \beta I_B = 0.729\,mA$

$V_{CE} = V_{CC} - I_C(R_C + R_E)$

$= 20 - 0.729(10K + 1.5K) = 11.62V$

and $I_{C(sat)} = \frac{V_{CC}}{R_C + R_E} = 1.74\,mA$

—x—

3

a) Define h-parameters & hence derive h-parameters model of CE-BJT. [06]

→ **h-parameters:**

The r_e model for a transistor is sensitive to the dc level of operation of the amplifier. the input resistance will vary with dc operating pt

The defining equations for h-parameters are:

$$V_i = f_1(I_i, V_o) \qquad I_o = f_2(I_i, V_o)$$

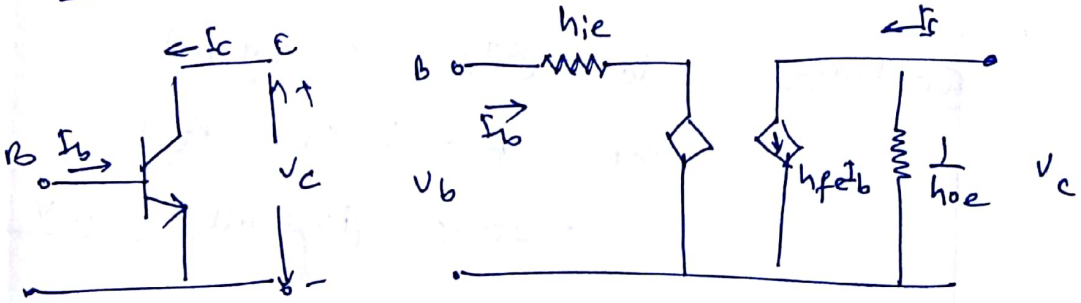
$$= h_{11} I_i + h_{12} V_o, \qquad = h_{21} I_i + h_{22} V_o$$

$$V_i = h_i I_i + h_r V_o \qquad = h_f I_i + h_o V_o$$

$$h_{11} = h_i = \left.\frac{V_i}{I_i}\right|_{V_o=0} \qquad h_{12} = h_r = \left.\frac{V_i}{V_o}\right|_{I_i=0}$$

$$h_{21} = h_f = \left.\frac{I_o}{I_i}\right|_{V_o=0} \qquad h_{22} = h_o = \left.\frac{I_o}{V_o}\right|_{I_i=0}.$$

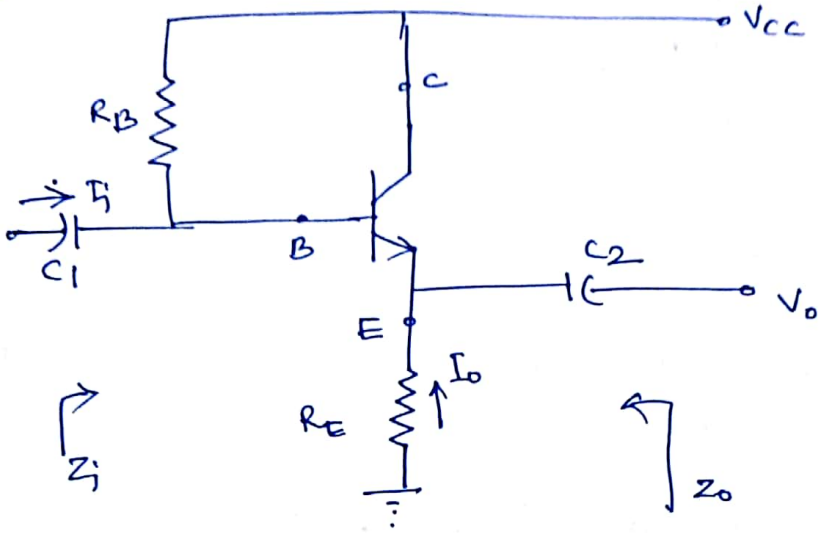
CE - BJT



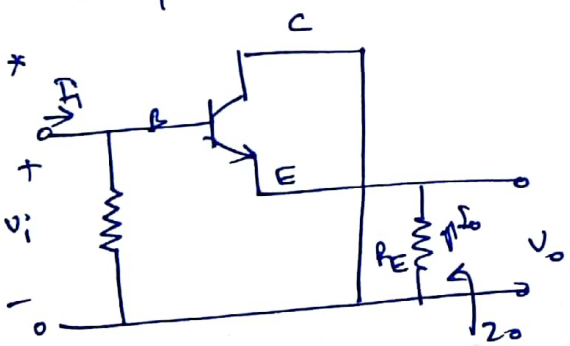
—x—

3 (b) Explain with a neat circuit diagram of emitter follower configuration. Justify how voltage gain is nearly equal to one. [06]

→



* i/p signal is applied to base through coupling capacitor C_1.
* o/p is taken from emitter.



$V_i = V_{be} + V_o$

neglecting V_{be}

$V_i = V_o$ ——— (1)

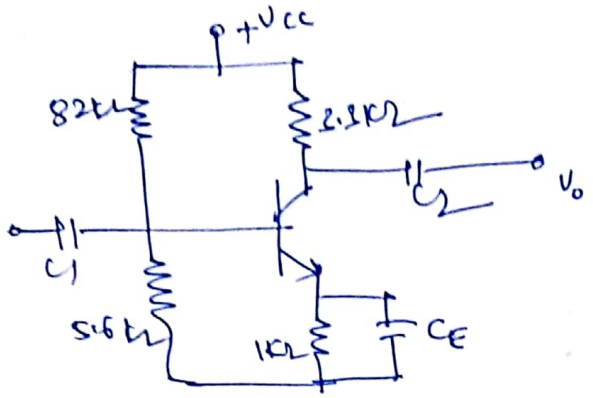
i.e o/p voltage follows i/p voltage

from eq 2 (i) $A_V = \frac{V_o}{V_i} \simeq 1$.

hence the proof

—x—

3 (c). For the circuit shown below. Determine V_{CC}, if $A_V = -160$ and $r_o = 100\text{k}\Omega$. Take $\beta = 100$.



$$\rightarrow \quad A_V = \frac{-r_o \parallel R_L}{r_e}$$

$$-160 = \frac{-100\text{k}\Omega \parallel 3.3\text{k}\Omega}{r_e} \qquad \Rightarrow \boxed{r_e = 19.96\Omega}$$

$$r_e = \frac{26\text{mV}}{I_e} \Rightarrow I_E = \frac{26\text{mV}}{19.96} = 1.3\text{mA}$$

$$V_{th} = V_{BE} + I_E R_E = 0.7 + (1.3\text{mA})(1\text{k}\Omega) = 2\text{V}$$

$$V_{th} = \frac{V_{CC} R_2}{R_1 + R_2}$$

$$V_{CC} = \frac{V_{th}(R_1 + R_2)}{R_2}$$

$$= \frac{(2\text{V})\,[\,82\text{k}\Omega + 5.6\text{k}\Omega\,]}{5.6\text{k}\Omega} = 31.2\text{V}.$$

4.

a) Draw the single stage RC coupled BJT amplifier and discuss the effect of [low freq response]:

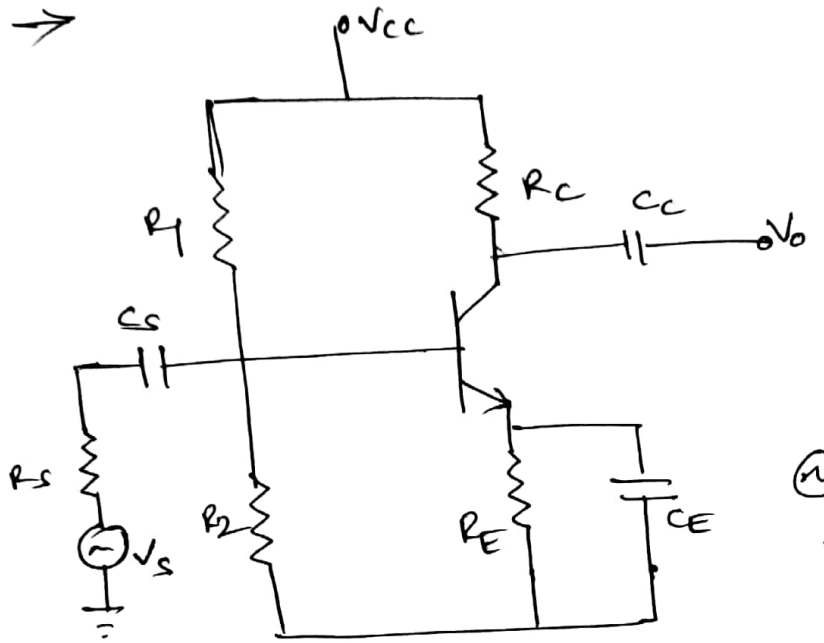
(i) Input capacitance C_s

(ii) Output capacitance C_c and

(iii) Emitter by pass capacitance C_E on freq response.

[05 Marks]

→



$$X_{Cs} = \frac{1}{2\pi f C_s}$$

$$V_o = V_s \cdot \frac{R_i'}{R - jX_C}$$

We have

Voltage Gain $= A_V = \frac{V_o}{V_i}$

$$= \frac{R_i'}{R - jX_C} = \frac{1}{1 - j\left[\frac{X_C}{R}\right]}$$

Here $R_i = R_1 \| R_2 \| h_{ie}$

$$\therefore V_o = V_c \cdot \frac{R_L}{R_o + R_L - jX_{CC}}$$

Where $R_o = r_o \| R_e$

$$f_{L_S} = \frac{1}{2\pi [R_s + R_i'] C_s}$$

$$f_{L_C} = \frac{1}{2\pi [R_o + R_L] C_C}$$

$$\text{and } f_{L_E} = \frac{1}{2\pi R_C C_E}$$

b) Prove that miller effect of input capacitance and output capacitance

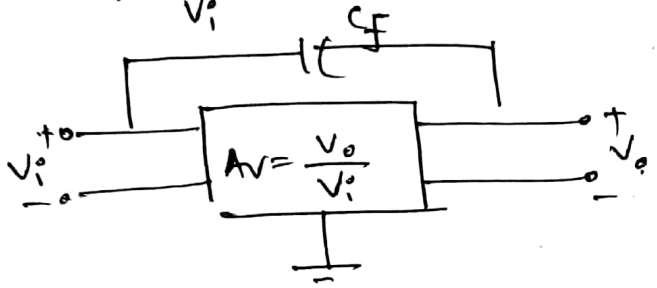
$C_{Mi} = (1 - A_V) C_f$

$C_{Mo} = \left(1 - \frac{1}{A_V}\right) C_f$.

(10 Marks)

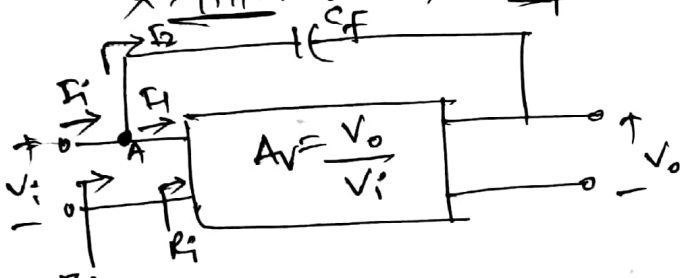
→ The miller effect accounts for the increase in the equivalent input capacitance of an inverting voltage amplifier due to amplification of the effect of capacitance between the input and output terminals.

Consider a inverting amplifier with gain $A_V = \frac{V_o}{V_i}$ and a capacitance 'C_f' between i/p & o/p.



As it is inverting amp V_i & V_o are 180° out of phase so 'A_V' is -ve.

* Miller ~~effect~~ Input capacitance: C_{Mi}.



Here: Let

$R_i = \frac{V_i}{I_1}$ or $I_1 = \frac{V_i}{R_i}$

and $Z_i = \frac{V_i}{I_i}$ or $I_i = \frac{V_i}{Z_i}$

KCL @ node 'A' $\quad I_i = I_1 + I_2$ ——— (1)

$\therefore \quad I_2 = \frac{V_i - V_o}{X_{Cf}}$

$= \frac{V_i - V_i A_V}{X_{Cf}}$ because @KT: $V_o = V_i A_V$.

$I_2 = \frac{V_i [1 - A_V]}{X_{Cf}}$

Put I_i, I_1 and I_2 in eqn (1),

$\frac{V_i}{Z_i} = \frac{V_i}{R_i} + \frac{V_i [1 - A_V]}{X_{Cf}}$

i.e. $\frac{1}{Z_i} = \frac{1}{R_i} + \frac{(1-A_V)}{X_{Cf}}$

It can be written as,

$$\frac{1}{Z_i} = \frac{1}{R_i} + \frac{1}{\left(\frac{1-A_V}{X_{Cf}}\right)} \Rightarrow \frac{1}{Z_i} = \frac{1}{R_i} + \frac{1}{X_{CMi}}$$

Where $X_{CMi} = \frac{X_{Cf}}{1-A_V}$ ——— (2)

& $X_{Cf} = \frac{1}{2\pi f C_f}$

$$X_{CMi} = \frac{1}{2\pi f [1-A_V] C_f}$$

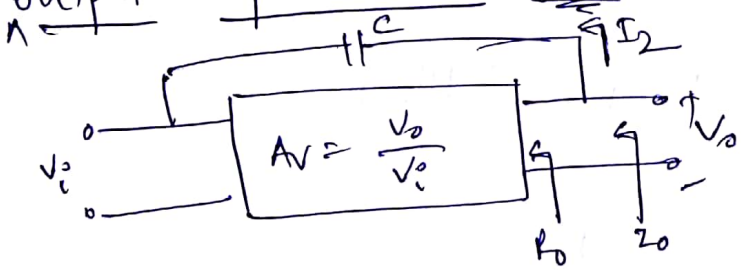
$$X_{Mi} = \frac{1}{2\pi f C_{Mi}}$$

Where $C_{Mi} = [1-A_V] C_f$

C_{Mi} is called the miller input capacitance.

Where $Z_i = R_i \| C_{Mi}$.

Miller Output capacitance: (C_{MO})



By

$$Z_o = \frac{1}{2\pi f C_{Mo}}$$

$$C_{Mo} = \left[1 - \frac{1}{A_V}\right] C_f.$$

—x—

c) It is desired that the voltage gain of an RC-coupled amplifier at 60 Hz should not decrease by more than 10% from its mid-band value. 5

Calculate: (i) the lower 3 dB frequency.

(ii) the required C if R = 2000Ω.

→ Solution:

We know that 60Hz lies in the low freq region.

(i) $$|A_V| = \frac{1}{\sqrt{1+\left[\frac{f_1}{f}\right]^2}}$$

at $f = 60$ Hz $|A_V| = 0.9$ ← given.

$$\therefore \quad 0.9 = \frac{1}{\sqrt{1+\left[\frac{f_1}{60}\right]^2}}$$

ie $\boxed{f_1 = 29\text{Hz}}$.

(ii) $$f_1 = \frac{1}{2\pi RC}$$

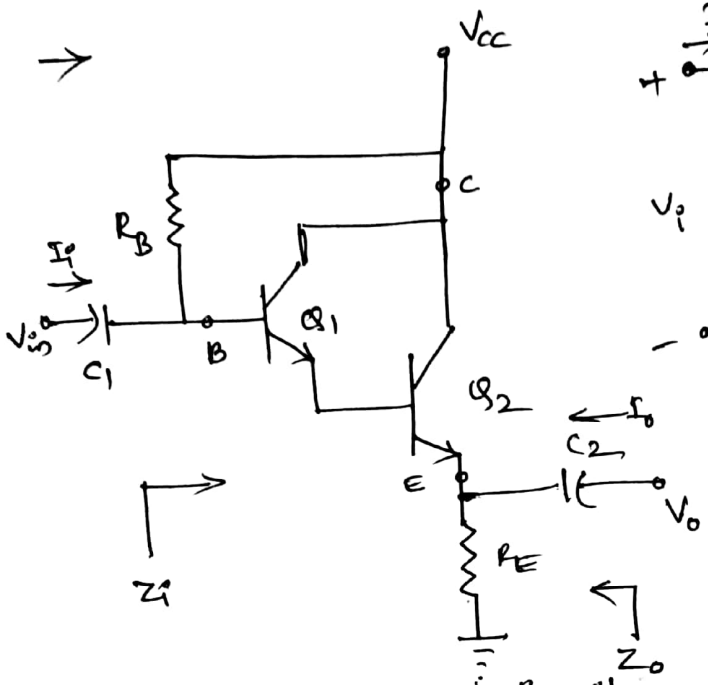
$$C = \frac{1}{2\pi f_1 R} = \frac{1}{2\pi (29)(2000\Omega)}$$

$$\therefore \boxed{C = 2.749\text{F}}.$$

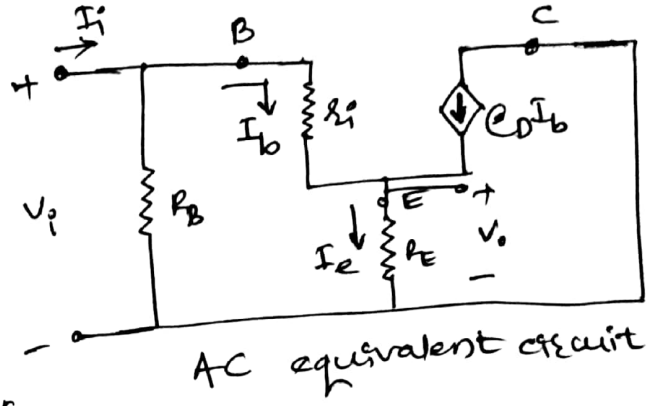
→×←

PART-B

5 a) Derive expressions for Z_i and A_i for a Darlington emitter follower circuit. [10 Marks]



D- emitter follower circuit



AC equivalent circuit.

↳ In AC equi D-trans is replaced by
(i) an i/p rees 'h_i' betn B & E.
(ii) controlled ckt source $\beta_D I_b$. betn C & E

To the base of Darlington transistor input is applied through input coupling capacitor 'C_1'.
III'ly The output is taken from emitter through the output coupling capacitor 'C_2'.

AC Input Impedance 'Z_i':

KVL to i/p ckt;

ie $V_i = I_b h_i + I_e R_E$

We have: $I_E = (1+\beta_D) I_b$,

$\therefore Z_b = \frac{V_i}{I_b} = h_i + (1+\beta_D) R_E$ — (1)

but as β_D is very high

$Z_b \simeq \beta_D R_E$ — (2)

$\therefore Z_i = \frac{V_i}{I_i} = R_B \| Z_b.$

AC current Gain 'A_i':

WKT, $A_I = \frac{I_o}{I_i} = \frac{I_o}{I_b} \cdot \frac{I_b}{I_i}$

but $I_o = I_e$

$\therefore A_I = \frac{I_e}{I_b} \cdot \frac{I_b}{I_i}$ — (1)

$I_e = (1+\beta_D) I_b \simeq \beta_D I_b$ — (2)

$\therefore \frac{I_e}{I_b} = \beta_D$ — (3)

KCL: $I_i = \frac{V_i}{R_B} + I_b \quad \{\because Z_b = \frac{V_i}{I_b}$

using $V_i = I_b Z_b$ we get,

$$I_i = \frac{I_b Z_b}{R_B} + I_b = I_b\left[\frac{Z_b}{R_B}+1\right]$$

$$\text{or} \quad = I_b\left[\frac{Z_b+R_B}{R_B}\right]$$

$$\Rightarrow \quad \frac{I_b}{I_i} = \frac{R_B}{Z_b+R_B} \qquad \text{——— (4)}$$

Use eq² (3) & (4) in eq² (1) we get,

$$A_i = \beta_D \cdot \frac{R_B}{Z_b+R_B} \qquad \text{——— (5)}$$

We have $Z_b = \beta_D R_E$.

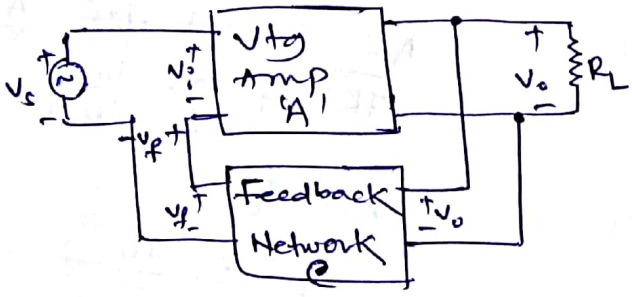
$$\therefore A_i = \beta_D \frac{R_B}{\beta_D R_E + R_B}$$

→

b) Mention the types of feedback connections. Draw their block diagrams indicating input & output signals.

[06 Marks]

→ (i) Voltage-Series feedback:



Gain without feedback $A = \frac{V_o}{V_i}$

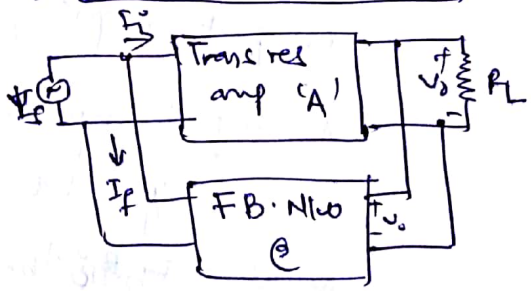
With feedback $A_f = \frac{V_o}{V_s}$

A_{vf} is closed loop Vtg gain.

Feedback factor $\beta = \frac{V_f}{V_o}$

$\Rightarrow V_f = \beta V_o$.

(ii) Voltage-Shunt feedback



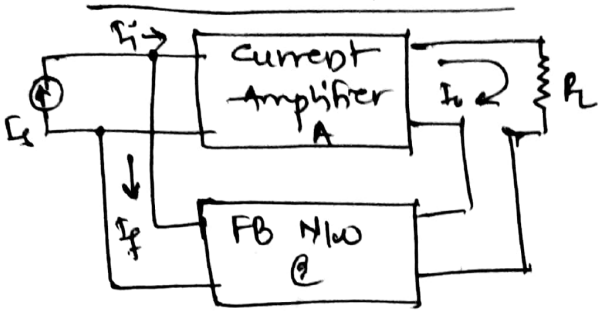
Gain without feedback: $A = \frac{V_o}{I_i}$

With feedback: $A_f = \frac{V_o}{I_i}$

Feedback factor $\beta = \frac{I_f}{V_o}$

i.e. $I_f = \beta V_o$.

(iii) Current-shunt feedback:



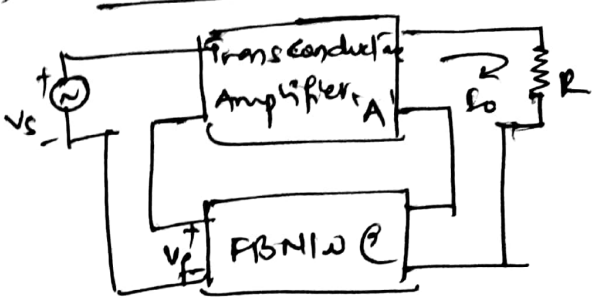
Gain without feedback $A = \frac{I_o}{I_i}$

With feedback $A_f = \frac{I_o}{I_s}$

Feedback factor $\beta = \frac{I_f}{I_o}$

$\therefore \boxed{I_f = \beta I_o}$

(iv) Current-series feedback:



$A = \frac{I_o}{V_i}$

$A_f = \frac{I_o}{V_s}$

$\beta = \frac{V_f}{I_o}$

$\therefore \boxed{V_f = \beta I_o}$

c) List the general characteristics of a negative feedback amplifier and its advantages [04 Marks]

→ General characteristics:

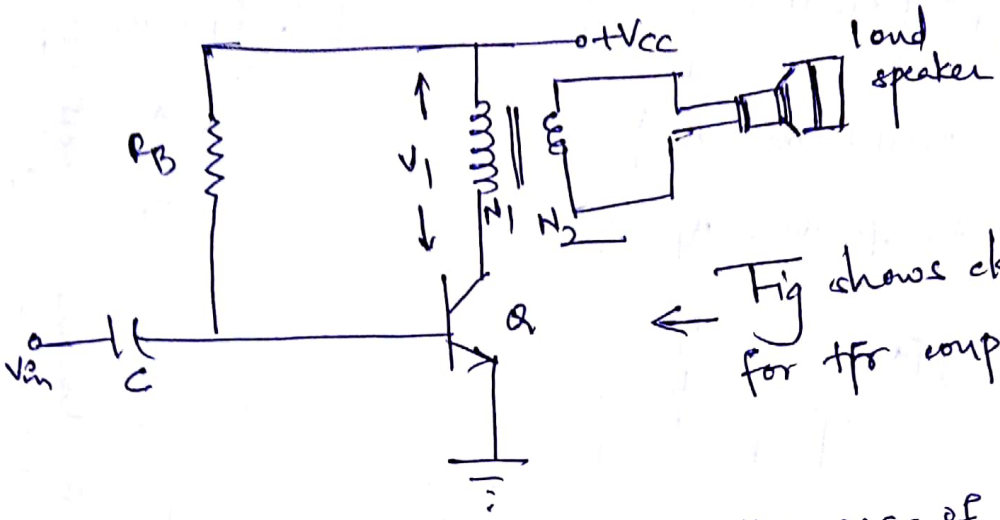
1) Stability of Transfer Gain.
2) Reduction in Noise.
3) Reduction in Frequency Distortion.

Advantages:

1) Increased stability gain.
2) feedback reduces distortion.
3) Bandwidth of amplifier can be increased.

6.
a) With a neat diagram, explain the operation of a transformer coupled class-A power amplifier. [07 Marks]

→



← Fig shows ckt diagram for tfr coupled class-A amplifier.

The load is connected to the sec. of tfr with res R_L.

DC operation:

Assuming zero ohm res of primary & sec wdgs, so there is no dc vtg drop alc primary.

@KT, the slope of the dc load line is reciprocal of res. of collector ckt

Here: $1/R_c = 1/0 = \infty$.

KVL to collector circuit:

$V_{CC} - V_{CE} = 0$ ie $V_{CC} = V_{CE}$ [because we assume 0Ω res @ prim.

$V_{CEQ} = V_{CC}$

& corresponding collector current is I_{CQ}.

∴ DC Power i/p ⇒ $\boxed{P_{DC} = V_{CC} \cdot I_{CQ}}$

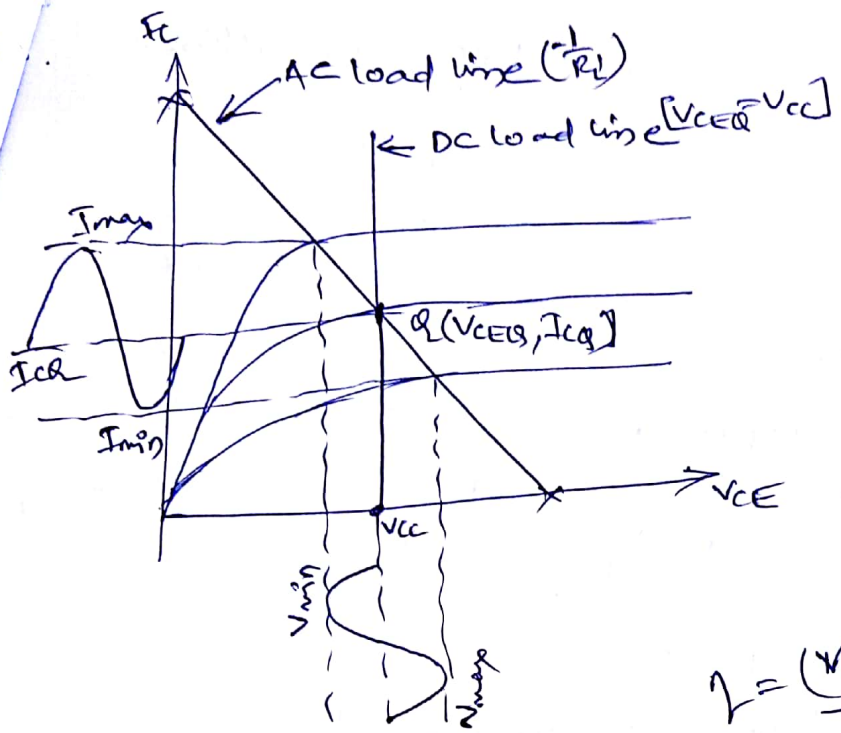
AC operation:

Drawing AC load line on the o/p chars.

for ac, load on sec. is R_L & when reflected on prim it is R_L'.

Where $R_L' = \frac{R_L}{n^2}$ or $\left(\frac{N_1}{N_2}\right)^2 R_L$.

iv)



Output Power:

ac power developed

$P_{ac} = V_{1rms} \cdot I_{1rms}$

or $= I_{1rms}^2 R_L'$

ac power delivered to load

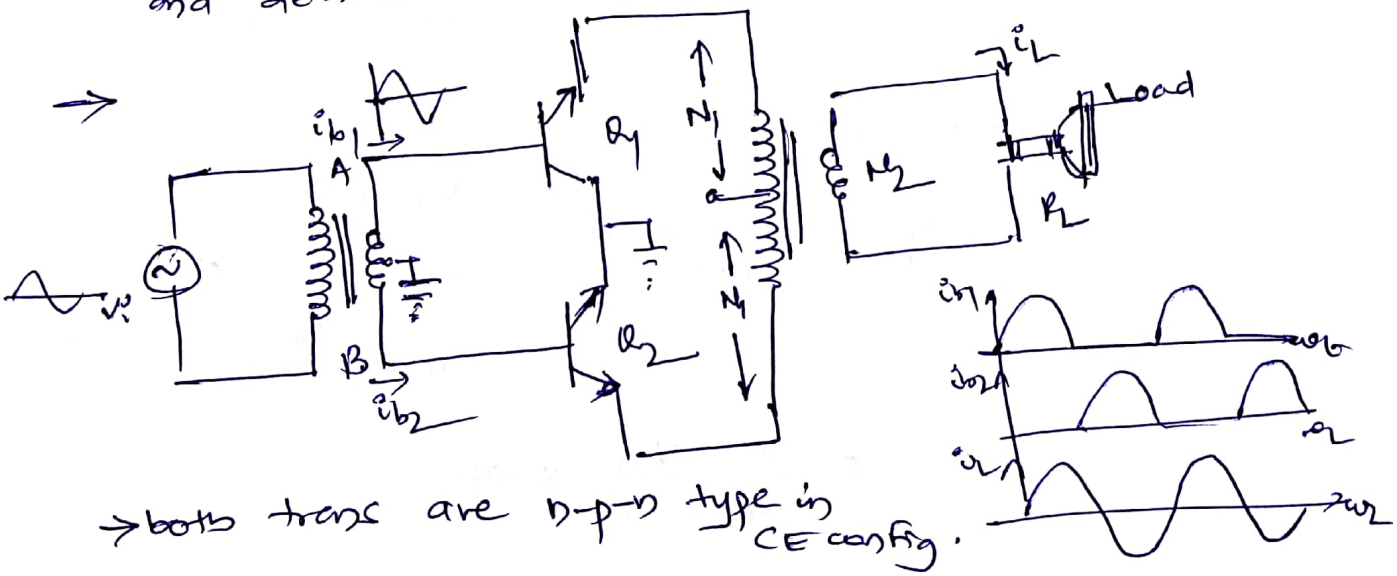
$P_{ac} = V_{2rms} I_{2rms}$

$\therefore P_{ac} = \frac{(V_{max} - V_{min})(I_{max} - I_{min})}{8}$

$\eta = \frac{(V_{max} - V_{min})(I_{max} - I_{min})}{8 V_{CC} \cdot I_{CQ}}$

b) Explain the operation of class-B push pull amplifier and derive its conversion efficiency. [08 Marks]

→



→ both trans are n-p-n type in CE config.

→

DC power input:

Each trans. o/p is in the form of half rectified wave.

If 'I_m' is the peak value of o/p c/n

then avg is given by $= \frac{I_m}{\pi}$ ← [avg value of HWR]

But, 2 trans draws 2 currents of these 2 c/n's from the dc supply which are in same direction, so the total dc or avg c/n is algebraic sum of two c/n's

$$I_{dc} = \frac{I_m}{\pi} + \frac{I_m}{\pi} = \frac{2I_m}{\pi}$$

∴ The total dc power i/p is,

$$\boxed{P_{dc} = \frac{2}{\pi} V_{cc} \cdot I_m}$$

AC power output:

$$P_{ac} = \frac{V_m I_m}{2} = \frac{I_m^2 R_L'}{2} = \frac{V_m^2}{2R_L'}$$

∴ Efficiency:

$$\eta = \frac{P_{ac}}{P_{dc}} * 100 = \frac{\left(\frac{V_m I_m}{2}\right)}{\left(\frac{2}{\pi} V_{cc} I_m\right)} * 100$$

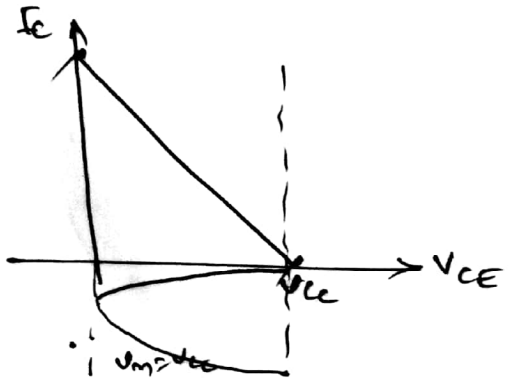
$$= \frac{\pi}{4} \frac{V_m}{V_{cc}} * 100$$

max. efficiency:

$$\%\eta_{max} = \frac{\pi}{4} * \frac{V_m}{V_m}$$

$$= \frac{\pi}{4} * 100$$

$$= 78.5\%$$



—x—

c) The following distortion reading are available for a power amplifier:
$D_2 = 0.2$, $D_3 = 0.02$, $D_4 = 0.06$, with $I_1 = 3.3A$ and $R_c = 4\Omega$. Calculate:
(i) the THD (ii) the fundamental power component
(iii) the total power. [05 Marks]

→ (i) $THD = \sqrt{D_2^2 + D_3^2 + D_4^2} = \sqrt{(0.2)^2 + (0.02)^2 + (0.06)^2} \times 100$

$= 20.97\%$.

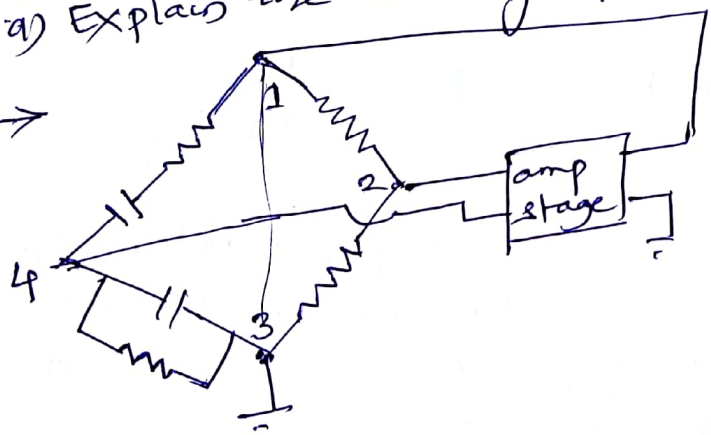
(ii) $P_1 = \frac{I_1^2}{2} R_L = \frac{I_1^2}{2} \cdot R_L = 21.78W$

(iii) Total Power $P_T = P_1 (1 + D^2) = 22.74W$.

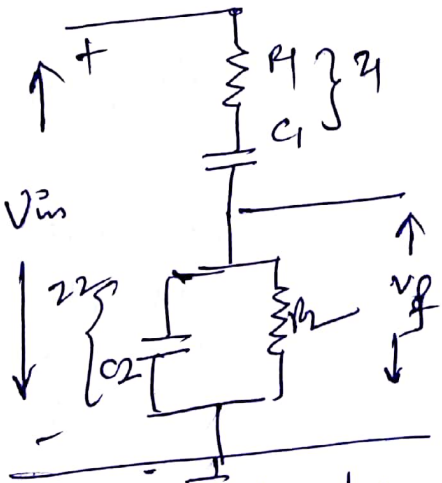
—×—

7. a) Explain the working of Wien Bridge Oscillator. (07)

→



Basic ckt



feedback n/w.

$\frac{R_3}{R_4} = \frac{R_1}{R_2} + \frac{C_2}{C_1}$

freq. of oscillr $f = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}}$

if $R_1 = R_2 = R$ & $C_1 = C_2 = C$

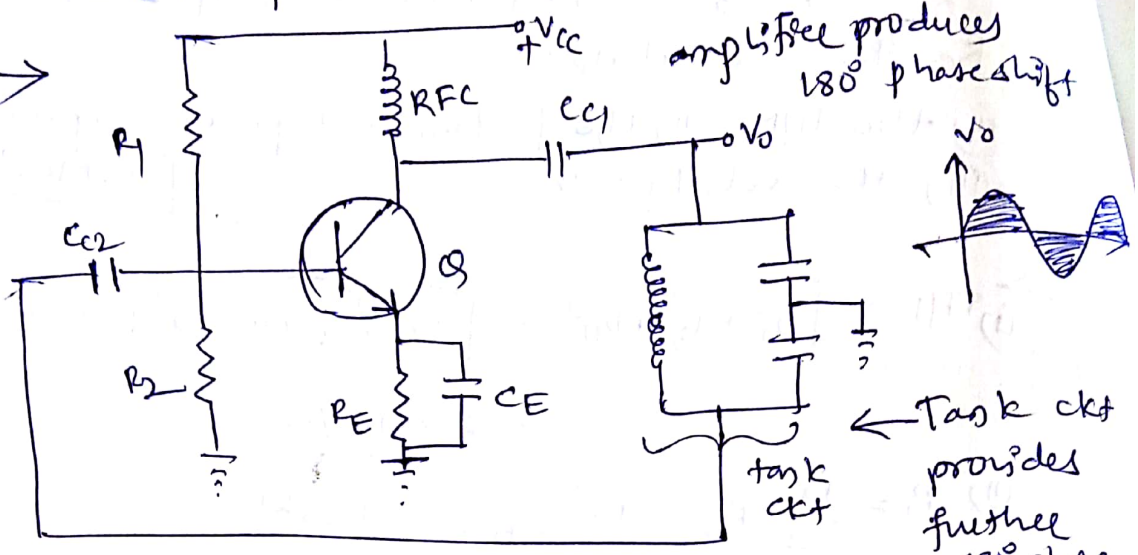
$\therefore f = \frac{1}{2\pi RC}$ $1 + \frac{R_3}{R_4} \geq 3$

$\frac{R_3}{R_4} \geq 2$

or

b) With a neat ckt dgm, explain the op of BJT colpitts Oscillator.

→



an LC oscillator which uses two capacitive reactances and one inductive reactance in the feedback network ie tank circuit, is called Colpitts Oscillator.

Freq of oscillation $f = \frac{1}{2\pi\sqrt{LC_{eq}}}$.

c) A crystal has the following parameter L=0.334H, C_M=1pF, C=0.065 and R=5.5KΩ. Calculate the series resonant frequency, parallel resonant freq and find Q of the crystal.

→ $f_s = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{0.334 \times 1p}} = 1.08 MHz$

$\omega_s = 2\pi f_s = 6.786$ M rad/sec.

$C_p = \frac{C \cdot C_M}{C + C_M} = 0.061$ pF

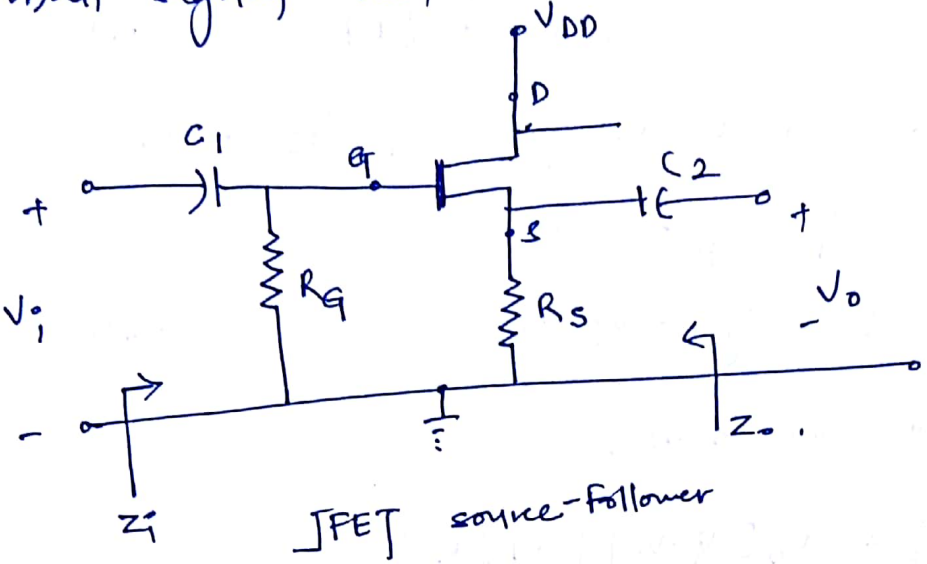
IIle res. freq $f_p = \frac{1}{2\pi\sqrt{LC_p}} = 1.115$ MHz

$\omega_p = 2\pi f_p = 7.005$ M rad/sec.

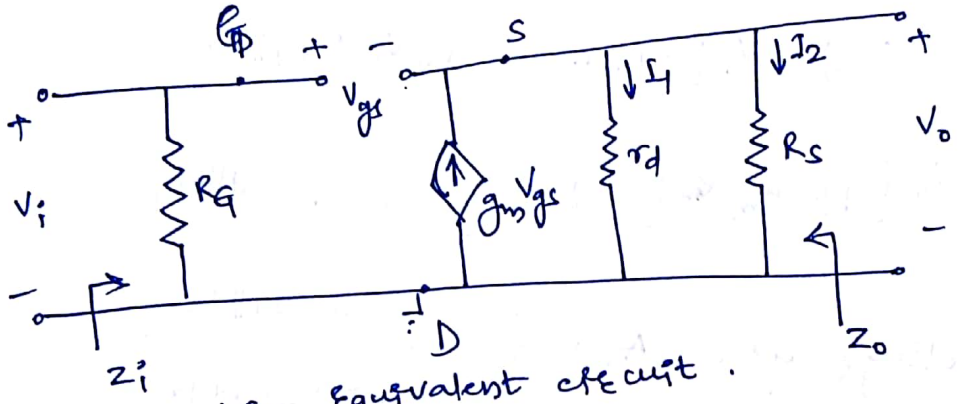
$Q = \frac{\omega_s L}{R} = 412.14$.

8. (a) Draw the JFET common drain configuration (source-follower) circuit. Derive z_i, z_o and Av using small signal model. (10).

→



JFET source-follower



AC Equivalent circuit.

* Input Impedance [Z_i]:

From ac equivalent circuit it is clear that,

$$Z_i = R_G.$$

* Voltage Gain [Av]:

applying KCL at the source node

$$g_m V_{gs} = \frac{V_o}{r_d} + \frac{V_o}{R_S}$$

$$= V_o \left[\frac{1}{r_d} + \frac{1}{R_S}\right]$$

=

$$\therefore g_m V_{gs} = V_o \left[\frac{R_s + r_d}{R_s \cdot r_d}\right]$$

$$\therefore V_o = g_m V_{gs} \left[\frac{R_s r_d}{R_s + r_d}\right]$$

i.e. $$V_o = g_m V_{gs} [R_s \parallel r_d] \quad \text{——(i)}$$

applying KVL to path V_i, V_{gs} & V_o.

$$\therefore V_i - V_{gs} - V_o = 0.$$

$$\text{or} \quad V_{gs} = V_i - V_o. \quad \text{——(ii)}$$

using (ii) in (i),

$$V_o = g_m [V_i - V_o] [r_d \parallel R_s]$$

$$= g_m V_i [r_d \parallel R_s] - g_m V_o [r_d \parallel R_s]$$

$$V_o \left[1 + g_m V_o [r_d \parallel R_s]\right] = g_m V_i [r_d \parallel R_s]$$

$$\therefore \text{Voltage gain } A_V = \frac{V_o}{V_i} = \frac{g_m [r_d \parallel R_s]}{1 + g_m [r_d \parallel R_s]}$$

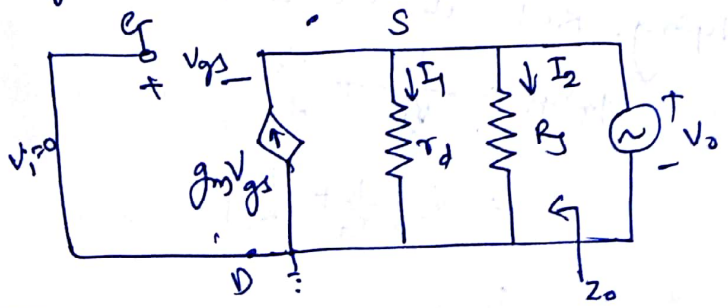
V_o & V_i both are in-phase.

* Output Impedance [Z_o]:

To find the output impedance

→ Input voltage V_i is set to zero. [R_G gets short circuited]

→ Voltage source V_o is connected betⁿ o/p terminals.



(b) Compare JFET & MOSFET.

→

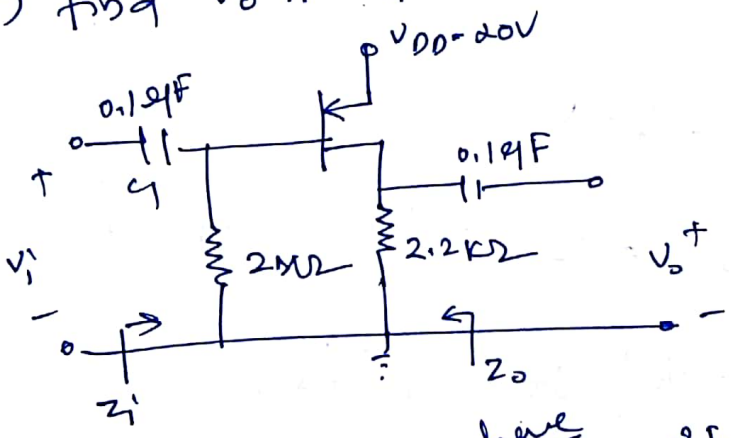
(c) For JFET common drain configuration shown below

Given $I_{dss} = 10mA$, $V_p = -5V$, $r_d = 40k\Omega$,

$V_{GSQ} = -2.85\ V$

i) calculate Z_i & Z_o ii) calculate A_V

iii) find V_o if $V_i = 20mV$ (p-p).



→ $g_m = g_{mo}\left[1 - \frac{V_{GSQ}}{V_p}\right]$ where $g_{mo} = \frac{2I_{DSS}}{|V_p|} = \frac{2(10m)}{5V} = 4mS$

$\therefore g_m = 4mS\left[1 - \frac{-2.85V}{-5V}\right] = 1.72\ mS$

i) $Z_i = R_G = 2M\Omega$ $\quad Z_o = \frac{1}{g_m} \| r_d \| R_S$

$\therefore \frac{1}{g_m} = \frac{1}{1.72mS} = 581.39\Omega$

$Z_o = 581.39\Omega \| 40k\Omega \| 2.2k\Omega = 454.63\Omega$

ii) $A_V = \frac{g_m[r_d \| R_S]}{1 + g_m[r_d \| R_S]}$ $\quad$ iii) $V_o = A_V V_i$

$= 0.7818$ $\quad = [0.7818][20mV]$

$= 15.636\ mV\ (p\text{-}p)$

From fig $Z_o = \frac{V_o}{I_o}$ ——(i)

KCL at node 's'

$$I_o + g_m V_{gs} - I_1 - I_2 = 0 \quad \text{——(ii)}$$

here $I_1 = \frac{V_o}{r_d}$ $\quad I_2 = \frac{V_o}{R_s}$ ——(iii)

using (iii) in (ii)

$$I_o + g_m V_{gs} - \frac{V_o}{r_d} - \frac{V_o}{R_s} = 0.$$

Applying KVL to path V_i, V_{gs} & V_o.

$$\therefore \quad V_i - V_{gs} - V_o = 0$$

as $V_i = 0$

$$\therefore \quad -V_o = V_{gs}$$

$$\therefore \quad I_o - g_m V_o - \frac{V_o}{r_d} - \frac{V_o}{R_s} = 0$$

$$I_o = V_o \left[g_m + \frac{1}{r_d} + \frac{1}{R_s} \right]$$

Now $$Z_o = \frac{V_o}{I_o} = \frac{1}{g_m + \frac{1}{r_d} + \frac{1}{R_s}}$$