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THIRD SEMESTER B.E DEGREE EXAMINATION

JUNE/JULY – 2014.

ANALOG ELECTRONIC CIRCUITS

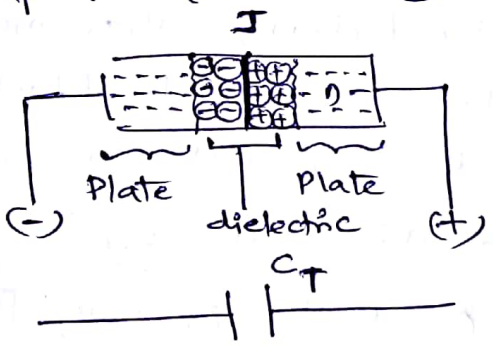
1.

a) With respect to a semiconductor diode, explain the following:

i) Transition & Diffusion capacitance.

ii) Reverse Recovery Time.

→ When a diode is reverse biased, the width of the depletion region increases & there will be more collection of the +ve & -ve charges present at depletion region.



Here p-region & n-region act like the plates of capacitor & depletion region act like dielectric.

Hence here exists a capacitance at the p-n junction. called TRANSITION CAPACITANCE or depletion region capacitance C_T.

mathematically, $C_T = \frac{\varepsilon A}{W}$

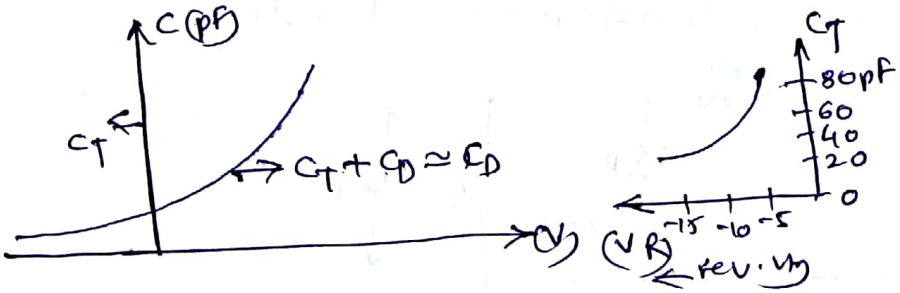
$\varepsilon = \varepsilon_0 \varepsilon_r$

$\varepsilon_0 = 8.849 \times 10^{-12}$ F/m.

ε_r = 16 for Ge
12 for Si

A = area of cross section.

W = width of dep. region



For a fwd biased condn, the width of depletion region decreases, holes from p-side starts diffusing to n-side & electrons from n-side moves to p-side. As the voltage increases concentration of charged particles increases.

"This rate of change of the injected charge with applied voltage is nothing but the diffusion capacitance"

$\therefore C_D = \frac{dQ}{dV}$

mathematically, $C_D = \frac{\tau I}{\eta V_T}$ — τ ← mean lifetime for holes.

from eq² $C_D \propto I$

for fwd biased condition ← C_D ranges from nF to μF

while C_T in terms pF

ie C_T is much higher than C_D.

(ii) Reverse Recovery Time:

when switching from the conducting to the blocking state, a diode has stored charge that must first be discharged before the diode blocks reverse current. This discharge takes a finite amount of time known as RRT 'trr'

During this time the diode cln may flow in the reverse direction.

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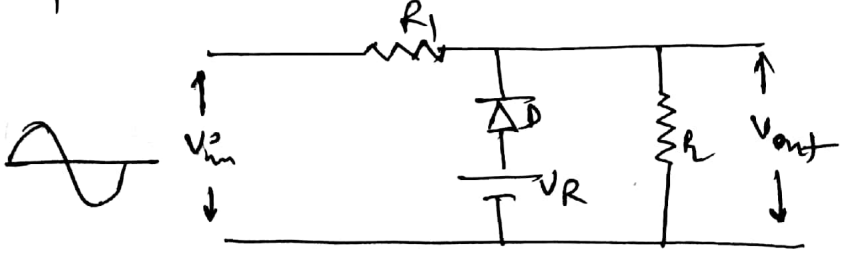
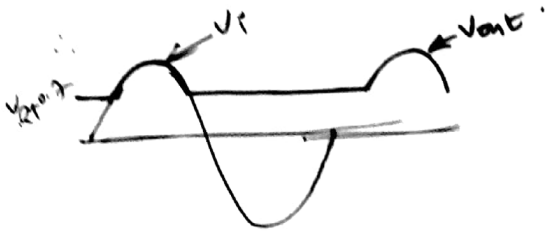
b) Explain the operation of the circuit shown. Draw output waveform & transfer characteristics



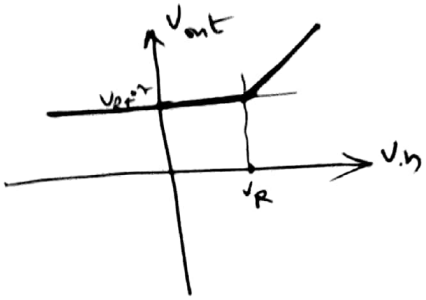
→ Let input V_{in} is applied with peak value V_m greater than V_R. If $V_m < V_R$

the half cycle — $V_R < V_{in} < V_m$. — Diode is off $\therefore V_o = V_{in}$.

$V_R < V_{in}$ — Diode is ON $\therefore V_o = V_R + 0.7V$.

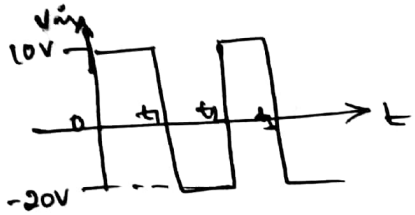


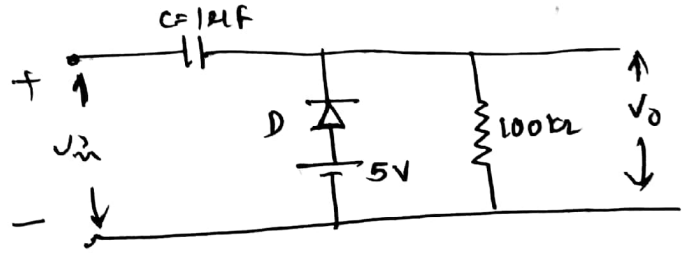
waveforms.



Transfer Characteristics

c) Write the procedure for analyzing the clamping circuit. Determine output voltage for the given shown. Assume $f = 1000Hz$ and ideal diode.

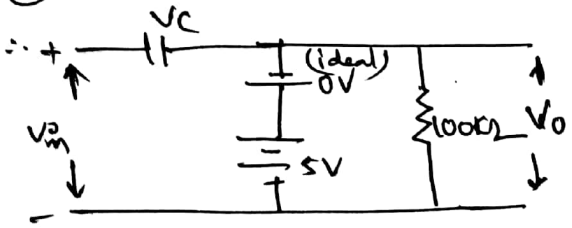




→ Output voltage V_o when diode is ON:

Diode is ON @ when $V_R > V_{in}$

@ when $V_i = -20V$ diode is ON.



writing KVL

$5V - V_C - V_{in} = 0$

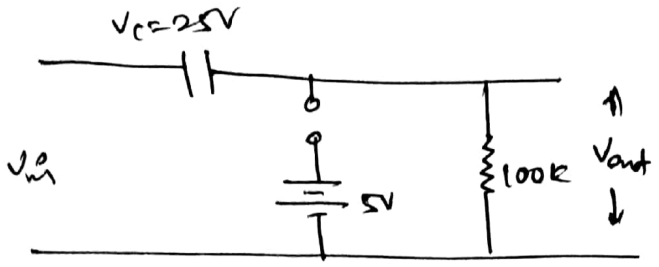
$\therefore -V_C = V_{in} - 5V$

$\therefore V_C = 20 + 5 = 25V$

$\therefore V_o = -20 + 25 = 5V$

Output voltage when diode is off:

@ when $V_i = 10V$ diode is off.



KVL:

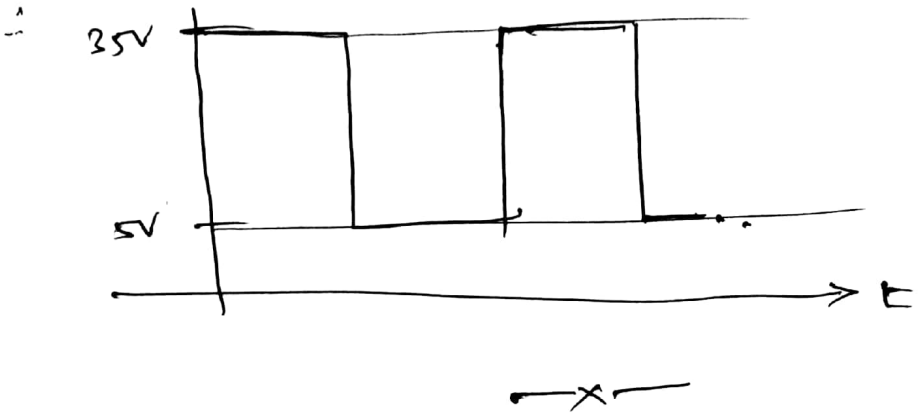
$V_i + V_C - V_o = 0$

$\therefore V_o = -V_i + V_C$

$V_o = +10 + 25 = 35V$

i.e. when $V_i = -20V$ $V_o = 5V$

$V_i = 10V$ $V_o = 35V$



2 a) What is biasing? Discuss the factors causes for bias instability in a transistor.

→ To operate transistor in a desired region, we need to apply external dc voltages of correct polarity & magnitude to the two junctions of the transistor.

Factors affecting stability:

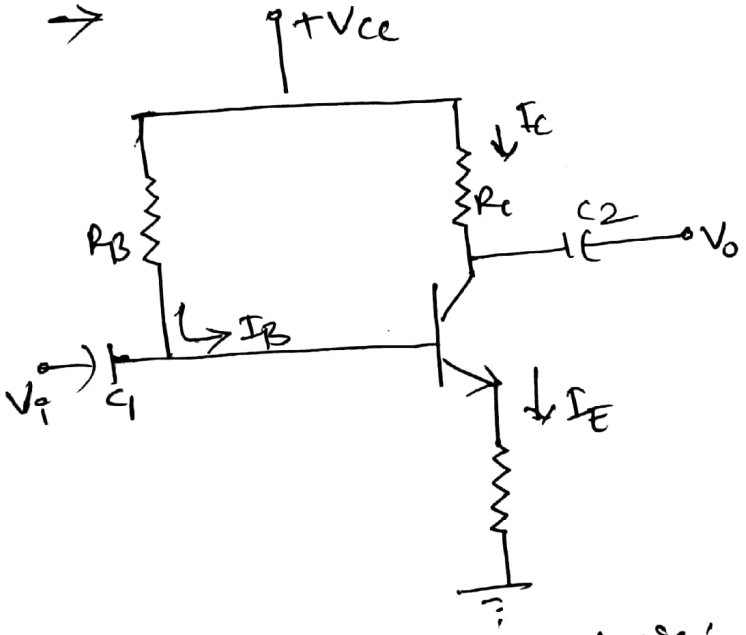
1. Temperature
   a) I_{CO} ↑
   b) V_{BE} ↓

2. change in β value.

If β ↑ I_C ↑ which changes the position of Q-point.

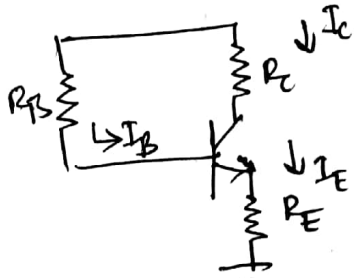
b) With circuit diagram, explain Emitter stabilized bias circuit. Write the necessary equations. (7)

→

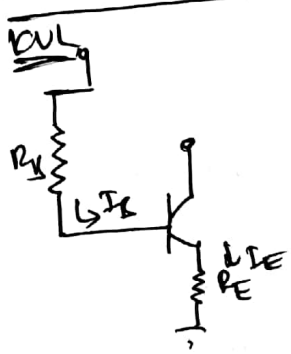


* An emitter resistor 'R_E' is added to improve the stability.

* Let us replace caps by open circuit.



Base-Emitter loop analysis:



$\therefore V_{CC} - I_B R_B - I_E R_E + V_{BE} = 0$

We have, $I_E = (\beta+1) I_B$

$\therefore V_{CC} = I_B R_B + I_B R_E (\beta+1) + V_{BE}$.

$\therefore$

or $\therefore V_{CC} = I_B [R_B + R_E(\beta+1)] + V_{BE}$.

$$\therefore I_B = \frac{V_{CC} - V_{BE}}{R_B + R_E(\beta+1)}$$

collector emitter loop analysis:

KVL $\quad V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$

we have $I_C \simeq I_E$

$\therefore \quad V_{CE} = V_{CC} - I_C [R_C + R_E]$.

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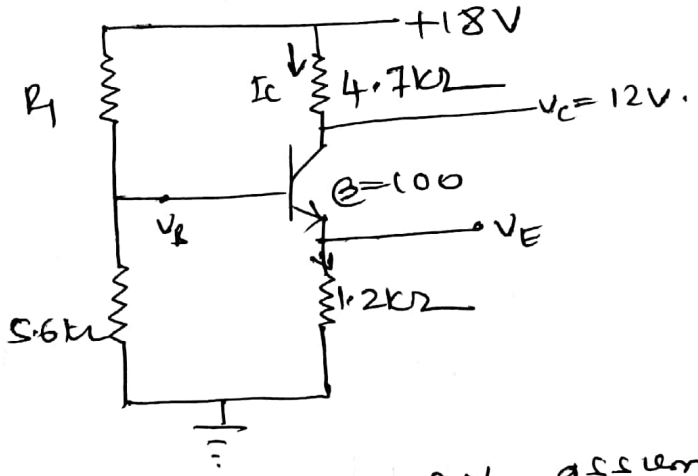
c) For the circuit shown in figure, find I_C, V_B, V_E, R_1 and $\beta_{(dc)}$.



→ Given $\beta = 100$, $V_{CC} = 18V$ & $V_C = 12V$ assume $V_{BE} = 0.7V$

$I_C = ?$ $\quad V_E = ?$ $\quad V_B = ?$ & $R_1 = ?$

we have

$$V_B = \frac{R_2}{R_1 + R_2} \cdot V_{CC}$$

$$= \frac{5.6K}{R_1 + 5.6K} * 18 \quad \text{—(1)}$$

$$R_1 \parallel R_2 = \frac{R_1 * 5.6K}{R_1 + 5.6K} \quad \text{—(2)}$$

@KL, $\quad I_C = \frac{V_{CC} - V_C}{R_C} = \frac{18-12}{4.7K} = 1.28mA$

$\therefore \quad I_B = \frac{I_C}{\beta} = 12.76\mu A$

as $I_E \simeq I_C + I_B = 1.29mA$

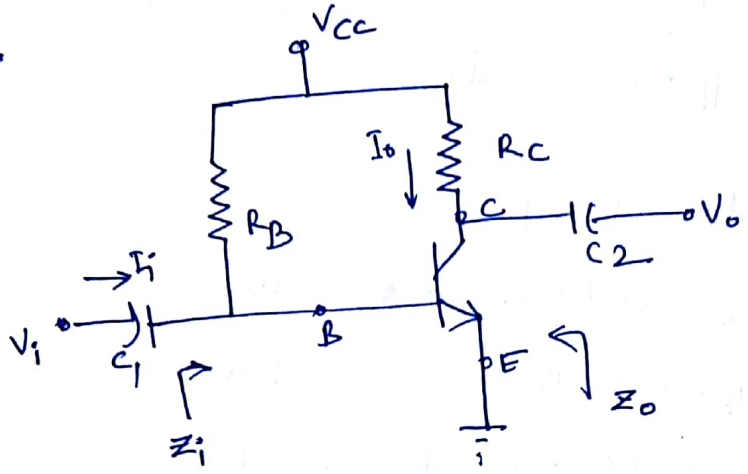
$V_E = I_E R_E = 1.51V$

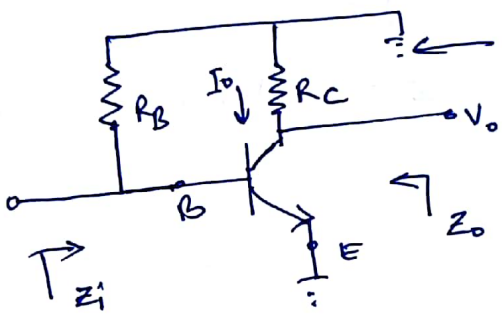
Base $\quad V_B - I_B R_{eq} - V_{BE} - I_E R_E = 0 \Rightarrow R_1 = 38K\Omega$

$\therefore \quad V_B = \frac{5.6K}{38K + 5.6K} * 18 = 2.31V$

3. g) Draw the circuit diagram of common emitter fixed bias configuration. Derive the expression for Z_i, Z_o, A_v using r_e-model. [08]

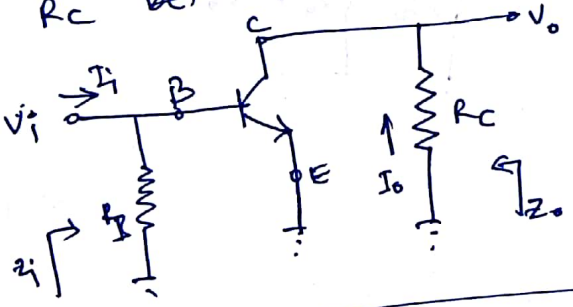
→



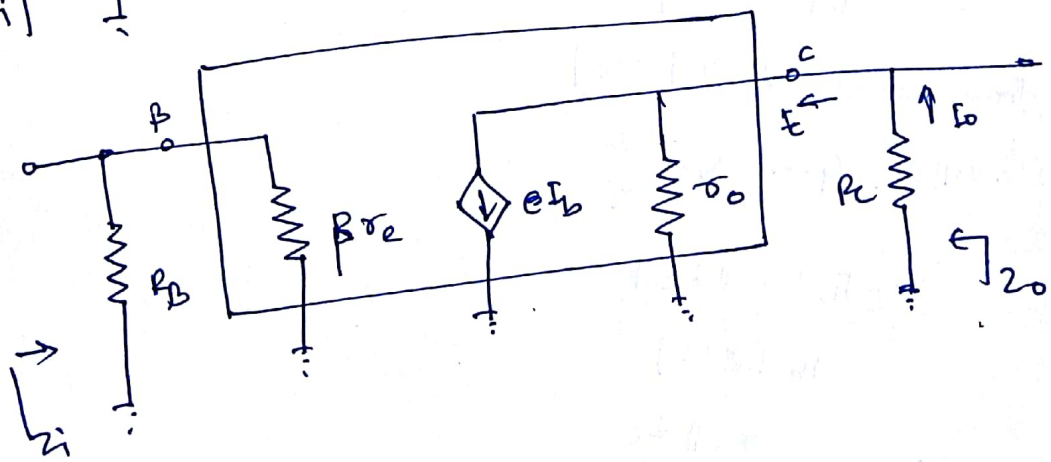


← AC Equivalent circuit

R_B appears between Base and ground and R_C between collector & ground.



← Simplified AC equi. circuit



PART-A

Input Impedance [Z_i]:

$$Z_i = \frac{V_i}{I_i} \quad \text{---- (i)}$$

from r_e-model,

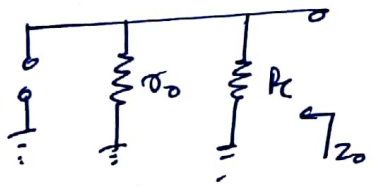
$$Z_i = R_B \parallel \beta r_e \quad \text{---- (ii)}$$

output Impedance [Z_o]:

to find Z_o reduce V_i to zero.

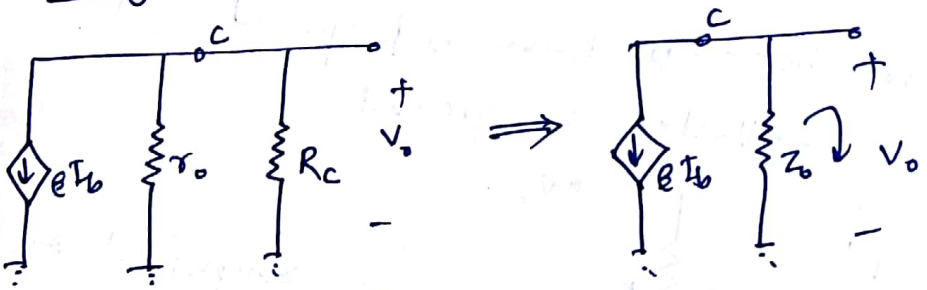
for $V_i = 0$, $I_i = 0$ & $I_b = 0$ $\therefore \beta I_b = 0$.

$\therefore$ c/p source is open circuited.



$\therefore Z_o = r_o \parallel R_c$.

Voltage Gain [A_V]:



$V_o = -\beta I_b Z_o$.

$= -\beta I_b [r_o \parallel R_c]$

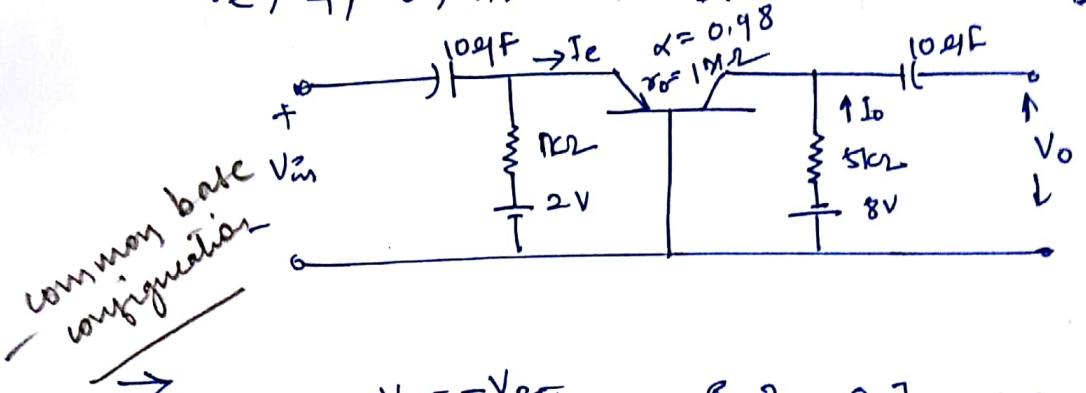
from circuit $V_i = I_b [\beta r_e]$

$\therefore$ voltage Gain $A_V = \frac{V_o}{V_i}$

$$= \frac{-\beta I_b [r_o \parallel R_c]}{I_b [\beta r_e]}$$

$$A_V = -\frac{r_o \parallel R_c}{r_e}$$

3 b). For the network shown, determine r_e, Z_i, Z_o, A_V and A_I. 06



→ (a) $I_E = \frac{V_{EE} - V_{BE}}{R_E} = \frac{2 - 0.7}{1K\Omega} = 1.3mA$

$r_e = \frac{26mV}{I_E} = \frac{26mV}{1.3m} = 20\Omega$

(b) $Z_i = R_E \| r_e = 1K\Omega \| 20\Omega = \frac{1K \times 20}{1K + 20} = 19.6\Omega$

(c) $Z_o = R_C = 5K\Omega$

(d) $A_V = \frac{\alpha R_C}{r_e} = \frac{(0.98)(5K\Omega)}{20} = 245$

(e) $A_I = -\alpha = -0.98$

—X—

(c) What are the advantages of h-parameters ? 6

→ 1) Easy to measure.
2) Real numbers at audio frequencies.
3) Can be obtained from static transistor char
4) Convinient to use in ckt analysis & design the hybrid equivalent for the 3-configuration

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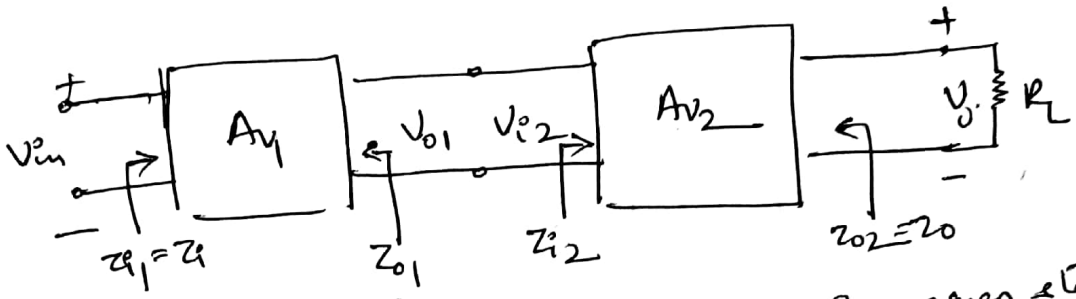
5. g) Explain the need of cascading amplifier? Draw & explain the block diagram of two stage cascade amp?

→ Need of cascading amplifiers:



From above fig, the i/p impedance of a given stage is nothing but output impedance of previous stage.

Let voltage gains as, A_{V_1} & A_{V_2} of 2 stages.

These values can be calculated by using no-load gains of particular stages.

From fig: It is clear that, the i/p impedance of first stage is nothing but i/p imp of the cascaded system & the o/p imp of the system is nothing but o/p impedance of last stage.

i.e $Z_i = Z_{i_1}$ and $Z_o = Z_{o2}$

as o/p of 1st stage is connected as i/p to the next stage. $\therefore V_{i2} = V_{o1}$

$\therefore$ Total Ag gain of the cascaded system is,

$$A_{V_{total}} = \frac{V_o}{V_{in}} = \frac{V_o}{V_{i2}} \cdot \frac{V_{i2}}{V_{in}}$$

$\therefore A_{V_{Total}} = A_{V_1} \cdot A_{V_2}$.

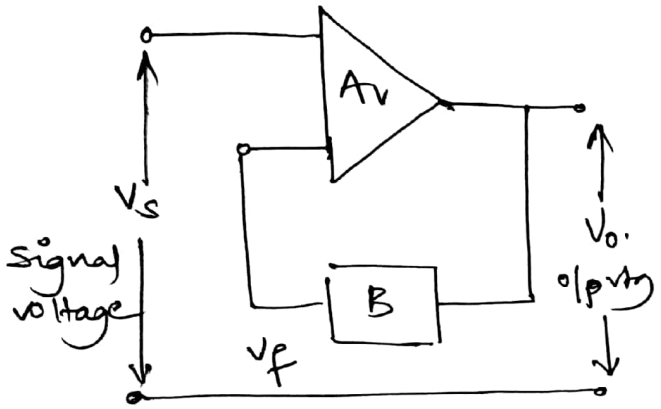
A_{V_1} — Vtg gain of 1st st

A_{V_2} — ——— 2nd st

—×—

b) With block diagram, explain the concept of feedback amplifier. If an amplifier has mid-band vtg gain ($A_{V\text{-mid}}$) of 1000 with $f_L = 50$Hz and $f_H = 50$kHz, if 5% feedback is applied then calculate f_L and f_H with feedback.

→



small portion of o/p is fed back to the input.

open loop gain $\cdot A_V = \frac{V_o}{V_{in}}$

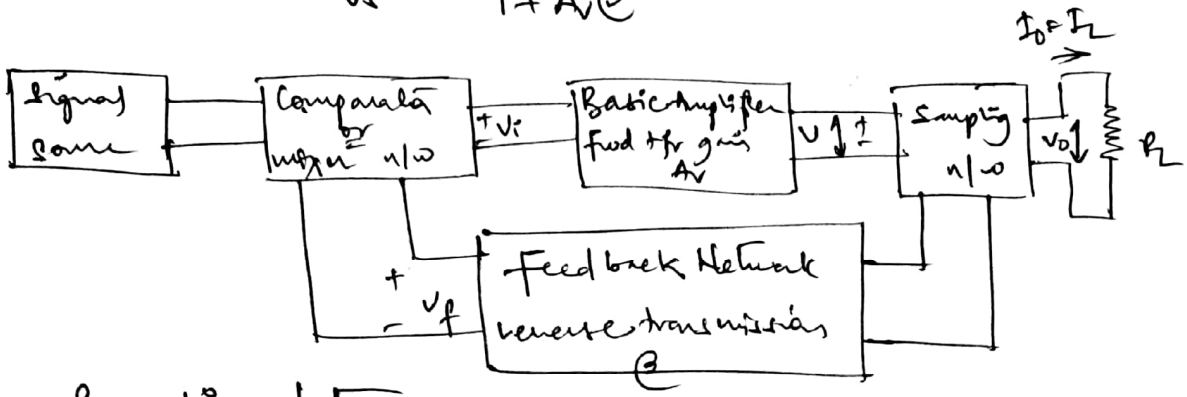
feedback factor $\beta = \frac{V_f}{V_o}$

Overall Gain $= A_{V_{C-L}} = \frac{V_o}{V_s}$

@e have input vtg $V_{in} = V_s - V_f$

$= V_s - \beta V_o$

$$\frac{V_o}{V_s} = \frac{A_V}{1 + A_V \beta}$$



* Sampling Network
* Feedback Network
* Mixer Network.

Given

$A_V = 1000$ $\quad \beta = \frac{5}{100} = 0.05$, $f_L = 50$, $f_H = 50\,kHz$

$f_{L\,feedback} = \frac{f_L}{1+\beta A_{Vmid}} = \frac{50}{1+0.05\times1000} = 0.98\,Hz$

$f_{H\,feedback} = f_H * (1+\beta A_{Vmid}) = 50k * (1+0.05*1000)$

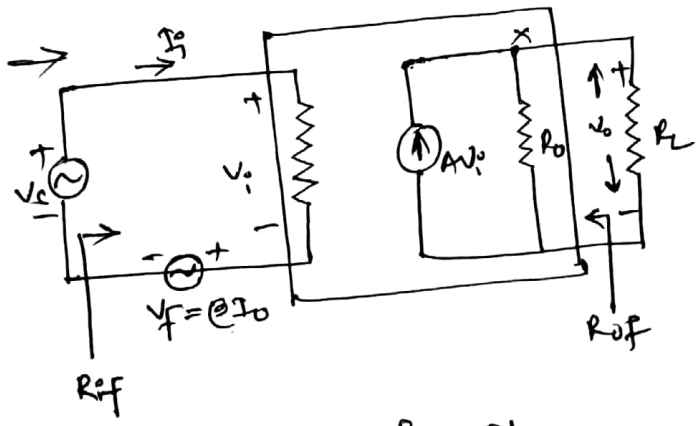
$= 2.55\,MHz$.

Gain with feedback $= \frac{A_{Vmid}}{1+\beta A_{Vmid}} = \frac{1000}{1+(0.05*1000)}$

$= 19.6$.

—x—

c) Derive the expression for input resistance (R_{if}) for feedback amplifier employing current series feedback.



$R_i = \frac{V_i}{I_i}$ ← i/p res without feedback.

$R_{if} = \frac{V_s}{I_i}$ ← i/p res with feedback.

KVL for i/p circuit,

$-V_f - V_i + V_s = 0$

We have, $V_i = I_i R_i$ and $V_f = \beta I_o$

$\therefore V_s - I_i R_i - \beta I_o = 0$

$I_o = AV_i = A I_i R_i$

$\therefore V_s - I_i R_i - \beta A I_i R_i = 0$

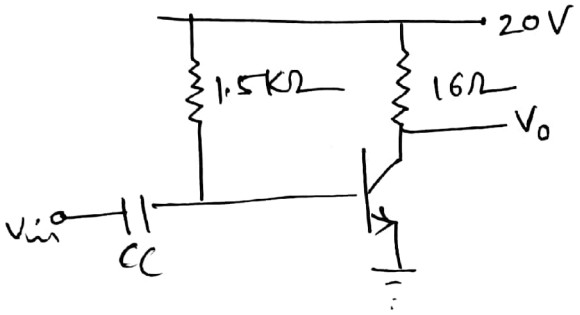
$\therefore V_s = I_i R_i [1+\beta A]$

$\therefore \boxed{R_{if} = \frac{V_s}{I_i} = R_i [1+\beta A]}$ → i/p res increases by $1+\beta A$ factor for series mixing.

as $[1+\beta A] > 1$

$R_{if} > R_i$

6. a) A series fed class-A amplifier shown operates from dc source & applied sinusoidal i/p signal generates peak base c/r 9mA. Calculate I_{CQ}, V_{CEQ}, P_{DC}, P_{ac} & η, Assume $\beta = 50$ & $V_{BE} = 0.7V$.



→ Given

We have $I_{BQ} = \frac{V_{CC} - V_{BE}}{R_B} = \frac{20 - 0.7}{15K} = 12.86mA$

$I_{CQ} = \beta I_{BQ} = 50 * 12.86m = 0.643A$

$V_{CEQ} = V_{CC} - I_{CQ} * R_L$

$= 20 - 0.643 * 16 = 9.71V$

$P_{dc} = V_{CC} * I_{CQ} = 20 * 0.643 = 12.86W$.

For P_{ac} we have $i_b = 9mA$ $\therefore i_c = \beta i_b = 50 * 9m = 450mA$ (Peak)

$\therefore i_{c(rms)} = \frac{450m}{\sqrt{2}} = 318.2mA$ rms.

$P_{ac} = I_{rms}^2 R_L = (318.2 * 10^{-3}) * 16 = 1.62W$

$\therefore$ Efficiency $\eta = 12.58\%$.

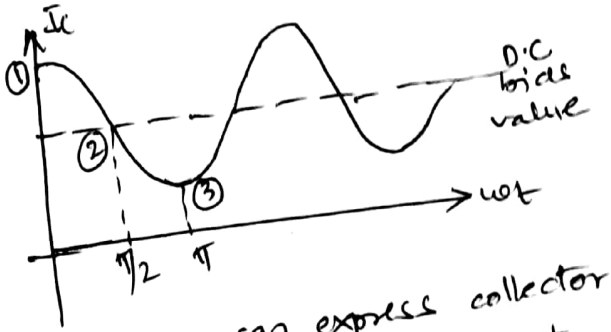
—x—

(6)

b) What is harmonic distortion? Explain the 3-pt method of calculating the second harmonic distortion.

→ **Harmonic Distortion**: Presence of freq components in the o/p w/f which are not present in the i/p.

The additional frequency components present in output are having frequency components present in ~~every~~ which are integer multiples of fundamental freq component, those are called Harmonics.



$i_C = B_0 + B_1 \cos \omega t + B_2 \cos 2\omega t$ — (1)

2nd harmonic

Now we can express collector c/r interms of its dc bias value, signal component, fundamental freq & 2nd Harmonic component.

$i_C = I_{CQ} + B_0 + B_1 \cos \omega t + B_2 \cos 2\omega t$ ——— (2)

Where: $I_{CQ} + B_0$ — dc component & independent,

B_1 ← Amp. of fund a freq

b_2 ← 2nd harmonic comp.

@ point 1, $\omega t = 0$,

$i_c = I_{CQ} + B_0 + B_1 + B_2$ ——— (3)

@ point 2, $\omega t = \pi/2$,

$\therefore i_C = I_{CQ} + B_0 - B_2$ ——— (4)

@ point 3, $\omega t = \pi$

$\therefore i_C = I_{CQ} + B_0 - B_1 + B_2$ ——— (5)

But (2) $\omega t = 0$, $i_C = I_{max}$

$\omega t = \pi/2$, $i_C = I_{CQ}$

$\omega t = \pi$, $i_C = I_{min}$

ie ③ ④ ⑤ below

$I_{max} = I_{CQ} + B_0 + B_1 + B_2$ ——— ⑥

$I_{CQ} = I_{CQ} + B_0 - B_2$ ——— ⑦

$I_{min} = I_{CQ} + B_0 - B_1 + B_2$ ——— ⑧

From 7 & 8, $B_0 = B_2$

we have $I_{max} - I_{min} = 2B_1$ ← Peak to Peak

eq² ⑥ - eq² ⑨ =

or $B_1 = \frac{I_{max} - I_{min}}{2}$ ——— ⑨

eq² ⑦ + eq² ⑨ we get,

$I_{max} - I_{min} = 2I_{CQ} + 2B_0 + 2B_2$

$= 2I_{CQ} + 2B_2 + 2B_2$

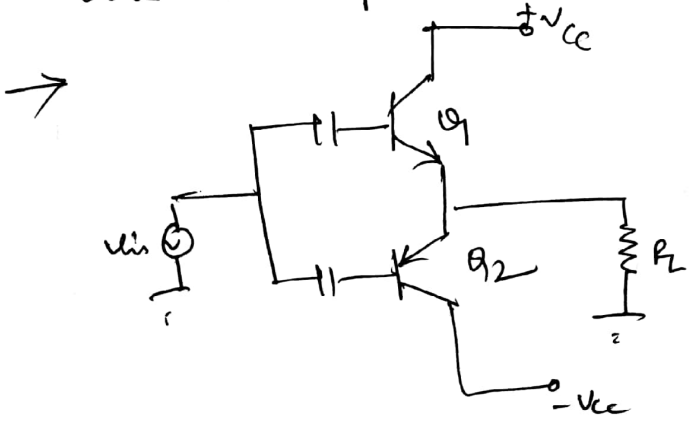
$= 2I_{CQ} + 4B_2$

$\therefore B_2 = \frac{I_{max} - I_{min} - 2I_{CQ}}{4}$ ——— ⑩

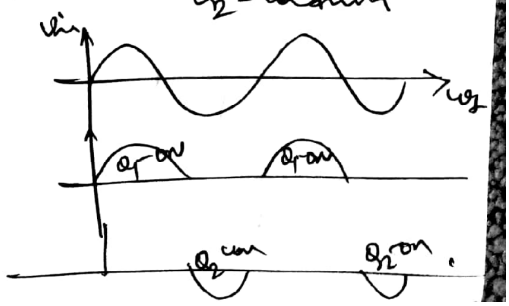
Now we know the amplitudes of fundamental & second harmonic components so, the 2nd harmonic distortion is calculated as,

$\%D_2 = \frac{|B_2|}{|B_1|} * 100$ also known as 3-point method.

c) Explain the working of complementary symmetry class-B amplifier.

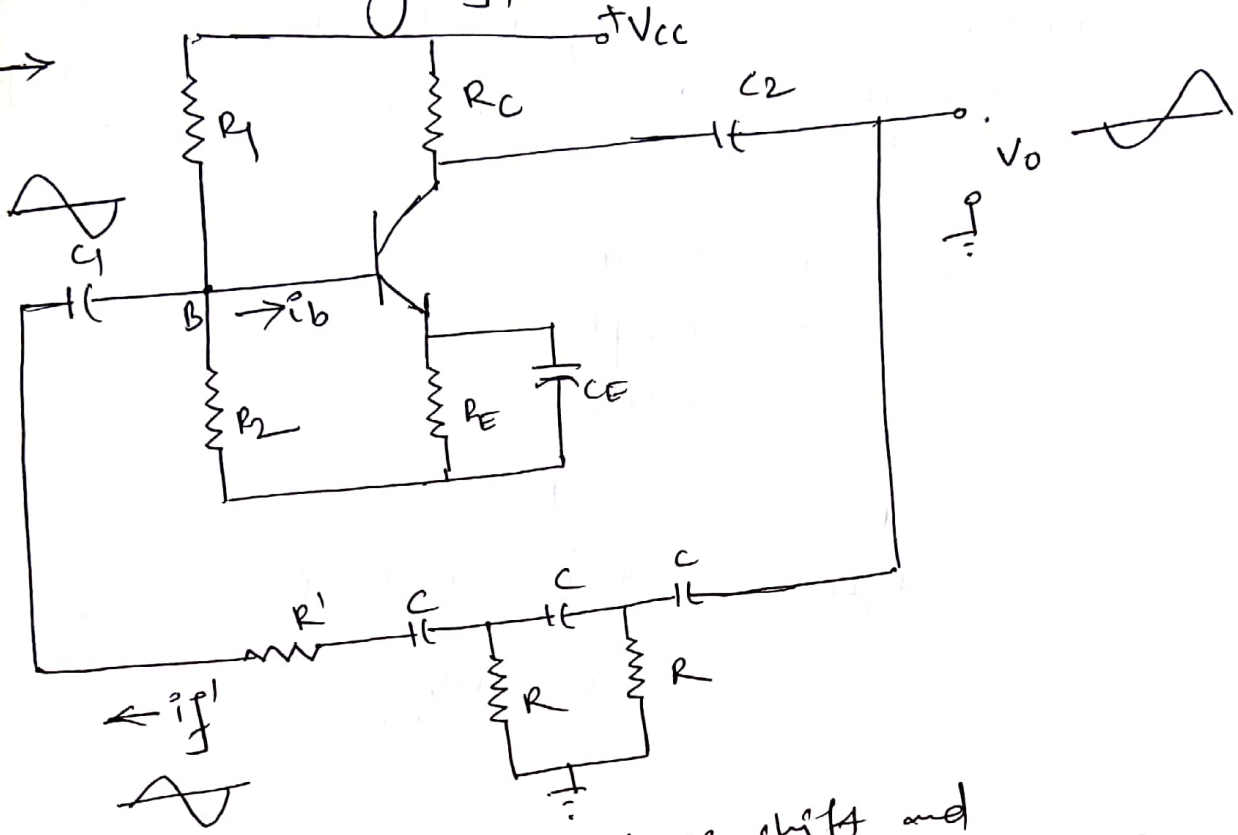


during the half cycle
Q_1 - conducts
during the half cycle
Q_2 conducts



7.

a) With circuit diagram, explain RC phase shift oscillator using BJT.



transistor adds 180° phase shift and RC network adds -180°. so total is 360°.

—x—

b) In a transistorized Hartley oscillator the two inductances are 2mH and 20μH, while the freq is to be changed from 950kHz to 2050kHz. Calculate the range over which the cap is to be varied.

→ $L_1 = 2mH$ $L_2 = 20\mu H$

$\therefore L_{eq} = L_1 + L_2 = 20\mu + 2m = \underline{2.02mH}$

for $f = f_{max}$, $f = \frac{1}{2\pi\sqrt{C * L_{eq}}}$ i.e. $2050K = \frac{1}{2\pi\sqrt{C * 2.02m}}$

$\therefore \underline{C = 19mF}$.

for $f = f_{min}$ $950K = \frac{1}{2\pi\sqrt{C * 2.02m}}$ $\therefore \underline{C = 41mF}$

—x—

9) With circuit diagram, explain the working principle of crystal oscillator in series resonant mode. A crystal has the following parameters L = 0.334H, C = 0.065pF and R = 5.5kΩ. Calculate resonant freq.

→ Given

$L = 0.334\,H$

$C = 0.065\,pF$

$R = 5.5\,k\Omega$

$$f_s = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{0.334 \times 0.065p}} \times 10^{12}$$

$$= 1.08\,MHz$$