MICROWAVES AND ANTENNAS

B.E., VII Semester, Electronics &Communication Engineering

[As per Choice Based Credit System (CBCS) scheme]

Subject Code	15EC71	IA Marks	20
Number of Lecture Hours/Week	04	Exam Marks	80
Total Number of Lecture	50 (10 Hours / Module)	Exam Hours	03
CREDITS – 04			

Modules

Module-1

Microwave Tubes: Introduction, Reflex Klystron Oscillator, Mechanism of Oscillations, Modes of Oscillations, Mode Curve (Qualitative Analysis only). (Text 1: 9.1, 9.2.2)

Microwave Transmission Lines: Microwave Frequencies, Microwave devices, Microwave Systems, Transmission Line equations and solutions, Reflection Coefficient and Transmission Coefficient, Standing Wave and Standing Wave Ratio, Smith Chart, Single Stub matching. (Text 2: 0.1, 0.2, 0.3, 3.1, 3.2, 3.3, 3.5, 3.6 Except Double stub matching)

Module-2

Microwave Network theory: Symmetrical Z and Y-Parameters for Reciprocal Networks, S matrix representation of Multi-Port Networks. (Text 1: 6.1, 6.2, 6.3)

Microwave Passive Devices: Coaxial Connectors and Adapters, Attenuators, Phase Shifters, Waveguide Tees, Magic tees. (Text 1: 6.4.2, 6.4.14, 6.4.15, 6.4.16)

Module-3

Strip Lines: Introduction, Micro Strip lines, Parallel Strip lines, Coplanar Strip lines, Shielded Strip Lines. (Text 2: Chapter 11)

Antenna Basics: Introduction, Basic Antenna Parameters, Patterns, Beam Area, Radiation Intensity, Beam Efficiency, Directivity and Gain, Antenna Apertures, Effective Height, Bandwidth, Radio Communication Link, Antenna Field Zones & Polarization. (Text 3: 2.1- 2.11, 2.13,2.15)

Module-4

Point Sources and Arrays: Introduction, Point Sources, Power Patterns, Power Theorem, Radiation Intensity, Field Patterns, Phase Patterns, Arrays of Two Isotropic Point Sources, Pattern Multiplication, Linear Arrays of n Isotropic Point Sources of equal Amplitude and Spacing. (Text 3: 5.1 – 5.9, 5.11,5.13)

Electric Dipoles: Introduction, Short Electric Dipole, Fields of a Short Dipole (General and Far Field Analyses), Radiation Resistance of a Short Dipole, Thin Linear Antenna (Field Analyses), Radiation Resistances of Lambda/2 Antenna. (Text 3: 6.1 -6.6)

Module-5

Loop and Horn Antenna: Introduction, Small loop, Comparison of Far fields of Small Loop and Short Dipole, The Loop Antenna General Case , Far field Patterns of Circular Loop Antenna with Uniform Current , Radiation Resistance of Loops, Directivity of Circular Loop Antennas with Uniform Current, Horn antennas Rectangular Horn Antennas. (Text 3: 7.1-7.8, 7.19, 7.20)

Antenna Types: Helical Antenna, Helical Geometry, Practical Design Considerations of Helical Antenna, Yagi-Uda array, Parabola General Properties , Log Periodic Antenna. (Text 3: 8.3, 8.5, 8.8,11.7)

Question paper pattern:

- The question paper will have ten questions
- Each full question consists of 16marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module
- The students will have to answer 5 full questions, selecting one full question from each module

Text Book:

1. **Microwave Engineering** – Annapurna Das, Sisir K Das TMH Publication, 2nd, 2010.
2. **Microwave Devices and circuits**- Liao, Pearson Education.
3. **Antennas and Wave Propagation,** John D. Krauss, Ronald J Marhefka and Ahmad S Khan,4th Special Indian Edition , McGraw- Hill Education Pvt. Ltd., 2010.

Reference Books:

1. **Microwave Engineering** – David M Pozar, John Wiley India Pvt.Ltd. 3rd Edn, 2008.
2. **Microwave Engineering** – Sushrut Das, Oxford Higher Education, 2ndEdn, 2015.
3. **Antennas and Wave Propagation** – Harish and Sachidananda: Oxford University Press, 2007.

DIGITAL IMAGE PROCESSING

B.E., VII Semester, Electronics & Communication Engineering

[As per Choice Based Credit System (CBCS) scheme]

Subject Code	15EC72	IA Marks	20
Number of Lecture Hours/Week	04	Exam Marks	80
Total Number of Lecture Hours	50 (10 Hours / Module)	Exam Hours	03

CREDITS – 04

Modules

Module-1

Digital Image Fundamentals: What is Digital Image Processing, Origins of Digital Image Processing, Examples of fields that use DIP, Fundamental Steps in Digital Image Processing, Components of an Image Processing System. Elements of Visual Perception, Image Sensing and Acquisition, Image Sampling and Quantization, Some Basic Relationships Between Pixels, Linear and Nonlinear Operations.

[Text: Chapter 1 and Chapter 2: Sections 2.1 to 2.5, 2.6.2]

Module-2

Spatial Domain: Some Basic Intensity Transformation Functions, Histogram Processing, Fundamentals of Spatial Filtering, Smoothing Spatial Filters, Sharpening Spatial Filters

Frequency Domain: Preliminary Concepts, The Discrete Fourier Transform (DFT) of Two Variables, Properties of the 2-D DFT, Filtering in the Frequency Domain, Image Smoothing and Image Sharpening Using Frequency Domain Filters, Selective Filtering.

[Text: Chapter 3: Sections 3.2 to 3.6 and Chapter 4: Sections 4.2, 4.5 to 4.10]

Module-3

Restoration: Noise models, Restoration in the Presence of Noise Only using Spatial Filtering and Frequency Domain Filtering, Linear, Position-Invariant Degradations, Estimating the Degradation Function, Inverse Filtering, Minimum Mean Square Error (Wiener) Filtering, Constrained Least Squares Filtering.

[Text: Chapter 5: Sections 5.2, to 5.9]

Module-4

Color Image Processing: Color Fundamentals, Color Models, Pseudocolor Image Processing.

Wavelets: Background, Multiresolution Expansions.

Morphological Image Processing: Preliminaries, Erosion and Dilation, Opening and Closing, The Hit-or-Miss Transforms, Some Basic Morphological Algorithms.

[Text: Chapter 6: Sections 6.1 to 6.3, Chapter 7: Sections 7.1 and 7.2, Chapter 9: Sections 9.1 to 9.5]

Module-5

Segmentation: Point, Line, and Edge Detection, Thresholding, Region-Based Segmentation, Segmentation Using Morphological Watersheds.
Representation and Description: Representation, Boundary descriptors.
[Text: Chapter 10: Sections 10.2, to 10.5 and Chapter 11: Sections 11.1 and 11.2]

Question paper pattern:
The question paper will have ten questions.

- Each full question consists of 16 marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module. The students will have to answer 5 full questions, selecting one full question from each module.

Text Books:

1. **Digital Image Processing** - Rafel C Gonzalez and Richard E. Woods, PHI 3rd Edition 2010.

Reference Books:

1. **Digital Image Procesing** - S.Jayaraman, S.Esakkirajan, T.Veerakumar, TataMcGraw Hill 2014.
2. **Fundamentals of Digital Image Processing**-A. K. Jain, Pearson 2004.

POWER ELECTRONICS

B.E., VII Semester, Electronics & Communication Engineering

[As per Choice Based Credit System (CBCS) scheme]

Subject Code	15EC73	IA Marks	20
Number of Lecture Hours/Week	04	Exam Marks	80
Total Number of Lecture	50 (10 Hours / Module)	Exam Hours	03
CREDITS – 04			

Modules

Module-1

Introduction - Applications of Power Electronics, Power Semiconductor Devices, Control Characteristics of Power Devices, types of Power Electronic Circuits, Peripheral Effects.
Power Transistors: Power BJTs: Steady state characteristics. Power MOSFETs: device operation, switching characteristics, IGBTs: device operation, output and transfer characteristics, di/dt and dv/dt limitations.
(Text 1)

Module-2

Thyristors - Introduction, Principle of Operation of SCR, Static Anode-Cathode Characteristics of SCR, Two transisitor model of SCR, Gate Characteristics of SCR, Turn-ON Methods, Turn-OFF Mechanism, Turn-OFF Methods: Natural and Forced Commutation – Class A and Class B types, Gate Trigger Circuit: Resistance Firing Circuit, Resistance capacitance firing circuit, UJT Firing Circuit.
(Text 2)

Module-3

Controlled rectifiers - Introduction, Principle of phase controlled converter operation, Single phase full converters, Single phase dual converters. Single phase semi-converter with RL load.
AC Voltage Controllers - Introduction, Principles of ON-OFF Control, Principle of Phase Control, Single phase control with resistive and inductive loads.
(Text 1)

Module-4

DC-DC Converters - Introduction, principle of step-down operation and it's analysis with RL load, principle of step-up operation, Step-up converter with a resistive load, Performance parameters, Converter classification, Switching mode regulators: Buck regulator, Boost regulator, Buck-Boost Regulators, Chopper circuit design.
(Text 1)

Module-5

Pulse Width Modulated Inverters- Introduction, principle of operation, performance parameters, Single phase bridge inverters, voltage control of single phase inverters, current source inverters, Variable DC-link inverter, Boost inverter, Inverter circuit design.
Static Switches: Introduction, Single phase AC switches, DC Switches, Solid state relays, Microelectronic relays.
(Text 1)

Evaluation of Internal Assessment Marks:

It is suggested that at least 4 experiments of Power Electronics to be conducted by the students. This activity can be considered for the evaluation of 5 marks out of 20 Internal assessment marks, reserved for the other activities.

Question paper pattern:

- The question paper will have ten questions
- Each full question consists of 16 marks**.**
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module
- The students will have to answer 5 full questions, selecting one full question from each module

Text Book:

1. Mohammad H Rashid ,Power Electronics, Circuits, Devices and Applications, ,3rd Edition, Pearson Education Inc,2014, ISBN: 978-93-325-1844-5.
2. M.D Singh and K B Khanchandani, Power Electronics, 2nd Edition, Tata Mc-Graw Hill, 2009, ISBN: 0070583897

Reference Books:

1. L. Umanand, Power Electronics, Essentials and Applications, John Wiley India Pvt. Ltd, 2009.
2. Dr. P. S. Bimbhra, “Power Electronics”, Khanna Publishers, Delhi., 2012.
3. P.C. Sen, “Modern Power Electronics”, S Chand & Co New Delhi, 2005.
4. Earl Gose, Richard Johnsonbaugh, Steve Jost, Pattern Recognition And Image Analysis, ePub eBook.

MULTIMEDIA COMMUNICATION

B.E., VII Semester, Electronics & Communication Engineering/ Telecommunication Engineering

[As per Choice Based credit System (CBCS) Scheme

Subject Code	15EC741	IA Marks	20
Number of Lecture Hours/Week	03	Exam Marks	80
Total Number of Lecture Hours	40 (08 Hours / Module)	Exam Hours	03
CREDITS – 03			

Course objectives:

- Gain fundamental knowledge in understanding the basics of different multimedia networks and applications.
- Enable students with digitization principle techniques required to analyze different media types.
- Analyze compression techniques required to compress text and image and gain knowledge of DMS.
- Enable students to analyze compression techniques required to compress audio and video.
- Gain fundamental knowledge about multimedia communication across different networks.

Modules

Module-1

Multimedia Communications: Introduction, Multimedia information representation, multimedia networks, multimedia applications, Application and networking terminology. (Chap 1 of Text 1)

Module-2

Information Representation: Introduction , Digitization principles, Text, Images, Audio and Video (Chap 2 of Text 1)

Module-3

Text and image compression: Introduction, Compression principles, text compression, image Compression. (Chap 3 of Text 1)

Distributed multimedia systems: Introduction, main Features of a DMS, Resource management of DMS, Networking, Multimedia operating systems (Chap. 4 - Sections 4.1 to 4.5 of Text 2).

Module-4

Audio and video compression: Introduction, Audio compression, video compression, video compression principles, video compression. (Chap. 4 of Text 1).

Module-5

Multimedia Communication Across Networks: Packet audio/video in the network environment, Video transport across generic networks, Multimedia Transport across ATM Networks.(Chap. 6 - Sections 6.1, 6.2, 6.3 of Text 2)

Course Outcomes: After studying this course, students will be able to:

- Understand basics of different multimedia networks and applications.
- Analyse different media types to represent them in digital form.
- Compress different types of text and images using different compression techniques and analyse DMS.
- Understand different compression techniques to compress audio and video.
- Describe multimedia Communication Across Networks

Graduate Attributes (as per NBA):

- Engineering Knowledge.
- Problem Analysis.
- Design / development of solutions (partly).
- Interpretation of data.

Question paper pattern:

The question paper will have ten questions.

- Each full question consists of 16marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module. The students will have to answer 5 full questions, selecting one full question from each module.

Text Books:

1. Fred Halsall, "Multimedia Communications", Pearson education, 2001 ISBN - 9788131709948.

2. K. R. Rao, Zoran S. Bojkovic, Dragorad A. Milovanovic, "Multimedia Communication Systems", Pearson education, 2004. ISBN -9788120321458

Reference Books:

1. Raif steinmetz, Klara Nahrstedt, "Multimedia: Computing, Communications and Applications", Pearson education, 2002. ISBN -9788177584417

BIOMEDICAL SIGNAL PROCESSING

B.E., VII Semester, Electronics & Communication Engineering/ Telecommunication Engineering

[As per Choice Based Credit System (CBCS) scheme]

Subject Code	15EC742	IA Marks	20
Number of Lecture Hours/Week	03	Exam Marks	80
Total Number of Lecture Hours	40 (8 Hours / Module)	Exam Hours	03
CREDITS – 03			

Modules

Module-1

Introduction to Biomedical Signals: The nature of Biomedical Signals, Examples of Biomedical Signals, Objectives and difficulties in Biomedical analysis.

Electrocardiography: Basic electrocardiography, ECG lead systems, ECG signal characteristics.

Signal Conversion :Simple signal conversion systems, Conversion requirements for biomedical signals, Signal conversion circuits (Text-1)

Module-2

Signal Averaging: Basics of signal averaging, signal averaging as a digital filter, a typical averager, software for signal averaging, limitations of signal averaging.

Adaptive Noise Cancelling: Principal noise canceller model, 60-Hzadaptive cancelling using a sine wave model, other applications of adaptive filtering. (Text-1)

Module-3

Data Compression Techniques: Turning point algorithm, AZTEC algorithm, Fan algorithm, Huffman coding, data reduction algorithms The Fourier transform, Correlation, Convolution, Power spectrum estimation, Frequency domain analysis of the ECG (Text-1)

Module-4

Cardiological signal processing:

Basic Electrocardiography, ECG data acquisition, ECG lead system, ECG signal characteristics (parameters and their estimation), Analog filters, ECG amplifier, and QRS detector, Power spectrum of the ECG, Band pass filtering techniques, Differentiation techniques, Template matching techniques, A QRS detection algorithm, Realtime ECG processing algorithm, ECG interpretation, ST segment analyzer, Portable arrhythmia monitor. (Text -2)

Module-5

Neurological signal processing: The brain and its potentials, The electrophysiological origin of brain waves, The EEG signal and its characteristics (EEG rhythms, waves, and transients), Correlation.

Analysis of EEG channels: Detection of EEG rhythms, Template matching for EEG, spike and wave detection (Text-2).

Question paper pattern:

The question paper will have ten questions.

- Each full question consists of 16marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module. The students will have to answer 5 full questions, selecting one full question from each module.

Text Books:

1. **Biomedical Digital Signal Processing-** Willis J. Tompkins, PHI 2001.
2. **Biomedical Signal Processing Principles and Techniques-** D C Reddy, McGraw-Hill publications 2005

Reference Book:

1. **Biomedical Signal Analysis-**Rangaraj M. Rangayyan,John Wiley & Sons 2002

REAL TIME SYSTEMS

B.E., VII Semester, Electronics & Communication Engineering /Telecommunication Engineering

[As per Choice Based Credit System (CBCS) scheme]

Subject Code	15EC743	IA Marks	20
Number of Lecture Hours/Week	03	Exam Marks	80
Total Number of Lecture Hours	40 (8 Hours / Module)	Exam Hours	03

CREDITS – 03

Modules

Module-1

INTRODUCTION TO REAL-TIME SYSTEMS: Historical background, Elements of a Computer Control System, RTS- Definition, Classification of Real-time Systems, Time Constraints, Classification of Programs.

CONCEPTS OF COMPUTER CONTROL: Introduction, Sequence Control, Loop Control, Supervisory Control, Centralized Computer Control, Hierarchical Systems. (Text Book: 1.1 to 1.6 and 2.1 to 2.6)

Module-2

COMPUTER HARDWARE REQUIREMENTS FOR REAL-TIME APPLICATIONS: Introduction, General Purpose Computer, Single Chip Microcomputers and Microcontrollers, Specialized Processors, Process-Related Interfaces, Data Transfer Techniques, Communications, Standard Interface.(Text Book: 3.1 to 3.8)

Module-3

LANGUAGES FOR REAL-TIME APPLICATIONS: Introduction, Syntax Layout and Readability, Declaration and Initialization of Variables and Constants, Modularity and Variables, Compilation of Modular Programs, Data types, Control Structures, Exception Handling, Low-level facilities, Co-routines, Interrupts and Device Handling, Concurrency, Real-Time Support, Overview of Real-Time Languages. (Text Book: 5.1 to 5.14)

Module-4

OPERATING SYSTEMS: Introduction, Real-Time Multi-Tasking OS, Scheduling Strategies, Priority Structures, Task Management, Scheduler and Real-Time Clock Interrupt Handler, Memory Management, Code Sharing, Resource Control, Task Co-Operation and Communication, Mutual Exclusion. (Text Book: 6.1 to 6.11)

Module-5

DESIGN OF RTS – GENERAL INTRODUCTION: Introduction, Specification Document, Preliminary Design, Single-Program Approach, Foreground/Background System.

RTS DEVELOPMENT METHODOLOGIES: Introduction, Yourdon Methodology, Ward and Mellor Method, Hately and Pirbhai Method. (Text Book: 7.1 to 7.5 and 8.1, 8.2, 8.4,8.5)

Question paper pattern:

The question paper will have ten questions.

- Each full question consists of 16marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module. The students will have to answer 5 full questions, selecting one full question from each module.

Text Book:

Real-Time Computer Control, Stuart Bennet, 2nd Edn. Pearson Education. 2008.

Reference Books:

1. Real –Time Systems C.M. Krishna, Kang G. Shin,", McGraw –Hill International Editions, 1997.
2. Real-Time Systems Design and Analysis, Phillip. A. Laplante, PHI, Second edition, 2005.
3. Embedded Systems, Raj Kamal, Tata McGraw Hill, India, third edition, 2005.

Cryptography

B.E., VII Semester, Electronics & Communication Engineering

[As per Choice Based Credit System (CBCS) scheme]

Subject Code	15EC744	IA Marks	20
Number of Lecture Hours/Week	03	Exam Marks	80
Total Number of Lecture Hours	40 (08 Hours / Module)	Exam Hours	03
CREDITS – 03			

Course Objectives:

1. To enable students to understand the basics of symmetric key and public key cryptography.
2. To equip students with some basic mathematical concepts and pseudorandom number generators required for cryptography.
3. To enable students to authenticate and protect the encrypted data
4. To enrich knowledge about Email, IP and Web security

Modules

Module-1

Basic Concepts of Number Theory and Finite Fields: Divisibility and the divisibility algorithm, Euclidean algorithm, Modular arithmetic, Groups, Rings and Fields, Finite fields of the form GF(p), Polynomial arithmetic, Finite fields of the form GF(2^n) (Text 1: Chapter 3)

Module-2

Classical Encryption Techniques: Symmetric cipher model, Substitution techniques, Transposition techniques, Steganography (Text 1: Chapter 1)

SYMMETRIC CIPHERS: Traditional Block Cipher structure, Data encryption standard (DES) (Text 1: Chapter 2: Section1, 2)

Module-3

SYMMETRIC CIPHERS: The AES Cipher. (Text 1: Chapter 4: Section 2, 3, 4)

Pseudo-Random-Sequence Generators and Stream Ciphers: Linear Congruential Generators, Linear Feedback Shift Registers, Design and analysis of stream ciphers, Stream ciphers using LFSRs (Text 2: Chapter 16: Section 1, 2, 3, 4)

Module-4

More number theory: Prime Numbers, Fermat's and Euler's theorem, Primality testing, Chinese Remainder theorem, discrete logarithm. (Text 1: Chapter 7)

Principles of Public-Key Cryptosystems: The RSA algorithm, Diffie - Hellman Key Exchange, Elliptic Curve Arithmetic, Elliptic Curve Cryptography (Text 1: Chapter 8, Chapter 9: Section 1, 3, 4)

Module-5

One-Way Hash Functions: Background, Snefru, N-Hash, MD4, MD5, Secure Hash Algorithm [SHA],One way hash functions using symmetric block algorithms, Using public key algorithms, Choosing a one-way hash functions, Message Authentication Codes. Digital Signature Algorithm, Discrete Logarithm Signature Scheme (Text 2: Chapter 18: Section 18.1 to 18.5, 18.7, 18.11 to 18.14 and Chapter 20: Section 20.1, 20.4)

Course Outcomes: After studying this course, students will be able to:

1. Use basic cryptographic algorithms to encrypt the data.
2. Generate some pseudorandom numbers required for cryptographic applications.
3. Provide authentication and protection for encrypted data.

Question paper pattern:

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Books:

1. William Stallings , "Cryptography and Network Security Principles and Practice", Pearson Education Inc., 6th Edition, 2014, ISBN: 978-93-325-1877-3
2. Bruce Schneier, "Applied Cryptography Protocols, Algorithms, and Source code in C", Wiley Publications, 2nd Edition, ISBN: 9971-51-348-X

Reference Books:

1. Cryptography and Network Security, Behrouz A. Forouzan, TMH, 2007.
2. Cryptography and Network Security, Atul Kahate, TMH, 2003.

CAD for VLSI

B.E., VII Semester, Electronics & Communication Engineering

[As per Choice Based Credit System (CBCS) scheme]

Subject Code	15EC745	IA Marks	20
Number of Lecture Hours/Week	03	Exam marks	80
Total Number of Lecture Hours	40 (8 Hours per Module)	Exam Hours	03
CREDITS – 03			

Course Objectives: This course will enable students to:

- Understand various stages of Physical design of VLSI circuits
- Know about mapping a design problem to a realizable algorithm
- Become aware of graph theoretic, heuristic and genetic algorithms
- Compare performance of different algorithms in terms of a cost function
- Design their own algorithms to suit specific requirements

Modules

Module-1

Data Structures and Basic Algorithms:

Basic terminology, Complexity issues and NP-Hardness. Examples - Exponential, heuristic, approximation and special cases. Basic Algorithms. Graph Algorithms for Search, spanning tree, shortest path, min-cut and max-cut, Steiner tree. Computational Geometry Algorithms: Line sweep and extended line sweep methods.

Basic Data Structures: Atomic operations for layout editors, Linked list of blocks, Bin-based method, Neighbor pointers, corner-stitching, Multi-layer operations, Limitations of existing data structures. Layout specification languages.

Graph algorithms for physical design: Classes of graphs in physical design, Relationship between graph classes, Graph problems in physical design,

Algorithms for Interval graphs, permutation graphs and circle graphs.

Module-2

Partitioning: Problem formulation, Design style specific partitioning problems, Classification of Partitioning Algorithms.

Group migration algorithms: Kernighan-Lin algorithm, Fiduccia-Mattheyses Algorithm, Goldberg- Burstein algorithm, Component replication and ratio-cut. Simulated Annealing, Simulated Evolution, performance driven partitioning.

Floor Planning: Problem formulation, Constraint based floor planning, Integer Programming based floor planning, Rectangular dualization, Simulated evolution algorithms

Pin Assignment: Problem formulation. Classification of pin assignment problems, General pin assignment problem.

Module-3

Placement: Problem formulation, Classification of placement algorithms. Simulation based placement: Simulated annealing, simulated evolution, force directed placement. Partitioning based algorithms: Breur's Algorithm, Terminal propagation algorithm. Other algorithms for placement.

Global Routing: Problem formulation, Classification of Global routing algorithms, Maze routing algorithms: Lee's algorithm, Soukup's algorithm and Hadlock's Algorithm, Line probe algorithms, shortest path based algorithms, Separability based algorithm, non-rectilinear steiner tree based algorithm.

Module-4

Detailed Routing: Problem formulation, Routing considerations, models, channel routing and switch box routing problems. General river routing problem, Single row routing problem.

Two-layer channel routing algorithms: Basic Left Edge Algorithm, Dogleg router, Symbolic router-YACR2.

Net merge channel router, Gridless channel router.

Three layer channel routing: Extended net merge channel router.

Switchbox routing algorithms: Greedy router, Rip-and-reroute based router.

Module 5

Over-the-cell Routing and via minimization: Cell models, Two layer OTC routers, Basic OTC routing algorithm, Planar OTC routing, OTC routing using vacant terminals. Three layer OTC routing. Via minimization, constrained via minimization. Graph representation of two layer CVM problem,

Clock and Power Routing: Clocking Schemes, Delay calculation for clock trees, Design specific problems. H-Tree based algorithm, MMM Algorithm, Geometric matching algorithm, Weighted center and Exact Zero skew algorithms, Multiple clock routing.

Question paper pattern:

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Book:

Algorithms for VLSI Physical Design Automation, 3rd Ed, Naveed Sherwani, 1999, Kluwer Academic Publishers, Reprint 2009 Springer (India) Private Ltd. ISBN 978-81-8128-317-7

DSP Algorithms and Architecture

B.E., VII Semester, Electronics & Communication Engineering /Telecommunication Engineering

[As per Choice Based Credit System (CBCS) scheme]

Subject Code	15EC751	IA Marks	20
Number of Lecture Hours/Week	03	Exam Marks	80
Total Number of Lecture Hours	40 (8 Hours / Module)	Exam Hours	03
CREDITS – 03			

Modules

Module-1

Introduction to Digital Signal Processing:
Introduction, A Digital Signal – Processing System, The Sampling Process, Discrete Time Sequences, Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear Time-Invariant Systems, Digital Filters, Decimation and Interpolation.

Computational Accuracy in DSP Implementations:
Number Formats for Signals and Coefficients in DSP Systems, Dynamic Range and Precision, Sources of Error in DSP Implementation.

Module-2

Architectures for Programmable Digital Signal – Processing Devices:
Introduction, Basic Architectural Features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Unit, Programmability and Program Execution, Speed Issues, Features for External Interfacing.

Module-3

Programmable Digital Signal Processors:
Introduction, Commercial Digital Signal-processing Devices, Data Addressing Modes of TMS32OC54XX, Memory Space of TMS32OC54xx Processors, Program Control. Detail Study of TMS320C54X & 54xx Instructions and Programming, On – Chip Peripherals, Interrupts of TMS32OC54XX Processors, Pipeline Operation of TMS32OC54xx Processor.

Module-4

Implementation of Basic DSP Algorithms:
Introduction, The Q – notation, FIR Filters, IIR Filters, Interpolation and Decimation Filters (one example in each case).

Implementation of FFT Algorithms:
Introduction, An FFT Algorithm for DFT Computation, Overflow and Scaling, Bit – Reversed Index. Generation & Implementation on the TMS32OC54xx.

Module-5

Interfacing Memory and Parallel I/O Peripherals to Programmable DSP Devices:
Introduction, Memory Space Organization, External Bus Interfacing Signals. Memory Interface, Parallel I/O Interface, Programmed I/O, Interrupts and I/O Direct Memory Access (DMA).

Interfacing and Applications of DSP Processors:
Introduction, Synchronous Serial Interface, A CODEC Interface Circuit, DSP Based Bio-telemetry Receiver, A Speech Processing System, An Image Processing System.

Question paper pattern:

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Book:

"Digital Signal Processing", Avatar Singh and S. Srinivasan, Thomson Learning, 2004.

Reference Books:

1. "Digital Signal Processing: A practical approach", Ifeachor E. C., Jervis B. W Pearson-Education, PHI, 2002.
2. "Digital Signal Processors", B Venkataramani and M Bhaskar, TMH, 2nd, 2010
3. "Architectures for Digital Signal Processing", Peter Pirsch John Weily, 2008

IoT & WIRELESS SENSOR NETWORKS

B.E., VII Semester, Electronics & Communication Engineering /Telecommunication Engineering

[As per Choice Based Credit System (CBCS) scheme]

Subject Code	15EC752	IA Marks	20
Number of Lecture Hours/Week	03	Exam Marks	80
Total Number of Lecture Hours	40 (8 Hours / Module)	Exam Hours	03
CREDITS – 03			

Modules

Module-1

Overview of Internet of Things: IoT Conceptual Framework, IoT Architectural View, Technology Behind IoT, Sources of IoT ,M2M communication, Examples of IoT. Modified OSI Model for the IoT/M2M Systems, data enrichment ,data consolidation and device management at IoT/M2M Gateway, web communication protocols used by connected IoT/M2M devices, Message communication protocols (CoAP-SMS , CoAP-MQ, MQTT ,XMPP) for IoT/M2M devices.

Module-2

Architecture and Design principles for IoT: Internet connectivity, Internet-based communication, IPv4, IPv6,6LoWPAN protocol, IP Addressing in the IoT, Application layer protocols: HTTP, HTTPS,FTP,TELNET and ports.

Data Collection, Storage and Computing using a Cloud Platform: Introduction, Cloud computing paradigm for data collection , storage and computing, Cloud service models, IoT Cloud- based data collection, storage and computing services using Nimbits.

Module-3

Prototyping and Designing The software for IoT Applications: Introduction, Prototyping Embedded device software, Programming Embedded Device Arduino Platform using IDE, Reading data from sensors and devices, Devices, Gateways, Internet and Web/Cloud services software development.

Programming MQTT clients and MQTT server. Introduction to IoT privacy and security. Vulnerabilities, security requirements and threat analysis, IoT Security Tomography and layered attacker model.

Module-4

OVERVIEW OF WIRELESS SENSOR NETWORKS

Challenges for Wireless Sensor Networks, Enabling Technologies for Wireless Sensor Networks.

ARCHITECTURES: Single-Node Architecture - Hardware Components, Energy Consumption of Sensor Nodes , Operating Systems and Execution Environments, Network Architecture -Sensor Network Scenarios, Optimization Goals and Figures of Merit, Design principles for WSNs, Service interfaces of WSNs Gateway Concepts.

Module-5

Communication Protocols

Physical Layer and Transceiver Design Considerations, MAC Protocols for Wireless Sensor Networks, Low Duty Cycle Protocols And Wakeup Concepts - S-MAC , The Mediation Device Protocol, Wakeup Radio Concepts, Contention based protocols(CSMA,PAMAS), Schedule based protocols (LEACH, SMACS, TRAMA) Address and Name Management in WSNs, Assignment of MAC Addresses, Routing Protocols-Energy-Efficient Routing, Geographic Routing, Hierarchical networks by clustering.

Question paper pattern:

- The question paper will have ten questions.
- Each full Question consisting of 16marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.
- The students will have to answer 5 full questions, selecting one full question from each module.

Graduating Attributes (as per NBA)

- Engineering Knowledge
- Problem Analysis
- Design / development of solutions (partly)

TEXT BOOKS:

1. Raj Kamal, ”Internet of Things-Architecture and design principles”, McGraw Hill Education.
2. Holger Karl & Andreas Willig, "Protocols And Architectures for Wireless Sensor Networks" , John Wiley, 2005.
3. Feng Zhao & Leonidas J. Guibas, “Wireless Sensor Networks- An Information Processing Approach", Elsevier, 2007.

REFERENCES:

1. Kazem Sohraby, Daniel Minoli, & Taieb Znati, “Wireless Sensor Networks-Technology, Protocols, And Applications”, John Wiley, 2007.
2. Anna Hac, “Wireless Sensor Network Designs”, John Wiley, 2003.

PATTERN RECOGNITION

B.E., VII Semester, Electronics & Communication Engineering/ Telecommunication Engineering

[As per Choice Based Credit System (CBCS) scheme]

Subject Code	15EC753	IA Marks	20
Number of Lecture Hours/Week	03	Exam Marks	80
Total Number of Lecture Hours	40 (8 Hours / Module)	Exam Hours	03
CREDITS – 03			

Modules

Module-1

Introduction: Importance of pattern recognition, Features, Feature Vectors, and Classifiers, Supervised, Unsupervised, and Semi-supervised learning, Introduction to Bayes Decision Theory, Discriminant Functions and Decision Surfaces, Gaussian PDF and Bayesian Classification for Normal Distributions.

Module-2

Data Transformation and Dimensionality Reduction: Introduction, Basis Vectors, The KarhunenLoeve(KL) Transformation, Singular Value Decomposition, Independent Component Analysis (Introduction only). Nonlinear Dimensionality Reduction, Kernel PCA.

Module-3

Estimation of Unknown Probability Density Functions: Maximum Likelihood Parameter Estimation, Maximum a Posteriori Probability estimation, Bayesian Interference, Maximum Entropy Estimation, Mixture Models, Naive-Bayes Classifier, The Nearest Neighbor Rule.

Module-4

Linear Classifiers: Introduction, Linear Discriminant Functions and Decision Hyperplanes, The Perceptron Algorithm, Mean Square Error Estimate, Stochastic Approximation of LMS Algorithm, Sum of Error Estimate.

Module-5

Nonlinear Classifiers: The XOR Problem, The two Layer Perceptron, Three Layer Perceptron, Back propagation Algorithm, Basic Concepts of Clustering, Introduction to Clustering , Proximity Measures.

Question paper pattern:

The question paper will have ten questions.

- Each full question consists of 16marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module. The students will have to answer 5 full questions, selecting one full question from each module.

Text Book:

Pattern Recognition: Sergios Theodoridis, Konstantinos Koutroumbas, Elsevier India Pvt.Ltd (Paper Back), 4th edition.

Reference Books:

1. **The Elements Of Statistical Learning:** Trevor Hastie, Springer-Verlag New York, LLC (Paper Back), 2009.
2. **Pattern Classification:** Richard O. Duda, Peter E. Hart, David G. Stork.
1. John Wiley & Sons, 2012.
3. Earl Gose, Richard Johnsonbaugh, Steve Jost, Pattern Recognition And Image Analysis, ePub eBook.

ADVANCED COMPUTER ARCHITECTURE

B.E., VII Semester, Electronics & Communication Engineering /Telecommunication Engineering

[As per Choice Based Credit System (CBCS) scheme]

Subject Code	15EC754	IA Marks	20
Number of Lecture Hours/Week	03	Exam Marks	80
Total Number of Lecture Hours	40 (8 Hours / Module)	Exam Hours	03

CREDITS – 03

Modules

Module-1

Parallel Computer Models: The state of computing, Classification of parallel computers, Multiprocessors and multicomputer, Multivectors and SIMD computers.

Program and Network Properties: Conditions of parallelism, Data and resource Dependences, Hardware and software parallelism, Program partitioning and scheduling, Grain Size and latency.

Module-2

Program flow mechanisms: Control flow versus data flow, Data flow Architecture, Demand driven mechanisms, Comparisons of flow mechanisms.

Principles of Scalable Performance: Performance Metrics and Measures, Parallel Processing Applications, Speedup Performance Laws, Scalability Analysis and Approaches.

Module-3

Speedup Performance Laws: Amdhal's law, Gustafson's law, Memory bounded speed up model, Scalability Analysis and Approaches.

Advanced Processors: Advanced processor technology, Instruction-set Architectures, CISC Scalar Processors, RISC Scalar Processors, Superscalar Processors, VLIW Architectures.

Module-4

Pipelining: Linear pipeline processor, nonlinear pipeline processor, Instruction pipeline Design, Mechanisms for instruction pipelining, Dynamic instruction scheduling, Branch Handling techniques, branch prediction, Arithmetic Pipeline Design

Memory Hierarchy Design: Cache basics & cache performance, reducing miss rate and miss penalty, multilevel cache hierarchies, main memory organizations, design of memory hierarchies.

Module-5

Multiprocessor Architectures: Symmetric shared memory architectures, distributed shared memory architectures, models of memory consistency, cache coherence protocols (MSI, MESI, MOESI), scalable cache coherence, overview of directory based approaches, design challenges of directory protocols, memory based directory protocols, cache based directory protocols.

Question paper pattern:

The question paper will have ten questions.

- Each full question consists of 16 marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module. The students will have to answer 5 full questions, selecting one full question from each module.

Text Books:

1. Kai Hwang, “Advanced computer architecture”; TMH.

Reference Books:

1. Kai Hwang and Zu, “Scalable Parallel Computers Architecture”; MGH.
2. M.J Flynn, “Computer Architecture, Pipelined and Parallel Processor Design”; Narosa Publishing.
3. D.A.Patterson, J.L.Hennessy, “Computer Architecture :A quantitative approach”; Morgan Kauffmann feb,2002.

SATELLITE COMMUNICATION

B.E., VII Semester, Electronics & Communication Engineering

[As per Choice Based Credit System (CBCS)]

Subject Code	15EC755	IA Marks	20
Number of Lecture Hours/Week	03	Exam Marks	80
Total Number of Lecture Hours	40 (8 Hours / Module)	Exam Hours	03
CREDITS – 03			

Modules

Module-1

Satellite Orbits and Trajectories: Definition, Basic Principles, Orbital parameters, Injection velocity and satellite trajectory, Types of Satellite orbits, Orbital perturbations, Satellite stabilization, Orbital effects on satellite's performance, Eclipses, Look angles: Azimuth angle, Elevation angle.

Module-2

Satellite subsystem: Power supply subsystem, Attitude and Orbit control, Tracking, Telemetry and command subsystem, Payload.

Earth Station: Types of earth station, Architecture, Design considerations, Testing, Earth station Hardware, Satellite tracking.

Module-3

Multiple Access Techniques: Introduction, FDMA (No derivation), SCPC Systems, MCPC Systems, TDMA, CDMA, SDMA.

Satellite Link Design Fundamentals: Transmission Equation, Satellite Link Parameters, Propagation considerations.

Module-4

Communication Satellites: Introduction, Related Applications, Frequency Bands, Payloads, Satellite Vs. Terrestrial Networks, Satellite Telephony, Satellite Television, Satellite radio, Regional satellite Systems, National Satellite Systems.

Module-5

Remote Sensing Satellites: Classification of remote sensing systems, orbits, Payloads, Types of images: Image Classification, Interpretation, Applications.

Weather Forecasting Satellites: Fundamentals, Images, Orbits, Payloads, Applications.

Navigation Satellites: Development of Satellite Navigation Systems, GPS system, Applications.

Graduating Attributes (as per NBA)

- Engineering Knowledge
- Problem Analysis
- Design / Development of solutions

Question Paper pattern:

- The Question paper will have ten questions.
- Each full Question consisting of 16marks
- There will be 2 full Questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.
- The Students will have to answer 5 full Questions, selecting one full Question from each module.

Text Book:

3. Anil K. Maini, Varsha Agrawal, Satellite Communications, Wiley India Pvt. Ltd., 2015, ISBN: 978-81-265-2071-8.

Reference Books :

1. Dennis Roddy, Satellite Communications, 4th Edition, McGraw- Hill International edition, 2006
2. Timothy Pratt, Charles Bostian, Jeremy Allnutt, Satellite Communications, 2nd Edition, Wiley India Pvt. Ltd , 2017, ISBN: 978-81-265-0833-4

ADVANCED COMMUNICATION LAB

B.E., VII Semester, Electronics & Communication Engineering

[As per Choice Based Credit System (CBCS) scheme]

Subject Code	15ECL767	IA Marks	20
Number of Lecture Hours/Week	01Hr Tutorial (Instructions) + 02 Hours Laboratory = 03	Exam Marks	80
		Exam Hours	03
CREDITS – 02			

Course objectives: This course will enable students to:

- Design and demonstrate the digital modulation techniques
- Demonstrate and measure the wave propagation in microstrip antennas
- Characteristics of microstrip devices and measurement of its parameters.
- Model an optical communication system and study its characteristics.
- Simulate the digital communication concepts and compute and display various parameters along with plots/figures.

Laboratory Experiments

PART-A: Following Experiments No. 1 to 4 has to be performed using discrete components.

1. Time Division Multiplexing and Demultiplexing of two band limited signals.
2. ASK generation and detection
3. FSK generation and detection
4. PSK generation and detection
5. Measurement of frequency, guide wavelength, power, VSWR and attenuation in microwave test bench.
6. Measurement of directivity and gain of microstrip dipole and Yagi antennas.
7. Determination of
    a. Coupling and isolation characteristics of microstrip directional coupler.
    b. Resonance characteristics of microstrip ring resonator and computation of dielectric constant of the substrate.
    c. Power division and isolation of microstrip power divider.
8. Measurement of propagation loss, bending loss and numerical aperture of an optical fiber.

PART-B: Simulation Experiments using SCILAB/MATLAB/Simulink or LabView

1. Simulate NRZ, RZ, half-sinusoid and raised cosine pulses and generate eye diagram for binary polar signaling.
2. Simulate the Pulse code modulation and demodulation system and display the waveforms.
3. Simulate the QPSK transmitter and receiver. Plot the signals and its constellation

diagram.

4. Test the performance of a binary differential phase shift keying system by simulating the non-coherent detection of binary DPSK.

Conduct of Practical Examination:

- All laboratory experiments are to be considered for practical examination.
- For examination one question from **PART-A** and one question from **PART-B or** only one question from **PART-B** experiments based on the complexity, to be set.
- Students are allowed to pick one experiment from the lot.
- Strictly follow the instructions as printed on the cover page of answer script for breakup of marks.
- Change of experiment is allowed only once and Marks allotted to the procedure part to be made zero.

VLSI LAB

B.E., VII Semester, Electronics & Communication Engineering

[As per Choice Based Credit System (CBCS) scheme]

Subject Code	15ECL77	IA Marks	20
Number of Lecture Hours/Week	01Hr Tutorial (Instructions) + 02 Hours Laboratory = 03	Exam Marks	80
		Exam Hours	03

CREDITS – 02

Experiments can be conducted using any of the following or equivalent design tools: Cadence/Synopsis/Mentor Graphics/Microwind

Laboratory Experiments

PART - A
ASIC-DIGITAL DESIGN

1. Write Verilog Code for the following circuits and their Test Bench for verification, observe the waveform and synthesize the code with technological library with given constraints*. Do the initial timing verification with gate level simulation.
   i. An inverter
   ii. A Buffer
   iii. Transmission Gate
   iv. Basic/universal gates
   v. Flip flop -RS, D, JK, MS, T
   vi. Serial & Parallel adder
   vii. 4-bit counter [Synchronous and Asynchronous counter]
   viii. Successive approximation register [SAR]

PART - B
ANALOG DESIGN

1. Design an Inverter with given specifications**, completing the design flow mentioned below:
   a. Draw the schematic and verify the following
      i) DC Analysis
      ii) Transient Analysis
   b. Draw the Layout and verify the DRC, ERC
   c. Check for LVS
   d. Extract RC and back annotate the same and verify the Design
   e. Verify & Optimize for Time, Power and Area to the given constraint*

2. Design the following circuits with given specifications**, completing the design flow mentioned below:
   a. Draw the schematic and verify the following
      i) DC Analysis
      ii) AC Analysis
      iii) Transient Analysis
   b. Draw the Layout and verify the DRC, ERC
   c. Check for LVS
   d. Extract RC and back annotate the same and verify the Design.

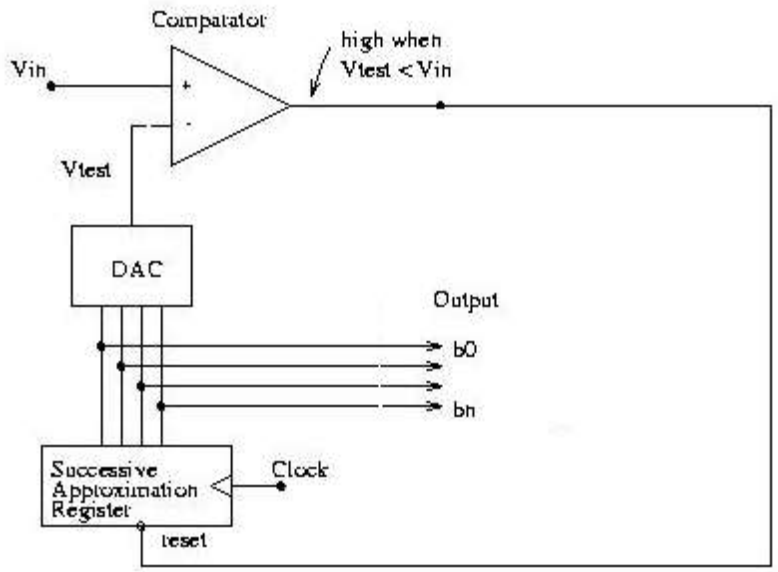
3. Design an op-amp with given specification** using given differential amplifier Common source and Common Drain amplifier in library*** and completing the design flow mentioned below:
   a. Draw the schematic and verify the following
      i) DC Analysis
      ii). AC Analysis
      iii) Transient Analysis
   b. Draw the Layout and verify the DRC, ERC
   c. Check for LVS
   d. Extract RC and back annotate the same and verify the Design.

4. Design a 4 bit R-2R based DAC for the given specification and completing the design flow mentioned using given op-amp in the library***.
   a. Draw the schematic and verify the following

      i) DC Analysis
      ii) AC Analysis
      iii) Transient Analysis
   b. Draw the Layout and verify the DRC, ERC

5. For the SAR based ADC mentioned in the figure below draw the mixed signal schematic and verify the functionality by completing ASIC Design FLOW.

[Specifications to GDS-II]



* An appropriate constraint should be given.

** Appropriate specification should be given.

*** Applicable Library should be added & information should be given to the Designer.

Conduct of Practical Examination:

- All laboratory experiments are to be included for practical examination.
- For examination, one question from **PART-A** and one question from **PART-B** to be set.
- Students are allowed to pick one experiment from the lot.
- Change of experiment is allowed only once and Marks allotted to the procedure part to be made zero.