DIGITAL COMMUNICATION

B.E., VI Semester, Electronics & Communication Engineering/ Telecommunication Engineering

[As per Choice Based Credit System (CBCS) scheme]

Subject Code	15EC61	IA Marks	20
Number of Lecture Hours/Week	04	Exam Marks	80
Total Number of Lecture Hours	50 (10 Hours/Module)	Exam Hours	03
CREDITS – 04			

Modules

Module-1

Bandpass signal to equivalent low pass: Hilbert Transform, Pre-envelopes, Complex envelopes, Canonical representation of bandpass signals, Complex low pass representation of band-pass systems, Complex representation of bandpass signals and systems.

Line codes: Unipolar, Polar, Bipolar (AMI) and Manchester code and their power spectral densities. Overview of HDB3, B3ZS, B6ZS.

(Text 1, Ref 1, 2)

Module-2

Signaling over AWGN channels-Detection and Estimation Introduction, Geometric representation of signals, Gram-Schmidt Orthogonalization procedure, Conversion of the continuous AWGN channel into a vector channel, Optimum receivers using coherent detection: ML Decoding, Correlation receiver, matched filter receiver. (Text 1)

Module-3

Digital Modulation Techniques: Digital modulation formats, Phase shift Keying techniques using coherent detection: BPSK, QPSK generation, detection and error probabilities, M-ary PSK, M-ary QAM.

Frequency shift keying techniques using Coherent detection: BFSK generation, detection and error probability.

Non coherent orthogonal modulation techniques: BFSK, DPSK Symbol representation, Block diagrams treatment of Transmitter and Receiver, Probability of error (Without derivation) (Text 1).

Module-4

Communication through Band Limited Channels: Digital Transmission through Band limited channels - Inter Symbol Interference, Eye diagrams, Signal design for Band limited ideal channel with zero ISI – Nyquist Criterion (statement only), Sinc and Raised pulse shaping.

Signal design for Band limited channel with controlled ISI – Correlative coding, DB and MDB, Precoding.

Basic Concepts of Equalization for non ideal channels – ZFE, MMSE, (without derivations), Adaptive Equalizers (Block diagram only) (Text 2, Ref 2).

Module-5

Principles of Spread Spectrum: Concept of Spread Spectrum, Direct Sequence/SS, Frequency Hopped SS, Processing Gain, Interference, and probability of error statement only.

PN sequences for Spread Spectrum – M- sequences with Properties; Gold, Kasami sequences with basic properties.

Direct sequence spread spectrum system concepts, Frequency Hopped Spread spectrum system concepts,

Spread Spectrum Synchronization (block diagram treatment) - Code Acquisition and Tracking. (Text 2)

Question paper pattern:

- The question paper will have ten questions
- Each full question consists of 16marks**.**
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module
- The students will have to answer 5 full questions, selecting one full question from each module

Text Book:

1. Simon Haykin, "Digital Communication Systems", John Wiley & sons, First Edition, 2014, ISBN 978-0-471-64735-5.
2. John G Proakis and Masoud Salehi, "Fundamentals of Communication Systems", 2014 Edition, Pearson Education, ISBN 978-8-131-70573-5.

Reference Books:

1. Ian A Glover and Peter M Grant, "Digital Communications", Pearson Education, Third Edition, 2010, ISBN 978-0-273-71830-7.
2. B.P.Lathi and Zhi Ding, "Modern Digital and Analog communication Systems", Oxford University Press, 4th Edition, 2010, ISBN: 978-0-198-07380-2.

ARM MICROCONTROLLER & EMBEDDED SYSTEM

B.E., VI Semester, Electronics & Communication Engineering/ Telecommunication Engineering

[As per Choice Based Credit System (CBCS) scheme]

Subject Code	15EC62	IA Marks	20
Number of Lecture Hours/Week	04	Exam Marks	80
Total Number of Lecture Hours	50 (10 Hours / Module)	Exam Hours	03
CREDITS – 04			

Modules

Module-1

ARM-32 bit Microcontroller: Thumb-2 technology and applications of ARM, Architecture of ARM Cortex M3, Various Units in the architecture, Debugging support, General Purpose Registers, Special Registers, exceptions, interrupts, stack operation, reset sequence (Text 1: Ch 1, 2, 3)

Module-2

ARM Cortex M3 Instruction Sets and Programming: Assembly basics, Instruction list and description, useful instructions, Assembly and C language Programming (Text 1: Ch-4, Ch-5, Ch-10 (10.1, 10.2, 10.3, 10.5 only))

Module-3

Embedded System Components: Embedded Vs General computing system, Classification of Embedded systems, Major applications and purpose of ES. Core of an Embedded System including all types of processor/controller, Memory, Sensors, Actuators, LED, 7 segment LED display, Optocoupler, relay, Piezo buzzer, Push button switch, Communication Interface (onboard and external types), Embedded firmware, Other system components.
(Text 2: All the Topics from Ch-2 and Ch-3, excluding 2.3 & 3.4 (stepper motor), 2.3 & 3.8 (keyboard) and 2.3 & 3.9 (PPI) sections).

Module-4

Embedded System Design Concepts: Characteristics and Quality Attributes of Embedded Systems, Operational and non-operational quality attributes, Embedded Systems-Application and Domain specific, Hardware Software Co-Design and Program Modelling (excluding UML), Embedded firmware design and development (excluding C language).
(Text 2: Ch-3, Ch-4, Ch-7 (Sections 7.1, 7.2 only), Ch-9 (Sections 9.1, 9.2, 9.3.1, 9.3.2 only)

Module-5

RTOS and IDE for Embedded System Design: Operating System basics, Types of operating systems, Task, process and threads (Only POSIX Threads with an example program), Thread preemption, Preemptive Task scheduling techniques, Task Communication, Task synchronization issues – Racing and Deadlock, Concept of Binary and counting semaphores (Mutex example without any program), How to

choose an RTOS, Integration and testing of Embedded hardware and firmware, Embedded system Development Environment – Block diagram (excluding Keil), Disassembler/decompiler, simulator, emulator and debugging techniques
(Text 2: Ch-10 (Sections 10.1, 10.2, 10.3, 10.5.2 , 10.7, 10.8.1.1, 10.8.1.2, 10.8.2.2, 10.10 only), Ch 12, Ch-13 (a block diagram before 13.1, 13.3, 13.4, 13.5, 13.6 only)

Question paper pattern:

- The question paper will have ten questions
- Each full question consists of 16marks**.**
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module
- The students will have to answer 5 full questions, selecting one full question from each module

Text Book:

1. Joseph Yiu, "The Definitive Guide to the ARM Cortex-M3", 2nd Edition, Newnes, (Elsevier), 2010.
1.
2. Shibu K V, "Introduction to Embedded Systems", Tata McGraw Hill Education Private Limited, 2009.

VLSI Design

B.E., VI Semester, Electronics & Communication Engineering

[As per Choice Based Credit System (CBCS) scheme]

Subject Code	15EC63	IA Marks	20
Number of Lecture Hours/Week	04	Exam Marks	80
Total Number of Lecture Hours	50 (10 Hours / Module)	Exam Hours	03
CREDITS – 04			

Modules

Module-1

Introduction: A Brief History, MOS Transistors, MOS Transistor Theory, Ideal I-V Characteristics, Non-ideal I-V Effects, DC Transfer Characteristics (1.1, 1.3, 2.1, 2.2, 2.4, 2.5 of TEXT 2).

Fabrication: nMOS Fabrication, CMOS Fabrication[P-well process, N-well process, Twin tub process], BiCMOS Technology (1.7, 1.8,1.10 of TEXT 1).

Module-2

MOS and BiCMOS Circuit Design Processes: MOS Layers, Stick Diagrams, Design Rules and Layout.

Basic Circuit Concepts: Sheet Resistance, Area Capacitances of Layers, Standard Unit of Capacitance, Some Area Capacitance Calculations, Delay Unit, Inverter Delays, Driving Large Capacitive Loads (3.1 to 3.3, 4.1, 4.3 to 4.8 of TEXT 1).

Module-3

Scaling of MOS Circuits: Scaling Models & Scaling Factors for Device Parameters

Subsystem Design Processes: Some General considerations, An illustration of Design Processes, **Illustration of the Design Processes**- Regularity, Design of an ALU Subsystem, The Manchester Carry-chain and Adder Enhancement Techniques (5.1, 5.2, 7.1, 7.2, 8.2, 8.3, 8.4.1, 8.4.2 of TEXT 1).

Module-4

Subsystem Design: Some Architectural Issues, Switch Logic, Gate(restoring) Logic, Parity Generators, Multiplexers, The Programmable Logic Array (PLA) (6.1 to 6.3, 6.4.1, 6.4.3, 6.4.6 of TEXT1).

FPGA Based Systems: Introduction, Basic concepts, Digital design and FPGA's, FPGA based System design, FPGA architecture, Physical design for FPGA's (1.1 to 1.4, 3.2, 4.8 of TEXT 3).

Module-5

Memory, Registers and Aspects of system Timing- System Timing Considerations, Some commonly used Storage/Memory elements (9.1, 9.2 of TEXT 1).

Testing and Verification: Introduction, Logic Verification, Logic Verification Principles, Manufacturing Test Principles, Design for testability (12.1, 12.1.1, 12.3, 12.5,12.6 of TEXT 2).

Question paper pattern:

- The question paper will have ten questions
- Each full question consists of 16marks**.**
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module
- The students will have to answer 5 full questions, selecting one full question from each module

Text Book:

1. **"Basic VLSI Design"**- Douglas A. Pucknell & Kamran Eshraghian, PHI 3rd Edition (original Edition – 1994).
2. **"CMOS VLSI Design- A Circuits and Systems Perspective"-** Neil H.E. Weste, David Harris, Ayan Banerjee, 3rd Edition, Pearson Education.
3. **"FPGA Based System Design"-**Wayne Wolf, Pearson Education, 2004, Technology and Engineering.

COMPUTER COMMUNICATION NETWORKS

B.E., VI Semester, Electronics & Communication Engineering / Telecommunication Engineering

[As per Choice Based Credit System (CBCS) scheme]

Subject Code	15EC64	IA Marks	20
Number of Lecture Hours/Week	04	Exam Marks	80
Total Number of Lecture Hours	50 (10 Hours / Module)	Exam Hours	03
CREDITS – 04			

Modules

Module-1

Introduction: Data Communications: Components, Representations, Data Flow, Networks: Physical Structures, Network Types: LAN, WAN, Switching, Internet.

Network Models: Protocol Layering: Scenarios, Principles, Logical Connections, TCP/IP Protocol Suite: Layered Architecture, Layers in TCP/IP suite, Description of layers, Encapsulation and Decapsulation, Addressing, Multiplexing and Demultiplexing, The OSI Model: OSI Versus TCP/IP.

Data-Link Layer: Introduction: Nodes and Links, Services, Categories' of link, Sublayers, Link Layer addressing: Types of addresses, ARP. Data Link Control (DLC) services: Framing, Flow and Error Control, Data Link Layer Protocols: Simple Protocol, Stop and Wait protocol, Piggybacking.

Module-2

Media Access Control: Random Access: ALOHA, CSMA, CSMA/CD, CSMA/CA. Controlled Access: Reservation, Polling, Token Passing.

Wired LANs: Ethernet: Ethernet Protocol: IEEE802, Ethernet Evolution, Standard Ethernet: Characteristics, Addressing, Access Method, Efficiency, Implementation, Fast Ethernet: Access Method, Physical Layer, Gigabit Ethernet: MAC Sublayer, Physical Layer, 10 Gigabit Ethernet.

Module-3

Wireless LANs: Introduction: Architectural Comparison, Characteristics, IEEE 802.11: Architecture, MAC sublayer, Adressing Mechanism, Physical Layer, Bluetooth: Architecture, Layers.

Connecting Devices: Hubs, Switches, **Virtual LANs:** Membership, Configuration, Communication between Switches, Advantages.

Network Layer: Introduction, Network Layer services: Packetizing, Routing and Forwarding, Other services, Packet Switching: Datagram Approach, Virtual Circuit Approach, IPV4 Addresses: Address Space, Classful Addressing, Classless Addressing, DHCP, Network Address Resolution, Forwarding of IP Packets: Based on destination Address and Label.

Module-4

Network Layer Protocols: Internet Protocol (IP): Datagram Format, Fragmentation, Options, Security of IPv4 Datagrams, ICMPv4: Messages, Debugging Tools, Mobile IP: Addressing, Agents, Three Phases, Inefficiency in Mobile IP.

Unicast Routing: Introduction, Routing Algorithms: Distance Vector Routing, Link State Routing, Path vector routing, Unicast Routing Protocol: Internet Structure, Routing Information Protocol, Open Shortest Path First, Border Gateway Protocol Version 4.

Module-5

Transport Layer: Introduction: Transport Layer Services, Connectionless and Connection oriented Protocols, Transport Layer Protocols: Simple protocol, Stop and wait protocol, Go-Back-N Protocol, Selective repeat protocol, User Datagram Protocol: User Datagram, UDP Services, UDP Applications, Transmission Control Protocol: TCP Services, TCP Features, Segment, Connection, State Transition diagram, Windows in TCP, Flow control, Error control, TCP congestion control.

Question paper pattern:

- The question paper will have ten questions
- Each full question consists of 16 marks**.**
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module
- The students will have to answer 5 full questions, selecting one full question from each module

Text Book:

1. Data Communications and Networking , Forouzan, 5th Edition, McGraw Hill, 2016 ISBN: 1-25-906475-3

Reference Books:

1. Computer Networks, James J Kurose, Keith W Ross, Pearson Education, 2013, ISBN: 0-273-76896-4
2. Introduction to Data Communication and Networking, Wayarles Tomasi, Pearson Education, 2007, ISBN:0130138282

CELLULAR MOBILE COMMUNICATIONS

B.E., VI Semester, Electronics & Communication Engineering/ Telecommunication Engineering

[As per Choice Based Credit System (CBCS) scheme]

Subject Code	15EC651	IA Marks	20
Number of Lecture Hours/Week	03	Exam Marks	80
Total Number of Lecture Hours	40 (8 Hours / Module)	Exam Hours	03
CREDITS – 03			

Modules

Module-1

Cellular Concept: Frequency Reuse, Channel Assignment Strategies, Interference and System Capacity, Power Control for Reducing Interference, Trunking and Grade of Service, Improving Capacity in Cellular Systems.

Mobile Radio Propagation: Large Scale path Loss- Free Space Model, Three basic propagation mechanisms, Practical Link Budget Design using Path Loss Models, Outdoor Propagation Models – Okumura, Hata, PCS Extension to Hata Model (explanations only) (Text 1).

Module-2

Mobile Radio Propagation: Small-Scale Fading and Multipath:

Small scale Multipath Propagation, Impulse Response Model of a Multipath Channel, Small-Scale Multipath Measurements, Parameters of Mobile Multipath Channels, Types of Small-Scale Fading, Rayleigh and Ricean Distributions, Statistical Model for Multipath Fading Channels (Clarke's Model for Flat Fading only). (Text 1)

Module-3

System Architecture and Addressing:

System architecture, The SIM concept, Addressing, Registers and subscriber data, Location registers (HLR and VLR) Security-related registers (AUC and EIR), Subscriber data, Network interfaces and configurations.

Air Interface – GSM Physical Layer:

Logical channels, Physical channels, Synchronization- Frequency and clock synchronization, Adaptive frame synchronization, Mapping of logical onto physical channels, Radio subsystem link control, Channel coding, source coding and speech processing, Source coding and speech processing, Channel coding, Power-up scenario.

GSM Protocols:

Protocol architecture planes, Protocol architecture of the user plane, Protocol architecture of the signaling plane, Signaling at the air interface (Um), Signaling at the A and Abis interfaces, Security-related network functions, Signaling at the user interface. (Text 2)

Module-4

GSM Roaming Scenarios and Handover:

Mobile application part interfaces, Location registration and location update,

Connection establishment and termination, Handover. (upto 6.4.1 only in Text2)

Services:

Classical GSM services, Popular GSM services: SMS and MMS

Improved data services in GSM: **GPRS, HSCSD and EDGE**

GPRS System architecture of GPRS , Services , Session management, mobility management and routing, Protocol architecture, Signaling plane, Interworking with IP networks, Air interface, Authentication and ciphering, Summary of GPRS .

HSCSD: Architecture, Air interface, HSCSD resource allocation and capacity issues.

EDGE: The EDGE concept, EDGE physical layer, modulation and coding, EDGE: effects on the GSM system architecture, ECSD and EGPRS. (Text 2)

Module-5

CDMA Technology – Introduction to CDMA,CDMA frequency bands, CDMA Network and System Architecture, CDMA Channel concept, Forward Logical Channels, Reverse logical Channels, CDMA frame format, CDMA System Operations (Initialization/Registration), Call Establishment, CDMA Call handoff,IS-95B,CDMA200,W-CDMA,UMTS,CDMA data networks, Evolution of CDMA to 3G,Cdma2000 RAN Components, Cdma 2000 Packet Data Service. (Text 3)

Question paper pattern:

- The question paper will have ten questions
- Each full question consists of 16 marks**.**
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module
- The students will have to answer 5 full questions, selecting one full question from each module

Text Book:

1. Theodore Rapport, "Wireless Communications – Principles and Practice", Prentice Hall of India , 2nd Edition, 2007, ISBN 978-8-120-32381-0.
2. Jorg Eberspacher, Hans-Jorg Vogel, Christian Bettstetter, Christian Hartmann, "GSM– Architecture, Protocols and Services", Wiley, 3rd Edition, 2009, ISBN-978-0-470-03070-7.
3. Gary J Mullet, "Introduction To Wireless Telecommunications Systems and Networks", Cengage Learning.

Adaptive Signal Processing

B.E., VI Semester, Electronics & Communication Engineering/ Telecommunication Engineering

[As per Choice Based Credit System (CBCS) scheme]

Subject Code	15EC652	IA Marks	20
Number of Lecture Hours/Week	03	Exam Marks	80
Total Number of Lecture Hours	40 (8 Hours / Module)	Exam Hours	03
CREDITS – 03			

Modules

Module-1

Adaptive systems : definitions and characteristics - applications - properties- examples - adaptive linear combiner input signal and weight vectors - performance function-gradient and minimum mean square error - introduction to filtering- smoothing and prediction - linear optimum filtering-orthogonality - Wiener – Hopf equation-performance Surface (Chapters 1& 2 of Text).

Module-2

Searching performance surface-stability and rate of convergence : learning curve- gradient search - Newton's method - method of steepest descent - comparison - Gradient estimation - performance penalty - variance - excess MSE and time constants – mis adjustments (Chapters 4& 5 of Text).

Module-3

LMS algorithm convergence of weight vector: LMS/Newton algorithm - properties - sequential regression algorithm - adaptive recursive filters - random-search algorithms - lattice structure - adaptive filters with orthogonal signals (Chapters 6 & 8 of Text).

Module-4

Applications-adaptive modeling and system identification-adaptive modeling: multipath communication channel, geophysical exploration,FIR digital filter synthesis (Chapter 9 of Text).

Module-5

Inverse adaptive modeling, equalization, and deconvolution adaptive equalization of telephone channels-adapting poles and zeros for IIR digital filter synthesis (Chapter 10 of Text).

Question paper pattern:

- The question paper will have ten questions
- Each full question consists of 16 marks**.**
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module

- The students will have to answer 5 full questions, selecting one full question from each module

Text Book:

1. Bernard Widrow and Samuel D. Stearns, "Adaptive Signal Processing", Person Education, 1985.

Reference Books:

2. Simon Haykin, "Adaptive Filter Theory", Pearson Education, 2003.
3. John R. Treichler, C. Richard Johnson, Michael G. Larimore, "Theory and Design of Adaptive Filters", Prentice-Hall of India, 2002.

ARITIFICAL NEURAL NETWORKS

B.E., VI Semester, Electronics & Communication Engineering/ Telecommunication Engineering

[As per Choice Based Credit System (CBCS) scheme]

Subject Code	15EC653	IA Marks	20
Number of Lecture Hours/Week	03	Exam Marks	80
Total Number of Lecture Hours	40 (8 Hours / Module)	Exam Hours	03
CREDITS – 03			

Modules

Module-1

Introduction: Biological Neuron – Artificial Neural Model - Types of activation functions – **Architecture**: Feedforward and Feedback, Convex Sets, Convex Hull and Linear Separability, Non-Linear Separable Problem. Xor Problem, Multilayer Networks.

Learning: Learning Algorithms, Error correction and Gradient Descent Rules, Learning objective of TLNs, Perceptron Learning Algorithm, Perceptron Convergence Theorem.

Module-2

Supervised Learning: Perceptron learning and Non Separable sets,α-Least Mean Square Learning, MSE Error surface, Steepest Descent Search, μ-LMS approximate to gradient descent, Application of LMS to Noise Cancelling, Multi-layered Network Architecture, Backpropagation Learning Algorithm, Practical consideration of BP algorithm.

Module-3

Support Vector Machines and Radial Basis Function : Learning from Examples, Statistical Learning Theory,Support Vector Machines, SVM application to Image Classification, Radial Basis Function Regularization theory, Generalized RBF Networks, Learning in RBFNs, RBF application to face recognition.

Module-4

Attractor Neural Networks: Associative Learning Attractor Associative Memory, Linear Associative memory, Hopfield Network, application of Hopfield Network, Brain State in a Box neural Network, Simulated Annealing, Boltzmann Machine, Bidirectional Associative Memory.

Module-5

Self-organization Feature Map: Maximal Eigenvector Filtering, Extracting Principal Components, Generalized Learning Laws, Vector Quantization, Self-organization Feature Maps, Application of SOM, Growing Neural Gas.

Question paper pattern:

The question paper will have ten questions.

- Each full question consists of 16 marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module. The students will have to answer 5 full questions, selecting one full question from each module.

Text Books:

1. **Neural Networks A Classroom Approach**– Satish Kumar, McGraw Hill Education (India) Pvt. Ltd, Second Edition.

Reference Books:

1. **Introduction to Artificial Neural Systems-**J.M. Zurada, Jaico Publications 1994.
2. **Artificial Neural Networks-**B. Yegnanarayana, PHI, New Delhi 1998.

DIGITAL SWITCHING SYSTEMS

B.E., VI Semester, Electronics & Communication Engineering/ Telecommunication Engineering

[As per Choice Based Credit System (CBCS) scheme]

Subject Code	15EC654	IA Marks	20
Number of Lecture Hours/Week	03	Exam Marks	80
Total Number of Lecture Hours	40 (8 Hours / Module)	Exam Hours	03
CREDITS – 03			

Module-1

DEVELOPMENT OF TELECOMMUNICATIONS: Network structure, Network services, terminology, Regulation, Standards. Introduction to telecommunications transmission, Power levels, Four wire circuits, Digital transmission, FDM,TDM, PDH and SDH [Text-1]

Module-2

EVOLUTION OF SWITCHING SYSTEMS: Introduction, Message switching, Circuit switching, Functions of switching systems, Distribution systems, Basics of crossbar systems, Electronic switching.

DIGITAL SWITCHING SYSTEMS: Switching system hierarchy, Evolution of digital switching systems, Stored program control switching systems, Building blocks of a digital switching system, Basic call processing. [Text-1 and 2]

Module-3

TELECOMMUNICATIONS TRAFFIC: Introduction, Unit of traffic, Congestion, Traffic measurement, Mathematical model, lost call systems, Queuing systems.

SWITCHING SYSTEMS: Introduction, Single stage networks, Gradings, Link Systems, GOS of Linked systems. [Text-1]

Module-4

TIME DIVISION SWITCHING: Introduction, space and time switching, Time switching networks, Synchronisation.

SWITCHING SYSTEM SOFTWARE: Introduction, Basic software architecture, Software architecture for level 1to 3 control, Digital switching system software classification, Call models, Software linkages during call, Feature flow diagram, Feature interaction. [Text-1 and 2]

Module-5

MAINTENANCE OF DIGITAL SWITCHING SYSTEM: Introduction , Software maintenance, Interface of a typical digital switching system central office, System outage and its impact on digital switching system reliability, Impact of software patches on digital switching system maintainability, A methodology for proper maintenance of digital switching system

A GENERIC DIGITAL SWITCHING SYSTEM MODEL: Introduction, Hardware architecture, Software architecture, Recovery strategy, Simple call through a digital system, Common characteristics of digital switching systems. Reliability analysis. [Text-2]

Question paper pattern:

- The question paper will have ten questions
- Each full question consists of 16 marks**.**
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module
- The students will have to answer 5 full questions, selecting one full question from each module

TEXT BOOKS:

1. Telecommunication and Switching, Traffic and Networks - J E Flood: Pearson Education, 2002.

2. Digital Switching Systems, Syed R. Ali, TMH Ed 2002.

REFERENCE BOOK:

Digital Telephony - John C Bellamy: Wiley India Pvt. Ltd, 3rd Ed, 2008.

MICROELECTRONICS

B.E., VI Semester, Electronics & Communication Engineering/ Telecommunication Engineering

[As per Choice Based Credit System (CBCS) scheme]

Subject Code	15EC655	IA Marks	20
Number of Lecture Hours/Week	03	Exam Marks	80
Total Number of Lecture Hours	40 (8 Hours / Module)	Exam Hours	03
CREDITS – 03			

Modules

Module-1

MOSFETS: Device Structure and Physical Operation, V-I Characteristics, MOSFET Circuits at DC, MOSFET as an amplifier and as a switch.

Module-2

MOSFETS (continued): Biasing in MOS amplifier Circuits, Small Signal Operation and Models, basic MOSFET amplifier, MOSFET internal capacitances, frequency response of CS amplifier.

Module-3

MOSFETS (continued): Discrete circuit MOS amplifiers.

Single Stage IC Amplifier: Comparison of MOSFET and BJT, Current sources, Current mirrors and Current steering circuits, high frequency response- general considerations.

Module-4

Single Stage IC Amplifier (continued): CS with active loads, high frequency response of CS, CG amplifiers with active loads, high frequency response of CG, Cascode amplifiers. CS with source degeneration (only MOS amplifiers to be dealt).

Module-5

Differential and Multistage Amplifiers: The MOS differential pair, small signal operation of MOS differential pair, Differential amplifier with active loads, and frequency response of the differential amplifiers. Multistage amplifiers (only MOS amplifiers to be dealt).

Question paper pattern:

- The question paper will have ten questions
- Each full question consists of 16 marks**.**
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module
- The students will have to answer 5 full questions, selecting one full question from each module

Text Book:

1. **"Microelectronic Circuits",** Adel Sedra and K.C. Smith, 6th Edition, Oxford

University Press, International Version, 2009.

Reference Books:

1. **"Microelectronics An integrated approach",** Roger T Howe, Charles G Sodini, Pearson education.
2. **"Fundamentals of Microelectronics",** Behzad Razavi, John Wiley India Pvt. Ltd, 2008.
3. **"Microelectronics – Analysis and Design",** Sundaram Natarajan, Tata McGraw-Hill, 2007

Embedded Controller Lab

B.E., VI Semester, Electronics & Communication Engineering/ Telecommunication Engineering

[As per Choice Based Credit System (CBCS) scheme]

Subject Code	15ECL67	IA Marks	20
Number of Lecture Hours/Week	01Hr Tutorial (Instructions) + 02 Hours Laboratory = 03	Exam Marks	80
		Exam Hours	03
CREDITS – 02			

Laboratory Experiments

PART-A: Conduct the following Study experiments to learn ALP using ARM Cortex M3 Registers using an Evaluation board and the required software tool.

1. ALP to multiply two 16 bit binary numbers.
2. ALP to find the sum of first 10 integer numbers.

PART-B: Conduct the following experiments on an ARM CORTEX M3 evaluation board using evaluation version of Embedded 'C' & Keil Uvision-4 tool/compiler.

1. Display “Hello World” message using Internal UART.
2. Interface and Control a DC Motor.
3. Interface a Stepper motor and rotate it in clockwise and anti-clockwise direction.
4. Determine Digital output for a given Analog input using Internal ADC of ARM controller.
5. Interface a DAC and generate Triangular and Square waveforms.
6. Interface a 4x4 keyboard and display the key code on an LCD.
7. Using the Internal PWM module of ARM controller generate PWM and vary its duty cycle.

8. Demonstrate the use of an external interrupt to toggle an LED On/Off.
9. Display the Hex digits 0 to F on a 7-segment LED interface, with an appropriate delay in between.
10. Interface a simple Switch and display its status through Relay, Buzzer and LED.
11. Measure Ambient temperature using a sensor and SPI ADC IC.

Conduction of Practical Examination:

1. PART-B experiments using Embedded-C are only to be considered for the practical examination. PART-A ALP programs are for study purpose and can be considered for Internal Marks evaluation.

2. Strictly follow the instructions as printed on the cover page of answer script for breakup of marks.

3. Change of experiment is allowed only once and 15% of Marks allotted to the procedure part to be made zero.

COMPUTER NETWORKS LABORATORY

B.E., VI Semester, Electronics & Communication Engineering

[As per Choice Based Credit System (CBCS) scheme]

Subject Code	15ECL68	IA Marks	20
Number of Lecture Hours/Week	01Hr Tutorial (Instructions) + 02 Hours Laboratory = 03	Exam Marks	80
		Exam Hours	03

CREDITS – 02

Course objectives: This course will enable students to:

- Choose suitable tools to model a network and understand the protocols at various OSI reference levels.
- Design a suitable network and simulate using a Network simulator tool.
- Simulate the networking concepts and protocols using C/C++ programming.
- Model the networks for different configurations and analyze the results.

Laboratory Experiments

PART-A: Simulation experiments using NS2/ NS3/ OPNET/ NCTUNS/ NetSim/ QualNet/ Packet Tracer or any other equivalent tool

1. Implement a point to pint network with four nodes and duplex links between them. Analyze the network performance by setting the queue size and varying the bandwidth.
2. Implement a four node point to point network with links n0-n2, n1-n2 and n2-n3. Apply TCP agent between n0-n3 and UDP between n1-n3. Apply relevant applications over TCP and UDP agents changing the parameter and determine the number of packets sent by TCP/UDP.
3. Implement Ethernet LAN using n (6-10) nodes. Compare the throughput by changing the error rate and data rate.
4. Implement Ethernet LAN using n nodes and assign multiple traffic to the nodes and obtain congestion window for different sources/ destinations.
5. Implement ESS with transmission nodes in Wireless LAN and obtain the performance parameters.
6. Implementation of Link state routing algorithm.

PART-B: Implement the following in C/C++

1. Write a program for a HLDC frame to perform the following.
   i) Bit stuffing
   ii) Character stuffing.
2. Write a program for distance vector algorithm to find suitable path for transmission.
3. Implement Dijkstra's algorithm to compute the shortest routing path.
4. For the given data, use CRC-CCITT polynomial to obtain CRC code. Verify the program for the cases
   a. Without error
   b. With error
5. Implementation of Stop and Wait Protocol and Sliding Window Protocol
6. Write a program for congestion control using leaky bucket algorithm.

Course outcomes: On the completion of this laboratory course, the students will be able to:

1. Design and Simulate Network elements with various protocols and standards.
2. Use the network simulator tools for learning and practice of networking algorithms.
3. Demonstrate the working of various protocols and algorithms using C programming.

Graduate Attributes (as per NBA)

- Engineering Knowledge.
- Problem Analysis.
- Design/Development of solutions.

Conduct of Practical Examination:

- All laboratory experiments are to be included for practical examination.
- For examination one question from software and one question from hardware or only one hardware experiments based on the complexity to be set.
- Students are allowed to pick one experiment from the lot.
- Strictly follow the instructions as printed on the cover page of answer script for breakup of marks.
- Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.