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06EC63

Sixth Semester B.E. Degree Examination, June 2012
Analog and Mixed Mode VLSI Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

PART – A

1 a. Determine the number of quantization levels needed if one wanted to make a digital thermometer that is capable of measuring temperature within 0.1°C accuracy over the range –50°C to 150°C. What is the resolution of ADC? **(04 Marks)**

b. Calculate DNL for a 3 bit ADC for the transfer curve shown in Fig.Q1(b). Assume V_{ref}= 5V. Draw the quantization error Q_e in units of LSB. **(06 Marks)**

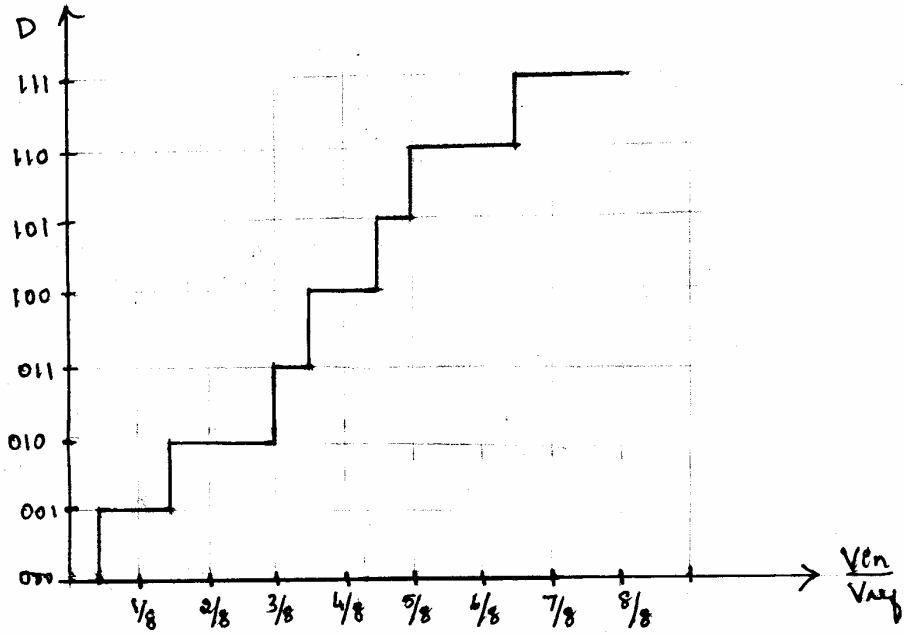

Fig.Q1(b)

c. With a neat diagram, explain the mixed signal layout issues in detail. **(10 Marks)**

2 a. Plot the transfer curve of a 3-bit R-2R DAC, if all R_s = 1.1 kΩ and $2R_s$ = 2 kΩ. What is the max INL for the converter? Assume all of the switch to be ideal and V_{ref} = 5 V. **(12 Marks)**

b. Design a 3 bit pipeline DAC and explain its operation. Also find the output voltage for a 3-bit pipeline DAC for 3 cases D_A = 101, D_B = 010, D_C = 011. Show that the conversion time to perform all three conversions is 5 clock cycles using pipeline approach. Assume V_{ref} = 5 V. **(08 Marks)**

3 a. With a neat diagram, explain the operation of a parallel feed through ADC along with its advantages and disadvantages. **(08 Marks)**

b. Design a 3 bit pipeline ADC. Analyse the conversion process by making a table for D_2, D_1, D_0, V_2, V_1 for V_{in} = 2V, 3V, 4.5V. Assume V_{ref} = 5V. Let V_3 be residue of 1st stage and V_2 be residue of 2nd stage. **(06 Marks)**

c. Explain the operation of a single slope ADC, with a neat diagram. **(06 Marks)**

4 a. Draw the block diagram of a high performance comparator and hence explain the operation of a decision circuit and obtain an expression for switching point. **(10 Marks)**

b. Explain the operation of a CMOS quad multiplier and hence obtain an expression for the multiplier output voltage. **(10 Marks)**

PART – B

5 a. Develop an expression for the effective number of bits in terms of measured SNR if the input sinewave has a peak amplitude of 40% of ($V_{ref+} - V_{ref-}$). **(06 Marks)**

b. Explain dump and interpolate circuit used for interpolation and reverse averaging. **(08 Marks)**

c. What is the magnitude response of $(1 - z^{-1})^3$. Sketch a block diagram implementation of the filter. **(06 Marks)**

6 a. Explain the sub-mirror CMOS process flow with a neat diagram. **(12 Marks)**

b. Estimate the size of Metal1 only to obtain the capacitance of 1 pF for the capacitor layout shown in Fig.Q6(b). Also estimate the bottom parasitic capacitance. **(04 Marks)**

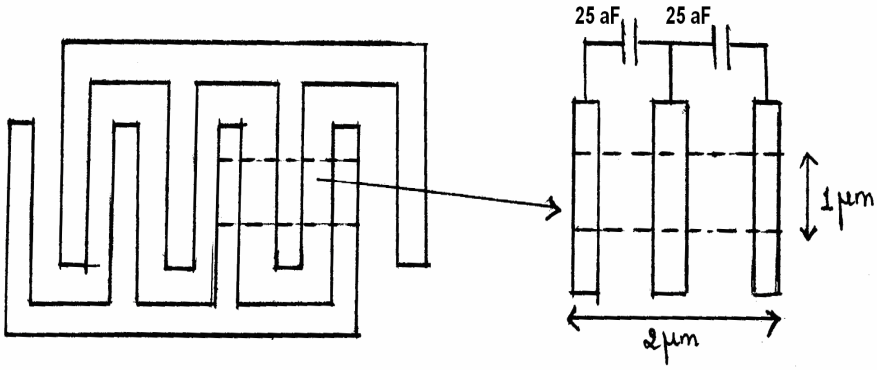

Fig.Q6(b)

c. Explain the fabrication of resistor using n-well. **(04 Marks)**

7 a. Explain the operation of D-Flip flop using TSPC logic and clocked CMOS logic with a neat diagram. **(08 Marks)**

b. Write the design equation for full adder. Using the equation, design full adder using dynamic logic. **(08 Marks)**

c. For the circuit shown in Fig.Q7(c), estimate the delay time. **(04 Marks)**

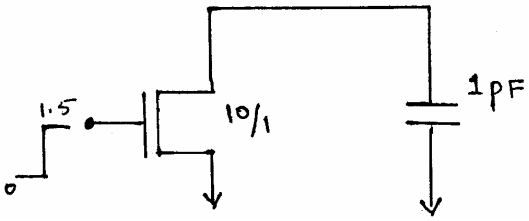

Fig.Q7(c)

8 a. Show that the floating current source will not load or decrease the resistance seen by cascade structure. **(08 Marks)**

b. Implement high speed, low power differential output op-amp and explain the operation. **(12 Marks)**

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