2002 SCHEME

USN | | | | | | | | | | |

EC64

Sixth Semester B.E. Degree Examination, June 2012

Digital System Design Using VHDL

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions.***

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

1 a. Bring out the difference between VHDL functions and procedures, with an example. **(06 Marks)**

b. Write VHDL code for square of three bit numbers. **(06 Marks)**

c. Explain selected signal assignment statement, using the same write VHDL code for a 4-to-1 MUX. **(08 Marks)**

2 a. Explain briefly packages and libraries. **(05 Marks)**

b. Write VHDL code for 2-to-4 binary decoder using process statement. **(05 Marks)**

c. Write VHDL code that represents a BCD-to-7 segment decoder using case statement. **(05 Marks)**

d. If A = "110", B = "111", C = "011000" and D = "111011", compute (A and not B or C ror2 and D). **(05 Marks)**

3 a. i) Draw a block diagram and write a VHDL description of an 8-bit bidirectional shift register that uses two 74194s as components. The parallel inputs and outputs to the 8-bit register should be X(7down to 0) and Y(7 down to 0). The serial inputs should be RSD and LSD.

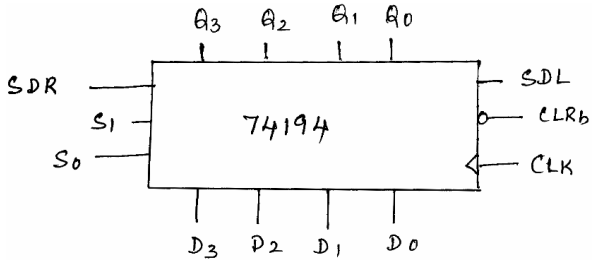


Fig.Q3(a)

ii) Write a behavioral level VHDL model for 74194. **(10 Marks)**

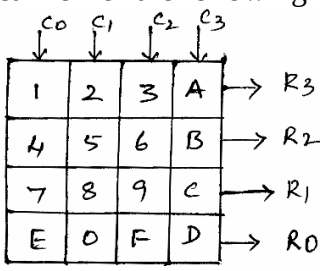
b. Realize the following functions using a PLA:

$F_1 = \sum m\ (2, 3, 5, 7, 8, 9, 10, 11, 13, 15)$

$F_2 = \sum m\ (2, 3, 5, 6, 7, 10, 11, 14, 15)$

$F_3 = \sum m\ (6, 7, 8, 9, 13, 14, 15)$ **(10 Marks)**

4 a. Design a 4 × 4 keypad scanner for the following keypad layout.



(continued)

Question.4(a) continued….

i) Assume only one key can be pressed at a time, find equations for a number decoder given R_{3-0} and C_{3-0}, whose output corresponds to the binary value of the key. For example, the F key will return N_{3-0} = 1111 in binary or 15.

ii) Design a debouncing circuit that detects when a key has been pressed or depressed. Assume switch bounce will die out in one or two clock cycles. When a key has been pressed, K = 1 and K_d is debounced signal. **(14 Marks)**

b. Write a short note on transport and inertial delay. **(06 Marks)**

5 a. Design a hardware required to multiply two 4 bit fraction (including sign bit). Also write a state graph for the control circuit. **(10 Marks)**

b. Explain the step by step procedure for carrying out the signed division. **(10 Marks)**

6 a. Explain briefly the block diagram for the dice game. Also write an SM chart and state graph for the same. **(14 Marks)**

b. Write behavioral model for dice game. **(06 Marks)**

7 a. List the steps required to design a digital system with an FPGA. **(05 Marks)**

b. Write and explain a simplified block diagram of an XC4000 configurable logic block. **(10 Marks)**

c. Differentiate between FPGA and CPLD. **(05 Marks)**

8 a. List the steps required to carryout floating point addition including all special cases. **(05 Marks)**

b. Specify the general form of generate statement. Write VHDL code for 16-to-1 MUX using a generate statement. **(10 Marks)**

c. List IEEE – 1164 standard logic system for use with VHDL. **(05 Marks)**

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