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10ES33

Third Semester B.E. Degree Examination, June 2012
Logic Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

PART – A

1 a. Define combinational logic. List the various steps in designing a combinational logic system. **(04 Marks)**

b. Define the following:
i) Literal
ii) Product of sums
iii) Canonical products of sums
iv) Sum of min-terms
v) Essential prime implicant. **(05 Marks)**

c. Simplify the function using K-Map:
$y = f(a, b, c, d) = \Pi M(0, 4, 5, 7, 8, 9, 11, 12, 13, 15)$. Write the simplified SOP and POS expression. **(06 Marks)**

d. Design a 4-bit odd parity detector circuit and realize it using only NAND gates. **(05 Marks)**

2 a. Simplify the following using Q-M method. Use decimal notations:
$f(a, b, c, d) = \sum (7, 9, 12, 13, 14, 15) + \sum d(4, 11)$. Realize the simplified expression using only NOR gates. **(10 Marks)**

b. Determine minimal sum and minimal product using MEV technique, taking a, b and c as the map variables.
$f(a, b, c, d) = \sum (3, 4, 5, 7, 8, 11, 12, 13, 15)$. Realize the simplified expression using only NAND gates. **(10 Marks)**

3 a. Design a combinational circuit to find the 9′s complement of a single digit BCD number. Realize the circuit using suitable logic gates. **(08 Marks)**

b. Implement the following function pairs using 74138 decoder:
$f_1(a, b, c) = \sum(0, 2, 4)$; $f_2(a, b, c) = \sum(1, 2, 4, 5, 7)$. **(06 Marks)**

c. Realize 16:4 encoder using two 8:3 priority encoders. **(06 Marks)**

4 a. Implement $f(a, b, c) = \sum(1, 4, 5, 7)$ using 4:1 multiplexer. **(06 Marks)**

b. Design a suitable BCD adder circuit using 7483 and provision has to be made for self correction in case if the sum is not a valid BCD number. Justify your design with examples. **(08 Marks)**

c. Design a 1-bit comparator using 2:4 decoder. Also design the circuit using only NOR gates. **(06 Marks)**

PART – B

5 a. Differentiate sequential logic circuit and combinational logic circuit. **(04 Marks)**

b. What is the difference between latch and flipflop? Explain the operation of SR latch with an example. **(06 Marks)**

c. Draw the circuit diagram of master slave JK flip flop using only NAND gates. Explain how race around condition is eliminated in this design. **(06 Marks)**

d. Write a note on 0s and 1s catching problem. **(04 Marks)**

6 a. Derive the characteristic equations of SR, JK, D and T flipflops. **(08 Marks)**

b. Design mod-11 asynchronous counter using JK flipflops. **(06 Marks)**

c. Design a 4 bit register using positive edge triggered D flipflops to operator as indicated in the table below–

Mode select a_1	a_0	Register operation
0	0	Hold
0	1	Clear
1	0	Complement contents
1	1	Circular right shift

Table 6(c) **(06 Marks)**

7 a. With a suitable example explain Mealy and Moore model in a sequential circuit analysis. **(10 Marks)**

b. A sequential circuit has one input and one output. The state diagram is as shown below in Fig.Q7(b). Design a sequential circuit using D-flipflop. **(10 Marks)**

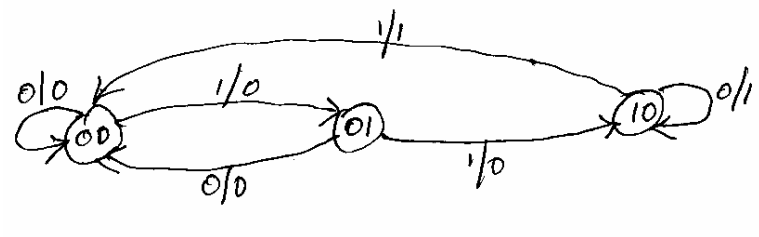

Fig.Q7(b)

8 a. Design a counter using JK flipflops whose sequence is {0, 1, 4, 6, 7, 5, 0 ……} by obtaining minimal sum equations. **(10 Marks)**

b. Design a synchronous 5421 code sequence using positive edge triggered D-flipflop with minimum combinational circuits. **(10 Marks)**

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