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06ES33

Third Semester B.E. Degree Examination, June 2012
Logic Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting atleast TWO questions each from Part – A and Part - B.***

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

PART - A

1 a. Convert the following into their proper canonical forms :
i) $P = (\overline{w} + x)(y + z)$ ii) $R = L + \overline{M}(\overline{N}M + \overline{M}L)$ **(04 Marks)**

b. Simplify the following noncanonical expressions using K – map and identify the prime – implicants and essential prime implicants.
i) $f(A, B, C, D) = \overline{A}\,\overline{C}D + \overline{A}CD + \overline{B}\,\overline{C}\,\overline{D} + A\overline{B}C + \overline{A}\,\overline{B}C\overline{D}$.
ii) $f(A, B, C, D) = (A + B + \overline{D})(\overline{A} + B + \overline{D})(A + \overline{B} + \overline{C} + D)(\overline{A} + \overline{B} + \overline{C} + \overline{D})(\overline{A} + \overline{B} + \overline{C} + D)$ **(08 Marks)**

c. Simplify the following using K – map and implement the simplified equation using basic gates.
i) $f(A, B, C, D) = \sum m(7, 9, 11, 12, 13, 14) + dc(3, 5, 6, 15)$.
ii) $f(A, B, C, D) = \pi M(2, 8, 11, 15) + dc(3, 12, 14)$. **(08 Marks)**

2 a. Simplify the following Boolean function using Quine Mccluskey minimization technique and prime implicant table reduction. $f(A, B, C, D) = \sum(1, 3, 13, 15) + \sum d(8, 9, 10, 11)$. **(12 Marks)**

b. Simplify the given SOP equation using MEV technique.
$f(A, B, C, D) = \sum(2, 3, 4, 5, 13, 15) + \sum d(8, 9, 10, 11)$. **(08 Marks)**

3 a. Design a combinational logic circuit that will convert a straight BCD digit to an excess – 3 BCD digits. i) construct the truth table ii) write the mintum list equation for each output iii) simplify the output equations and write the logic equations iv) Draw the resulting logic diagram. **(12 Marks)**

b. Draw the logic diagram for a 2 to 4 logic decoder with an active low encode enable and active high data outputs. Construct the truth table and identify the data inputs, the enable input, and the outputs. Draw the logic symbol for the decoder. **(06 Marks)**

c. Realize the following function using decoder.
i) $f(a, b, c) = \sum(2, 5)$ ii) $f(a, b, c) = \sum(3, 5, 6)$. **(02 Marks)**

4 a. Realize the Boolean function using 8:1 multiplexer
$f(x, y, z) = \sum(1, 2, 4, 5, 7)$. **(04 Marks)**

b. Design a full – adder.
i) Construct the truth table and simplify the output equations ii) Draw the logic diagram of full adder using basic gates. **(06 Marks)**

c. Explain a 4 – bit parallel adder with look ahead carry scheme. **(10 Marks)**

PART - B

5 a. Draw the logic diagram, construct the excitation table and write the characteristic equations for the following flip flops : i) R – S latch ii) Gated S – R latch iii) JK iv) T or toggle v) D or data flip flop. **(10 Marks)**

b. With a neat logic diagram, explain master – slave S – R flip flop. Explain the flip – flop action during control signal. Also write the function table. **(10 Marks)**

6 a. With a neat logic diagram, explain universal shift register. **(08 Marks)**

b. Explain the operation of mod – 7 twisted ring counter with its block diagram. Write the count sequence table and the decoding logic used to identify various states. **(08 Marks)**

c. Draw the logic diagram of 4 – bit binary ripple counter. Write the counting sequence and relevant timing diagram. **(04 Marks)**

7 a. Draw and explain Mealy and Moove synchronous machine models for clocked synchronous sequential circuits. Also define the following terms : i) Excitation table ii) State table iii) Transition table iv) State diagram. **(10 Marks)**

b. Construct the excitation table, transition table and state diagram for the sequential circuit given below, Fig. Q7(b) **(10 Marks)**

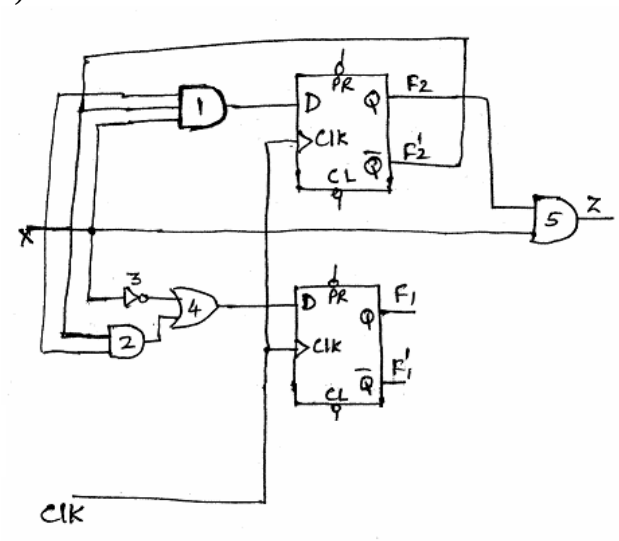

Fig.Q7(b)

8 a. Design a synchronous counter to count the sequence 0 → 4 → 1 → 2 → 6 → 0 using positive edge triggered SR flip flops. **(10 Marks)**

b. Construct a Mealy state diagram that will detect a serial input sequence of 10110. The detection of the required bit pattern can occur in a longer data string and the correct pattern can overlap with another pattern. When the input pattern has been detected, cause the output Z to be asserted high. Write the state table. **(10 Marks)**

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