USN | | | | | | | | | | |

06EC45

Fourth Semester B.E. Degree Examination, June 2012
Fundamentals of HDL

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO questions from each part.***

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

PART – A

1 a. Describe verilog data types with an example. **(08 Marks)**

b. For the following VHDL code, determine legal and illegal operations between data of different types.

```
SIGNAL a : BIT ;
SIGNAL b : BIT_VECTOR (7 DOWNTO 0);
SIGNAL c : STD_LOGIC ;
SIGNAL d : STD_LOGIC_VECTOR (7 DOWN TO 0);
SIGNAL e : INTEGER RANGE 0 TO 255;
…
   a < = b(5) ;
   b(0) < = a ;
   c < = d(5) ;
   d(0) < = c ;
   a < = c ;
   b < = d ;
   e < = b ;
   e < = d ;
```

(05 Marks)

c. Find the value of the expressions X1….X8, for the following VHDL signal declarations.

```
SIGNAL a : BIT : = '1' ;
SIGNAL b : BIT_VECTOR (3 DOWNTO 0) : = "1100";
SIGNAL c : BIT_VECTOR (3 DOWNTO 0) : = "0010";
SIGNAL d : BIT_VECTOR (7 DOWNTO 0) ;
```

i) X1 < = a and c;
ii) X2 < = c and b ;
iii) X3 < = b XOR c ;
iv) X4 < = a NOR b(3) ;
v) X5 < = b sll 2;
vi) X6 < = b sla 2;
vii) X7 < = b rol 2;
viii) X8 < = a AND NOT b(0) AND NOT c(1); **(07 Marks)**

2 a. Write a data – flow description in both VHDL and verilog of a system that has three 1 – bit input, a(1), a(2) and a(3) ; and one 1 – bit output b. The least significant bit is a(1); and b is I only when (a(3) a(2) a(1) = 1, 3, 6, or 7 (all in decimal), otherwise b is 0. Derive a minimized Boolean function of the system and write the data flow description. **(12 Marks)**

b. Write VHDL code using a data flow description of a full adder with enable. If the enable is low (0), the sum and carry are zero; otherwise, the sum and carry are the usual output of the adder. Draw the truth table of this adder, and derive the simplified Boolean function. **(08 Marks)**

3 a. Develop a VHDL model for a pipelined circuit that computes the average of corresponding values in three streams of input values, a, b and c. The pipeline consists of three stages : The first stage sums values of a and b and saves the value of c ; the second stage adds on the saved value of c, and third stage divides by three. The inputs and output are all signed fixed – point numbers indexed from 5 down to – 8. **(12 Marks)**

b. Explain the structure of the HDL behavioral description, with an example. **(08 Marks)**

4 a. Write a VHDL code, using structural description of a 3-bit comparator using adders. **(10 Marks)**

b. Develop a verilog model of a switch debouncer for a push button that uses a debounce interval of 10 ms. Assume the system clock frequency is 50 MHz. **(06 Marks)**

c. Write a verilog code of a pulse triggered master–slave JK flip flop, using structural description. **(04 Marks)**

PART – B

5 a. Explain how functions are described in VHDL and verilog. **(06 Marks)**

b. Develop VHDL code for signed vector multiplication, using procedure and tasks. **(14 Marks)**

6 a. Describe procedure for invoking a VHDL entity from a verilog module and a verilog module from a VHDL module. **(08 Marks)**

b. Develop mixed-language description of a 9-bit adder. **(08 Marks)**

c. Write a note on VHDL packages. **(04 Marks)**

7 a. List limitations of mixed-language description. **(04 Marks)**

b. Write mixed – language description of a simple RC filter. **(12 Marks)**

c. Describe instantiating CASEX in VHDL. **(04 Marks)**

8 a. With the help of flow chart. Explain synthesis steps in HDL. **(08 Marks)**

b. With an example, explain how mapping of procedure and task takes place in VHDL and verilog synthesis respectively. **(12 Marks)**

* * * * *