S J P N Trust's Hirasugar Institute of Technology, Nidasoshi

FACULTY PROFILE

1. ***Name in full*** : Sujatha. S. Kamate

2. ***Contact Nos.*** : *9008696825*

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: *sskamate21@gmail.com*

4. ***Date of Birth*** *01- 07-1980*

5. ***Address for communication:*** *"Shivanand"*
Basaveshwar Nagar,
Chikodi-591236
Dist : Belgaum, Karnataka

6. ***Educational qualifications :***

Sl. No	Degree	University/Institution	Year	Specialization
1.	Ph.D	VTU, Belagavi	2017	VLSI
2.	M.Tech	VTU, Belagavi/ GIT,Belagavi	2012	Digital Electronics
3.	B.E	VTU, Belgaum/ HIT, Nidasoshi	2002	Electronics and Communication

7. ***Details of previous employment:***

Sl. No	Name of the Institution/Organization	Period		Designation
		From	To	
1.	Hirasugar Institute of Technology, Nidasoshi	01-04-2018	Till date	Assistant Professor
2.	Hirasugar Institute of Technology, Nidasoshi	01-01-2017	31-03-2018	Associate Professor
3.	Hirasugar Institute of Technology, Nidasoshi	01-10-2013	31-12-2016	Assistant Professor

4.	Hirasugar Institute of Technology, Nidasoshi	01-09-2008	30-09-2013	Senior Lecturer
5.	Hirasugar Institute of Technology, Nidasoshi	06-09-2004	31-01-2008	Lecturer
6	C.B. Kore polytechnic, Chikodi	13-11-2002	03-09-2004	Lecturer
Total Experience in years 15.10yrs				

8. ***Date of Service in this Institution:*** ***06-09-2004***

9. ***Total Experience in years:*** ***15.10yrs***

10. ***Subjects of Interest:***

- ***Signals and Systems***
- ***Engineering Electromagnetics***
- ***VLSI DESIGN***
- ***Microelectronic Circuits***
- ***Control Systems***
- ***Analog and Mixed mode VLSI***
- ***Analog Communication***
- ***Optical fiber Communication***

11. ***Publications in National and International Journals & Conferences:***

National/International Journals

- "Design and Implementation of low power CMOS Analog to Digital Converter in cadence tool" Journal of Advances in Science and Technology, Vol. 12, Issue No. 25, (Special Issue) December-2016, ISSN 2230-9659

National/International Conferences

- "A 4-bit, 3.2GSPS Flash ADC with a new multiplexer based encoder" ICRISET , 2018.
- "Design and Implementation of low power CMOS Analog to Digital Converter in cadence tool" Journal of Advances in Science and Technology, Vol. 12, Issue No. 25, (Special Issue) December-2016, ISSN 2230-9659

12. ***Technical Papers presented:***

- "Design and Implementation of low power CMOS Analog to Digital Converter in cadence tool" Journal of Advances in Science and Technology, Vol. 12, Issue No. 25, (Special Issue) December-2016, ISSN 2230-9659

13. ***Books Published:***

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14. ***Workshop / Seminars Conducted:***

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15. ***Training Programmes/Workshops/Seminars/STTPs/Symposiums Attended:***

Sl. No.	Topic	Period	Date	Venue
1.	STTP on Artificial Intelligence and Medical Image processing	7 Days	16th to 22nd January 2018	KLE MSS CET, Belagavi
2.	Research Methodology	1 Day	11th November 2017	GIT, Belagavi
3.	NBA SAR Filling and preparedness for Assessment	3 Days	15th to 17th September, 2018	HIT, Nidasoshi
4	Two week ISTE STTP on CMOS Mixed Signal and RF VLSI Design	6 Days	30th January to 04th February 2017.	GIT, Belagavi
5.	Workshop on "Advanced VLSI Design using Cadence Design Suite"	3 Days	16th to 18th July 2014	JSSATE, Bagalore
6.	Workshop on "Latest Trends in EDA for Digital Electronics and VLSI Technology"	2 Days	22nd-23rd Sept. 2013	MMEC, Belgaum
7.	Application of Mathematics in Engg	2 Days	30th -31st August, 2010	HIT, Nidasoshi
8.	" Hands on Workshop on VLSI Design Using Cadence Tools suite"	3 Days	28th-30th July, 2010	Sambhram Institute of Technology, Bangalore
9.	Workshop on "CMOS VLSI and ASIC designs using MICROWIND tool"	2 Days	27th – 28th August 2009	SIT, Tumkur
10.	Workshop on CMOS VLSI and ASIC designs using Microwind	2 Days	31st August, to 2009 1st Sept.,2007	BMS Bangalore
11.	STTP on "Role of Women in Technical Education"	5 Days	2nd – 6th August 2004	AIT, Bangalore
12.	"Embeded System	1 Day	19th June	ISM, Bangalore

	Development" using ARM Controller		2004	

16. ***Awards/Achievements:***

17. ***Details of Memberships in Professional Societies:***

- *Life member of ISTE*
- *IEEE Member; Branch Counselor of IEEE HIT SB, Nidasoshi.*

18. ***Any other information***

Signature of the Faculty/Staff **Signature of the HOD**