

FACULTY PROFILE |

1. **Name in full** : Sujatha. S. Kamate
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 4. **Date of Birth** 01- 07- 1980
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 5. **Address for communication:** "Shivanand"
 Basaveshwar Nagar,
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6. **Educational qualifications :**

SI. No	Degree	University/Institution	Year	Specialization
1	Ph.D			
2	M.Tech.	VTU, Belgaum/ GIT, Belgaum	2012	Digital Electronics
3	B.E.	VTU, Belgaum/ HIT, Nidasoshi	2002	Electronics and communication

7. **Details of previous employment:**

SI. No	Name of the Institution/Organization	Period		Designation
		From	To	
1.	Hirasugar Institute of Technology, Nidasoshi	01-01-2017	Till date	Associate Professor
2.	Hirasugar Institute of Technology, Nidasoshi	01-10-2013	31-12-2016	Assistant Professor
3.	Hirasugar Institute of Technology, Nidasoshi	01-09-2008	30-09-2013	Senior Lecturer
4.	Hirasugar Institute of Technology, Nidasoshi	06-09-2004	31-01-2008	Lecturer
5.	C.B. Kore polytechnic, Chikodi	13-11-2002	03-09-2004	Lecturer
Total Experience in years				14.108yrs

8. **Date of Service in this Institution:**

06-09-2004

9. **Total Experience in years:** 14.10yrs

10. **Subjects of Interest:**

- **Signals and Systems**
- **Engineering Electromagnetics**
- **Microelectronic Circuits**
- **Control Systems**
- **Analog and Mixed mode VLSI**
- **Analog Communication**
- **Optical fiber Communication**

11. **Publications in National and International Journals & Conferences:**

National/International Journals

- “Design and Implementation of low power CMOS Analog to Digital Converter in cadence tool” Journal of Advances in Science and Technology, Vol. 12, Issue No. 25, (Special Issue) December-2016, ISSN 2230-9659

National/International Conferences

- “Design and Implementation of low power CMOS Analog to Digital Converter in cadence tool” Journal of Advances in Science and Technology, Vol. 12, Issue No. 25, (Special Issue) December-2016, ISSN 2230-9659

12. **Technical Papers presented:**

- “Design and Implementation of low power CMOS Analog to Digital Converter in cadence tool” Journal of Advances in Science and Technology, Vol. 12, Issue No. 25, (Special Issue) December-2016, ISSN 2230-9659

13. **Books Published:**

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14. **Workshop / Seminars Conducted:**

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15. Training Programmes/Workshops/Seminars/STTPs/Symposiums Attended:

Sl. No.	Topic	Period	Date	Venue
1.	Two week ISTE STTP on CMOS Mixed Signal and RF VLSI Design	6 Days	30 th January to 04 th February 2017.	GIT, Belagavi
	Workshop on “Advanced VLSI Design using Cadence Design Suite”	3 Days	16 th to 18 th July 2014	JSSATE, Bagalore
	Workshop on “Latest Trends in EDA for Digital Electronics and VLSI Technology”	2 Days	22nd-23rd	MMEC, Belgaum

4.	Workshop on Signals & System	3Days	4,5,6 Oct 2012	HIT, Nidasoshi
5.	Application of Mathematics in Engg	2 Days	30th-31 st Aug-2010	HIT, Nidasoshi
6.	“ Hands on Workshop on VLSI Design Using Cadence Tools suite”	3 Days	28th-30th July 2010	Sambhram Institute of Technology, Bangalore
7.	Workshop on “CMOS VLSI and ASIC designs using MICROWIND tool”	2 Days	27th – 28th	SIT, Tumkur
8.	and ASIC designs using MICROWIND tool” MICROWIND tool”		August 2009 1st Sept. 2007	Bangalore
9.	STTP on “Role of Women in Technical Education”	5 Days	2nd – 6th August 2004	AIT, Bangalore
10.	“Embedded System Development” using ARM Controller	1 Day	19th June 2004	ISM, Bangalore

16. **Awards/Achievements:**

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17. **Details of Memberships in Professional Societies:**

- Life member of ISTE
- IEEE Member; Branch Counselor of IEEE HIT SB, Nidasoshi.

18. **Any other information**

Signature of the Faculty/Staff

Signature of the HOD