S J P N Trust's Hirasugar Institute of Technology, Nidasoshi

FACULTY PROFILE

1. ***Name in full***	PRAMOD PATIL	
2. ***Contact Nos.***	+91 - 9731104059	
3. ***Email ID***	pramodpatil.ece@hsit.ac.in patil.pramod080@gmail.com	
4. ***Date of Birth***	15-06-1988	
5. ***Address for communication***	Assistant Professor, Dept. of ECE, HIT, Nidasoshi, Karnataka Pin - 591 236	A/p:- CHIKODI Tq:- CHIKODI Dt:- Belgaum *Karanataka* *Pin – 591201*

6. ***Educational qualifications :***

Sl. No	Degree	University/Institution	Year	Specialization
1	M. Tech.	VTU/SJCE, Mysore	2012	VLSI Design & Embedded Systems
2	B.E.	VTU /HIT Nidasoshi	2009	Electronics & Communication Engg

7. ***Details of previous employment:***

Sl. No	Name of the Institution/Organization	Period		Designation
		From	To	
1	Hirasugar Institute of Technology, Nidasoshi	06-08-2012	Till Now	Assistant Professor
			Total Experience in years	6 Years 00 Months

8. ***Date of Service in this Institution:*** 06-08-2012

9. ***Total Experience in years:*** 6 Years 00 Months

10. Subjects of Interest:

- Real time systems
- Real time operating systems
- Microprocessor/Microcontroller
- C/C++
- Network Analysis
- HDL
- Information Theory coding

11. Publications in National and International Journals & Conferences:

- "A multilayered Pereceptron reconfigurable ANN(Artificial Neural Networks)For image compression & Decompression " in National Level Conference on Recent Advancement in Engineering (NCRAE-12) at SETI,Panhala Kolhapur.
- "Implementation Of RISC Processor using Verilog" in Advances in Science & Technology.
- "Implementation of Soft Error-Resilient built in 2D Hamming Product code using Verilog " " in Advances in Science & Technology

12. Technical Papers presented:

- "A multilayered Pereceptron reconfigurable ANN(Artificial Neural Networks)For image compression & Decompression " in National Level Conference on Recent Advancement in Engineering (NCRAE-12) at SETI,Panhala Kolhapur.
- "Implementation Of RISC Processor using Verilog" in Advances in Science & Technology
- "Implementation of Soft Error-Resilient built in 2D Hamming Product code using Verilog" in Advances in Science & Technology.

13. Books Published:

- **NIL**

14. Workshop / Seminars Conducted:

- National Level Workshop on Embedded Linux Multimedia & Android Application, at HIT Nidasoshi on 23rd and 24th March 2013.
- Workshop on Professional Android Application Development, at HIT Nidasoshi, On 15th & 16th March 2014.
- National Level Workshop on Network Security-2 at Yadrav on 17th -19th October 2013

15.Training Programmes/Workshops/Seminars/STTPs/Symposiums Attended:

Sl. No.	Topic	Period		Venue
		From	TO	
1	Two-week ISTE STTP on CMOS,MIXED Signal and Radio frequency VLSI Design, by IIT Kharagpur	26/12/16	04/02/16	Gogte Institute of Technology, Belgaum
2	ICRIE-2016 Conference at HIT Nidasoshi.	08/09/16	09/09/16	HIT, Nidasoshi

16.Awards/Achievements:

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17. Details of Memberships in Professional Societies:

- ***LMISTE***

18.Any other information

Active role or participation in fund procurement from external bodies *(At least one in a year)*:

Name of the Project/Proposal/Event	Sanctioned/Requested Amount	Date of Sanction/Request
From ERTS Labs IIT,IIT Bombay Obtained 3 Firebird V -2560 bots.	81,000/-	08/09/16
Design And Implementation of 16 point FFT Processor for OFDM using HDL	3500=00 KSCST, Bangalore	27/03/17

Active Association with any related Industry/Institution ***(At least with one in a year):***

Name of the Industry/Institution	Nature of association	Dates of visit
1.ERTS Lab ,IIT Bombay	E-Yantra Trainer	Routine Updates
2.Nano Scientific Research Center Pvt.Ltd Hyderabad	Consultation as a RTL Designer Engineer	Regular updates online
3. Int-thoughts VLSI Design service organization Belgaum.	Consultation as a System Verilog/ Verilog/VHDL Expert	Regular updates online

Signature of the Faculty/Staff **Signature of the HOD**