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10CS33

Third Semester B.E. Degree Examination, June 2012
Logic Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. Realize basic gates, using only NOR gates. **(06 Marks)**

b. State the DeMorgan's theorems for two variables and prove the same using perfect induction. **(06 Marks)**

c. What is HDL? Explain verilog program the structures. **(08 Marks)**

2 a. Using K-Map technique simplify
$f(a, b, c, d) = \sum(1, 2, 4, 5, 6, 8, 9, 11, 15) + dc(3, 7, 13)$. **(05 Marks)**

b. Using Quine Mc Clusky method simplify,
$f(w, x, y, z) = \sum(0, 1, 3, 4, 7, 12, 14, 15)$ **(10 Marks)**

c. Does circuit in Fig. 2(c), experience hazard? If so, verify the same with timing diagram. **(05 Marks)**

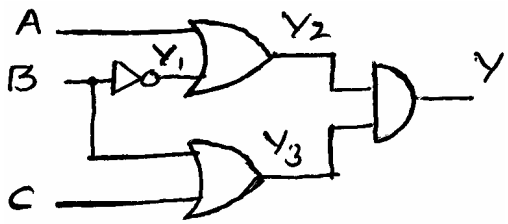

Fig. Q2(c)

3 a. Prove that a 4 : 1 Mux can be realized, using only 2 : 1 multiplexers. **(06 Marks)**

b. Using a 3 : 8 decoder realize a full adder. **(06 Marks)**

c. Implement the following Boolean functions, using suitable PLA.
$f_1 = \sum(0, 1, 4, 6)$, $f_2 = \sum(2, 3, 4, 6, 7)$
$f_3 = \sum(0, 1, 2, 6)$, $f_4 = \sum(2, 3, 5, 6, 7)$. **(08 Marks)**

4 a. Explain the characteristic of an ideal clock. **(04 Marks)**

b. What do you mean by characteristic equation of a flip – flop? Derive characteristic equation for S.R. Flip-Flop. **(06 Marks)**

c. Write the state table and state diagram for the circuit shown in Fig. Q4(c). **(10 Marks)**

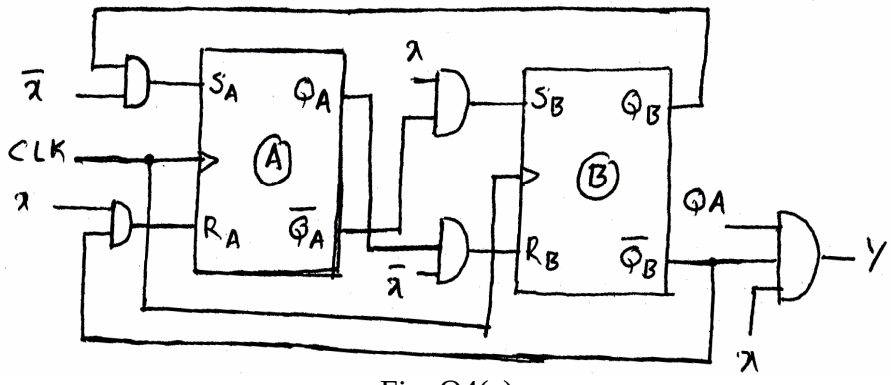

Fig. Q4(c)

PART – B

5 a. With neat timing diagram, explain the working of a 4-bit SISO register. **(10 Marks)**

b. With neat diagram, explain how 7495 can be connected to function as switched tail counter. **(05 Marks)**

c. Write verilog code for Johnson counter. **(05 Marks)**

6 a. Design mod – 12 counter using 7493. **(04 Marks)**

b. What do you mean by lockout condition in counters? Using J.K Flip-Flops design self correcting mod-6 counter. **(12 Marks)**

c. Bring out the differences between synchronous and asynchronous counters. **(04 Marks)**

7 a. With the aid of neat block diagrams, define Mealy and Moore machines. **(06 Marks)**

b. Draw the ASM chart for Mealy machine shown in Fig. Q7(b). **(04 Marks)**

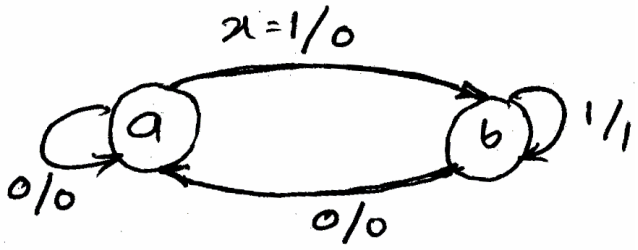

Fig. 7(b)

c. Reduce the state table in Table Q7(c), using implication table method. **(10 Marks)**

PS	NS		O/P	
	x = 0	x = 1	x = 0	x = 1
a	h	c	1	0
b	c	d	0	1
c	h	b	0	0
d	f	h	0	0
e	c	f	0	1
f	f	g	0	0
g	g	c	1	0
h	a	c	1	0

Table Q7(c)

8 a. With neat circuit diagram, explain the working of R – 2R ladder DAC. **(08 Marks)**

b. Explain the working of ADC. **(08 Marks)**

c. Calculate conversion time for 10-bit ADC operating at 5MHz clock. **(04 Marks)**

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