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06CS33

Third Semester B.E. Degree Examination, June 2012
Logic Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Simplify the following Boolean expressions using K-map :
i) $f(A, B, C) = \sum m(0, 2, 3, 5, 6) + d(4, 7)$.
ii) $f(W, X, Y, Z) = \sum m(0, 1, 2, 5, 6, 7, 8, 10, 11, 12, 13, 15)$. **(08 Marks)**

b. Simplify and realize using NAND gates only : $f(A, B, C) = \sum m(2, 3, 5, 7)$. **(04 Marks)**

c. Simplify using Quine – Mc Clusky tabulation method
$f(a, b, c, d) = \sum m(1, 2, 8, 9, 10, 12, 13, 14) + d(15)$. **(08 Marks)**

2 a. What is multiplexer? Construct 8 : 1 Mux using 2 : 1 Mux's. **(04 Marks)**

b. What is decoder? Realize the following Boolean function using 3 : 8 decoder and OR gate.
$f(a, b, c) = \sum m(1, 2, 5, 7)$. **(04 Marks)**

c. What is magnitude comparator? Design one bit magnitude comparator using basic gates. **(06 Marks)**

d. Implement following Boolean functions using $3 \times 4 \times 2$ PLA.
$f_1(a, b, c) = \sum m(0, 1, 3, 4)$
$f_2(a, b, c) = \sum m(1, 2, 3, 4, 5)$ **(06 Marks)**

3 a. Show the 8 bit addition of these decimal numbers in 2's compliment representation.
i) +83, +16
ii) +125, -68
iii) +37, -115
iv) -43, -78
v) -28, +15. **(10 Marks)**

b. Design 4 bit parallel adder/subtractor using full adders. **(10 Marks)**

4 a. What is monostable multivibrator? Illustrate with an example. **(04 Marks)**

b. Explain JK flip-flop operation along with state diagram. **(06 Marks)**

c. Write verilog/VHDL code for 'D' flip-flop. **(04 Marks)**

d. Convert RS flip-flop into JK flip-flop. **(06 Marks)**

PART – B

5 a. What is shift register? Explain with the suitable diagram and wave forms 4 bit Johnson and ring counters. **(10 Marks)**

b. Design a self correcting mod-5 counter using JK flip-flops and all the unused states leads to state, Q_A, Q_B, Q_C = 000. **(10 Marks)**

6 a. Obtain reduced state table and state diagram for the state table given below using implication table method : **(10 Marks)**

PS	NS		O/P	
	x = 0	x = 1	x = 0	x = 1
A	A	B	0	0
B	D	C	0	1
C	F	E	0	0
D	D	F	0	0
E	B	G	0	0
F	G	C	0	1
G	A	F	0	0

b. Design clocked sequential circuit for the state diagram given below Fig.Q.6(b), using JK flip-flop's. **(10 Marks)**

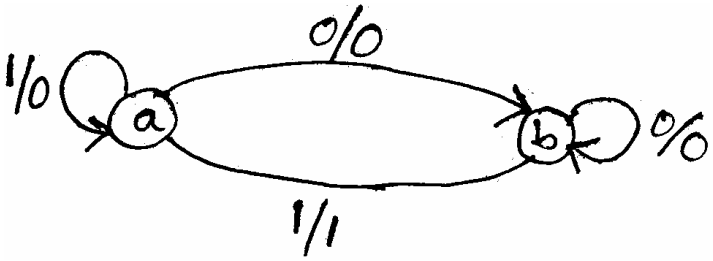

Fig.Q.6(b)

7 a. Draw a 4 bit D/A converter using R/2 R resistors and explain the working. **(10 Marks)**

b. Explain continuous A/D conversion with an example. **(10 Marks)**

8 a. Explain with neat diagram, CMOS inverter. **(06 Marks)**

b. Explain methods for interfacing CMOS device to TTL devices. **(10 Marks)**

c. What is MOSFET? Explain its working. **(04 Marks)**

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